REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-10-06

Document Description

Schematic Checklist for the LAN91C96 Operating at +3.3V, 100-pin QFP Package

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Document Number	Revision
SC471194	A

Schematic Checklist for LAN91C96

Information Particular for the 100-pin QFP Package

LAN91C96 QFP Phy Interface:

1. TPETXP (pin 77); This pin is the transmit twisted pair output positive connection from the internal phy. Operating the LAN91C96 QFP @ +3.3V requires a 6.04Ω series resistor to the transmit channel positive of the magnetics (low pass filter side).

2. TPETXDP (pin 74); This pin is the transmit twisted pair output positive pre-distortion connection from the internal phy. Operating the LAN91C96 QFP @ +3.3V requires a 24.3Ω series resistor to the transmit channel positive of the magnetics (low pass filter side).

3. These two outputs (TPETXP & TPETXDP) get resistively added together to form the TPO+ signal. They both connect, through their respective resistors, to the same pin of the magnetics. Refer to the latest SMSC reference schematic for details.

4. TPETXN (pin 75); This pin is the transmit twisted pair output negative connection from the internal phy. Operating the LAN91C96 QFP @ +3.3V requires a 6.04Ω series resistor to the transmit channel negative of the magnetics (low pass filter side).

5. TPETXDN (pin 76); This pin is the transmit twisted pair output negative pre-distortion connection from the internal phy. Operating the LAN91C96 QFP @ +3.3V requires a 24.3Ω series resistor to the transmit channel positive of the magnetics (low pass filter side).

6. These two outputs (TPETXN & TPETXDN) get resistively added together to form the TPO- signal. They both connect, through their respective resistors, to the same pin of the magnetics. Refer to the latest SMSC reference schematic for details.

7. TPERXP (pin 87); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 100Ω termination resistor. This pin connects to the receive channel positive connection of the magnetics (low pass filter side).

8. TPERXN (pin 86); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 100Ω termination resistor. This pin connects to the receive channel negative connection of the magnetics (low pass filter side).

9. Only one 100Ω receive termination resistor is required. Connect it between pins 86 & 87.

LAN91C96 QFP 10BASE-T Magnetics:

1. The center tap connection on the LAN91C96 side (low pass filter side) for the transmit channel should be connected to digital ground through a .01 μF capacitor.

2. The center tap connection on the LAN91C96 side (low pass filter side) for the receive channel should be connected to digital ground through a .01 μF capacitor.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel may be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground. Another option (depending on magnetics selected) is to no-connect this center tap.

4. The center tap connection on the cable side (RJ45 side) for the receive channel may be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground. Another option (depending on magnetics selected) is to no-connect this center tap.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to the TPO+ signal. Again, the TPO+ signal is derived from the resistive addition of pins 74 & 77 on the LAN91C96 QFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to the TPO- signal. Again, the TPO- signal is derived from the resistive addition of pins 75 & 76 on the LAN91C96 QFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPERXP (pin 87) of the LAN91C96 QFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPERXN (pin 86) of the LAN91C96 QFP.

10. It is very important to select the proper magnetics to use with the LAN91C96. The transformer must a 10BASE-T type with Low Pass Filters. The Low Pass Filters are very important in guaranteeing the proper operation of the LAN91C96. The turns ratio of both transmit & receive channels must be 1:1. Please refer to the latest version of SMSC's "Suggested Magnetics" Application Note for recommended magnetics for the LAN91C96.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Crystal Connections:

1. A 20.000 MHz crystal must be used with the LAN91C96. For exact specifications and tolerances refer to the latest revision LAN91C96 data sheet.

2. XTAL1 (pin 96) on the LAN91C96 QFP is the crystal circuit input. This pin requires a 10 – 30 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 97) on the LAN91C96 QFP is the crystal circuit output. We strongly recommend placing a 10 - 30Ω resistor in series with this pin to the crystal for EMI purposes. The other side of the resistor can then connect to a matching 10 – 30 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the value for the series resistor is system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

Attachment Unit Interface (AUI)

1. COLP (pin 83); This pin is the AUI collision positive differential input signal. It should connect directly to the COL+ connection on the AUI isolation transformer.

2. COLN (pin 82); This pin is the AUI collision negative differential input signal. It should connect directly to the COL- connection on the AUI isolation transformer.

3. RECP (pin 85); This pin is the AUI receive positive differential input signal. It should connect directly to the REC+ connection on the AUI isolation transformer.

4. RECN (pin 84); This pin is the AUI receive negative differential input signal. It should connect directly to the REC- connection on the AUI isolation transformer.

5. Also required across pins 84 & 85 of the LAN91C96 QFP, is a 240 ρF capacitor.

6. TXP (pin 79); This pin is the AUI transmit positive differential output signal. It should connect directly to the TXP connection on the AUI isolation transformer.

7. TXN (pin 78); This pin is the AUI transmit negative differential output signal. It should connect directly to the TXN connection on the AUI isolation transformer.

8. Pins 78 & 79 also require a resistive termination. Each pin requires a 154 Ω resistor to VCC for proper termination.

9. On the other side of the AUI isolation transformer, the system configuration is application dependant. In using a Coaxial Transceiver, the designer must implement as such. Please refer to the particular data sheets, application notes and/or other reference material for correct implementation of third party devices.

External Encoder/Decoder Interface (ENDEC)

1. The LAN91C96 may be used with an external ENDEC, one type is the 8023A style of Encoder / Decoder. To make this mode operational, pin 92 is the External Encoder/Decoder Mode input with an internal pull-up. This pin should be strapped high or left unconnected for normal operation (using the LAN91C96's internal encoder/decoder). Strapping this pin low configures the LAN91C96 to use an external encoder/decoder. This mode may also be referred to as a "7 wire interface".

2. RXD (pin 69); in this mode, this pin is an input to the LAN91C96 QFP with an internal pull-up. Connect this pin to the receive data output pin of the external ENDEC selected.

3. RXCLK (pin 71); in this mode, this pin is an input to the LAN91C96 QFP with an internal pull-up. Connect this pin to the receive clock output of the external ENDEC selected.

4. TXD (pin 70); in this mode, this pin is an output of the LAN91C96 QFP. Connect this pin to the transmit data input pin of the external ENDEC selected.

5. TXCLK (pin 68); in this mode, this pin is an input to the LAN91C96 QFP with an internal pull-up. Connect this pin to the transmit clock output pin of the external ENDEC selected.

6. nTXEN (pin 72); in this mode, this pin is an active low output of the LAN91C96 QFP. Connect this pin to the transmit enable input of the external ENDEC selected.

7. nCOLL (pin 79); in this mode, this pin is an active low input to the LAN91C96 QFP. Connect this pin to the collision sense output of the external ENDEC selected.

8. nCRS (pin 78); in this mode, this pin is an active low input to the LAN91C96 QFP. Connect this pin to the carrier sense output of the external ENDEC selected.

9. The rest of the design around the external ENDEC is application dependant. In using a Coaxial Transceiver, the designer must implement as such. Please refer to the particular data sheets, application notes and/or other reference material for correct implementation of third party devices.

Power Connections:

1. VDD pins on the LAN91C96 QFP are 13, 21, 40, 50, 61 & 100. They require connection to +3.3V.

2. Each power pin should have one .01 μF (or smaller) capacitor to decouple the LAN91C96. The capacitor size should be SMD_0603 or smaller.

3. AVDD pins on the LAN91C96 QFP are 73, 81 & 91. They require connection to +3.3V.

4. Each AVDD pin should have one .01 μF (or smaller) capacitor to decouple the LAN91C96. The capacitor size should be SMD_0603 or smaller.

5. Unless there are some issues with EMI problems, we recommend tying the VDD & the AVDD pins together and connect them to a +3.3V power plane.

6. If EMI problems are encountered, ferrite beads may be placed in series with the voltage connections of the VDD pins or the AVDD pins or both. This may or may not pay dividends at EMI testing. If ferrite beads are used, be certain to place bulk capacitors on each side of the ferrite bead.

Ground Connections:

1. Digital Ground pins on the LAN91C96 QFP are 2, 8, 18, 24, 31, 56, 66 & 94. They need to be connected directly to a solid ground plane.

2. AVSS pins on the LAN91C96 QFP are 80, 88 & 89. They need to be connected directly to a solid ground plane.

3. We recommend that the Digital Ground pins and the AVSS pins be tied together to the same ground plane.

EEPROM Interface:

1. EECS (pin 6) on the LAN91C96 QFP connects to the external EEPROM's CS pin.
2. EESK (pin 7) on the LAN91C96 QFP connects to the external EEPROM's serial clock pin.
3. EEDO (pin 4) on the LAN91C96 QFP connects to the external EEPROM's Data In pin.
4. EEDI (pin 5) on the LAN91C96 QFP connects to the external EEPROM's Data Out pin.
5. Be sure to strap the external EEPROM for 64 x 16 operation.
6. In order to use the EEPROM interface, be sure ENEEP (pin 3) can be strapped high. This input of the LAN91C96 QFP has an internal pull-up. If no serial EEPROM is used, this pin must tied to ground.
7. ISO0 (pin 98), ISO1 (pin 99) & ISO2 (pin 1) control what data is used from the EEPROM. Strap these pins to a known state. These inputs to the LAN91C96 QFP have internal pull-ups.

RBIAS Resistor:

1. RBIAS (pin 90) on the LAN91C96 QFP should connect to ground through a 2.43K Ω resistor when operating at +3.3V.

Required External Pull-ups:

1. IOCHRDY/nWAIT (pin 55) is an open-drain output of the LAN91C96 TQFP. An external pull-up resistor is required for this signal.
2. nIOCS16/nIOIS16 (pin 25) is an open-drain output of the LAN91C96 TQFP. An external pull-up resistor is required for this signal.
3. nBSELED (pin 69); This open-drain, active low output of the LAN91C96 QFP indicates the system is being accessed. Connect this pin to the cathode side of a LED and the anode side of the LED through a 511Ω resistor to +3.3V.
4. nLNKLED (pin 70); This open-drain, active low output of the LAN91C96 QFP indicates that link connection has been made in the Ethernet interface. Connect this pin to the cathode side of a LED and the anode side of the LED through a 511Ω resistor to +3.3V.
5. nTXLED (pin 72); This open-drain, active low output of the LAN91C96 QFP indicates that the device is transmitting data in the Ethernet interface. Connect this pin to the cathode side of a LED and the anode side of the LED through a 511Ω resistor to +3.3V.
6. nRXLED (pin 71); This open-drain, active low output of the LAN91C96 QFP indicates that the Ethernet interface is either transmitting or receiving data. This pin can be considered an Activity indicator, contrary to data sheet information. Connect this pin to the cathode side of a LED and the anode side of the LED through a 511Ω resistor to +3.3V.

CPU Interface:

1. A0 – A19 Address Bus: Please refer to the latest revision of the LAN91C96 Application Note for exact implementation of the CPU interface selected.

2. D0 – D15 Data Bus: Please refer to the latest revision of the LAN91C96 Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN91C96 Application Note for exact implementation of the CPU interface selected.

Miscellaneous:

1. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

2. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

3. PWRDWN (pin 68); this input to the LAN91C96 QFP is a power down pin with an internal pull-up. This pin should be strapped low for normal operation. To enter the power down state, the pin should be pulled high or left unconnected.

4. nEN16 (pin 93); This input to the LAN91C96 QFP has an internal pull-up. When low, the LAN91C96 is strapped for 16-bit bus operation mode. When high, the LAN91C96 works in 8-bit bus operation mode.

5. RESET (pin 67); This active high input to the LAN91C96 QFP resets the device. This input must be high for more than 100 nS to reset the part. This particular input buffer has Schmitt Trigger Hysteresis characteristics.

6. nROM/nPCMCIA (pin 95); This input pin is used to configure the LAN91C96 QFP in either Local Bus Mode or PCMCIA operation mode. Sampled at the end of reset, if this pin is connected to ground, the LAN91C96 will be configured for PCMCIA mode. Since it has an internal pull-up, if left unconnected or pulled high, the LAN91C96 will be configured for Local Bus Mode. In Local Bus Mode, this pin can be used as a ROM chip select.

LAN91C96 QFP QuickCheck Pinout Table:

Use the following table to check the LAN91C96 QFP shape in your schematic.

LAN91C96 QFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	IOS2	31	VSS	51	nIORD	81	AVDD
2	VSS	32	A3	52	nIOWR	82	COLN
3	ENEEP	33	A4	53	nMEMR	83	COLP
4	EEDO	34	A5	54	AEN	84	RECN
5	EEDI	35	A6	55	IOCHRDY	85	RECP
6	EECS	36	A7	56	VSS	86	TPERXN
7	EESK	37	A8	57	D0	87	TPERXP
8	VSS	38	A9	58	D1	88	AVSS
9	D8	39	A10	59	D2	89	AVSS
10	D9	40	VDD	60	D3	90	RBIAS
11	D10	41	A11	61	VDD	91	AVDD
12	D11	42	A12	62	D4	92	nXENDEC
13	VDD	43	A13	63	D5	93	nEN16
14	D12	44	A14	64	D6	94	VSS
15	D13	45	A15	65	D7	95	nROM
16	D14	46	A16	66	VSS	96	XTAL1
17	D15	47	A17	67	RESET	97	XTAL2
18	VSS	48	A18	68	PWRDWN	98	IOS0
19	INTR0	49	A19	69	nBSELED	99	IOS1
20	INTR1	50	VDD	70	nLNKLED	100	VDD
21	VDD			71	nRXLED		
22	INTR2			72	nTXLED		
23	INTR3			73	AVDD		
24	VSS			74	TPETXDP		
25	nIOCS16			75	TPETXN		
26	nSBHE			76	TPETXDN		
27	BALE			77	TPETXP		
28	A0			78	TXN		
29	A1			79	TXP		
30	A2			80	AVSS		

Reference Material:

1. SMSC LAN91C96 Data Sheet; check web site for latest revision.

2. SMSC LAN91C96 @ +3.3V EVB Schematic, Assembly No. 6254; check web site for latest revision.

3. SMSC LAN91C96 @ +3.3V EVB PCB, Assembly No. 6254; order PCB from web site.

4. SMSC LAN91C96 @ +3.3V EVB PCB Bill of Materials, Assembly No. 6254; check web site for latest revision.

5. SMSC LAN91C96 Application Notes AN 8-9 & AN 8-15; check web site for latest revision.

6. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.