dsPIC33FJ12MC202

dsPIC33FJ12MC202 PIM Information Sheet

The dsPIC33FJ12MC202 PIM is designed to demonstrate the capabilities of the dsPIC33FJ12MC202 family of general purpose devices using the Explorer 16 Development Board and the PICtail™ Plus daughter boards.

The dsPIC33FJ12MC202 is a high-performance 16-bit digital signal controller within a small 28-pin 6x6 mm QFN package.

The dsPIC33FJ12MC202 is equipped with Peripheral Pin Select (PPS), which allows many of the digital peripherals to be remapped to use any number of pins on the device.

The PIM takes advantage of PPS by using zero ohm resistors to connect the I/O to the 100-pin Explorer 16 Development Board. Simply removing the zero ohm resistors and using the test points associated with each I/O pin (i.e., RP0, RP1, etc.), allows the designer to reroute the pin to any of the available pins on the Explorer 16 Development Board. This capability enables easier and faster design times.

Table 1 shows the mapping between the Explorer 16 functions and the device pins.

TABLE 1: 28-PIN TO 100-PIN PINOUT

Device Pin Number	dsPIC33FJ12MC202	PIM Pin Number	Functional Description
1	PGED1/AN2/RP0/CN4/RB0	35, 28	DC Bus/POT
2	PGEC1/AN3/RP1/CN5/RB1	20, 41	POT/Phase 1 Voltage Feedback
3	AN4/RP2/CN6/RB2	83, 42	Switch 1/Phase 2 Voltage Feedback
4	AN5/RP3/CN7/RB3	84, 43	Switch 2/Phase 3 Voltage Feedback
5	Vss	15	
6	OSCI/CLKI/CN30/RA2	63	OSCI
7	OSCO/CLKO/CN29/RA3	64	OSCO
8	PGED3/SOSCI/RP4/CN1/RB4	27	Debug
9	PGEC3/SOSCO/T1CK/CN0/RA4	26	Debug
10	VDD	16	
11	ASDA1/RP5/CN27/RB5	20, 68, 83	QEB/Hall Sensor A/Switch 1
12	ASCL1/RP6/CN24/RB6	21, 69, 84	QEA/Hall Sensor B/Switch 2
13	INT0/RP7/CN23/RB7	22, 70	Index/Hall Sensor C
14	TCK/ PWM2H1/SCL1/RP8/CN22/RB8	18	Fault 1A
15	TDO /PWM2L1/SDA1/RP9/CN21/RB9	19, 71	Fault Reset/PWM Enable
16	VSS	36	
17	VCAP/VDDCORE	85	
18	TDI/PWM1H3/RP10/CN16/RB10	3	PWM1H3
19	TMS/PWM1L3/RP11/CN15/RB11	100	PWM1L3
20	PWM1H2/RP12/CN14/RB12	99	PWM1H2
21	PWM1L2/RP13/CN13/RB13	98	PWM1L2
22	PWM1H1/RP14/CN12/RB14	94	PWM1H1
23	PWM1L1/RP15/CN11/RB15	93	PWM1L1
24	AVSS	31	
25	AVDD	30	
26	$\overline{\text{MCLR}}$	13	
27	PGED2/AN0/VREF+/CN2/RA0	20, 25	POT/Phase 1 Current Feedback
28	PGEC2/AN1/VREF-/CN3/RA1	32, 24	BUS Shunt/Phase 2 Current Feedback

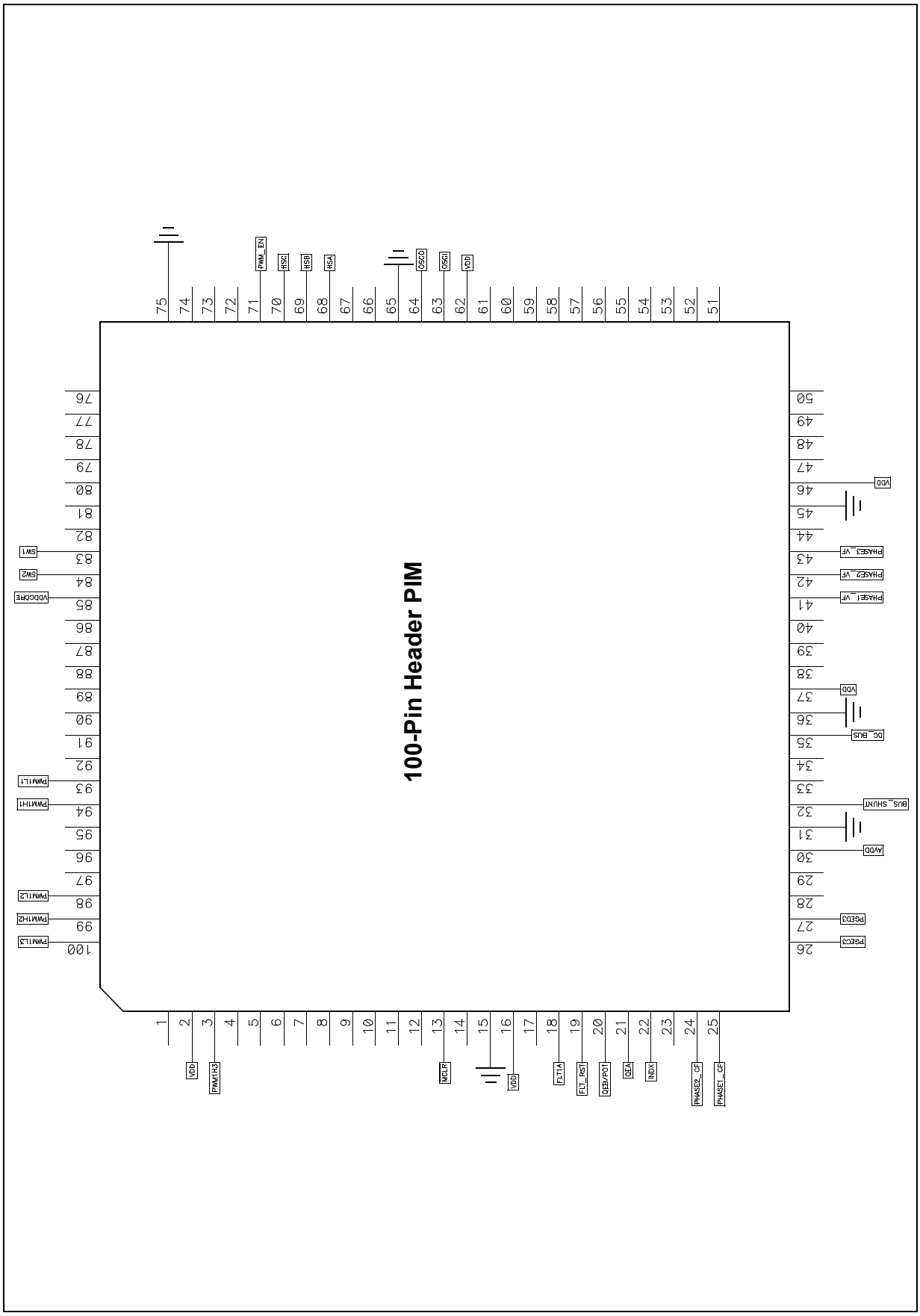

FIGURE 1: 100-PIN HEADER SCHEMATIC

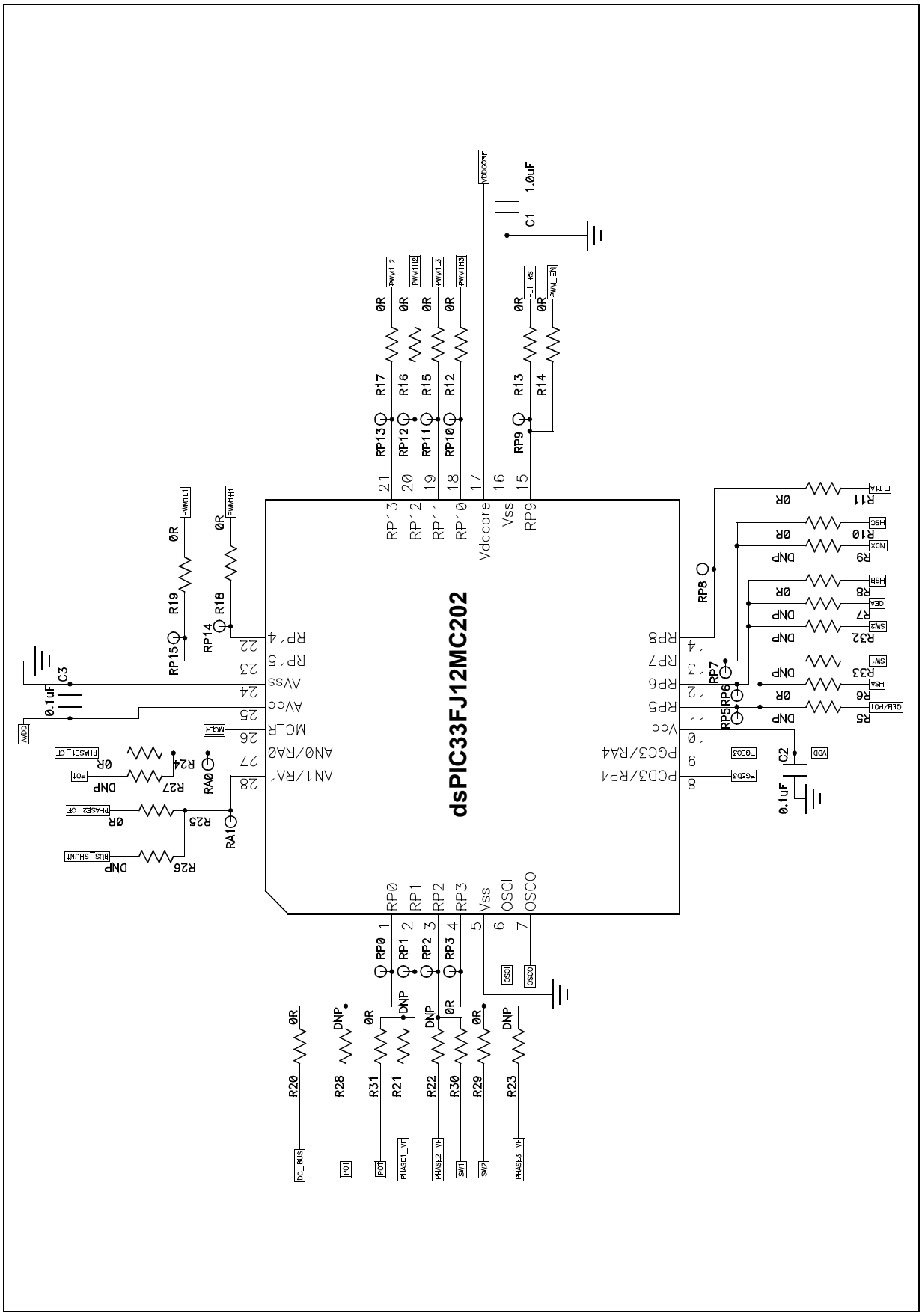

FIGURE 2: 28-PIN DEVICE SCHEMATIC

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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