REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-04-08
B	Added EEPROM_SIZE_x Pull-up/Pull-down Details		6-27-08

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9311I, 128-pin XVTQFP Package

SMSC
80 Arkay Drive
Hauppauge, New York 11788

Document Number	Revision
SC471214	B

Schematic Checklist for LAN9311I

Information Particular for the 128-pin XVTQFP Package

LAN9311I XVTQFP Phy No. 1 Interface:

1. TXP1 (pin 111); This pin is the transmit twisted pair output positive connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

2. TXN1 (pin 110); This pin is the transmit twisted pair output negative connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. RXP1 (pin 116); This pin is the receive twisted pair input positive connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

5. RXN1 (pin 115); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

LAN9311I XVTQFP Phy No. 2 Interface:

1. TXP2 (pin 126); This pin is the transmit twisted pair output positive connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

2. TXN2 (pin 127); This pin is the transmit twisted pair output negative connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. RXP2 (pin 123); This pin is the receive twisted pair input positive connection to the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

5. RXN2 (pin 124); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

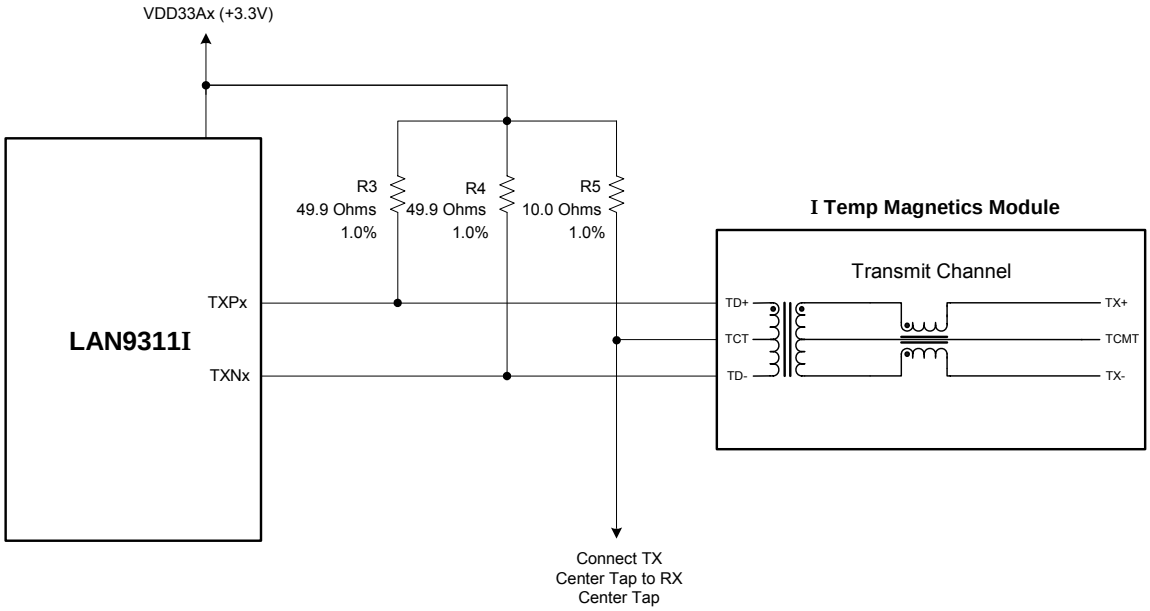

Figure 1 – Transmit Channel Connections and Terminations

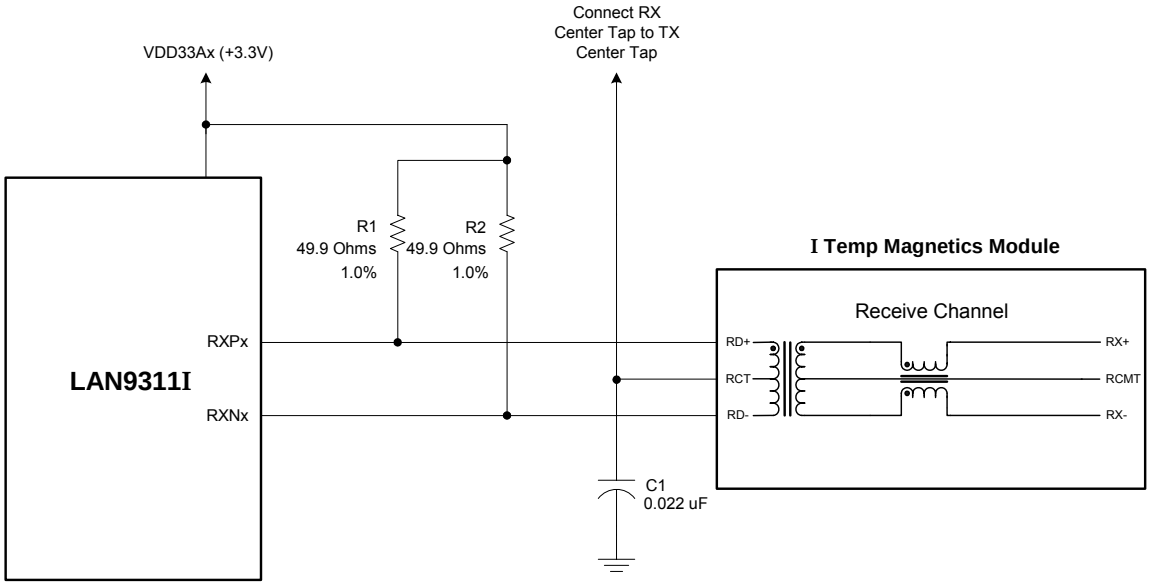

Figure 2 - Receive Channel Connections and Terminations

LAN9311I XVTQFP Magnetic No. 1:

1. The center tap connection on the LAN9311I side for the transmit channel must be connected to VDD33A1 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the primary magnetics also connects to the receive channel center tap of the primary magnetics.

2. The center tap connection on the LAN9311I side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the primary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP1 (pin 111) of the LAN9311I XVTQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN1 (pin 110) of the LAN9311I XVTQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP1 (pin 116) of the LAN9311I XVTQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN1 (pin 115) of the LAN9311I XVTQFP.

10. When using the SMSC LAN931x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

11. In order to guarantee IEEE compliancy over the entire temperature range of operation, the magnetics used in conjunction with the LAN9311I must be rated for Industrial Temperature use.

LAN9311I XVTQFP Magnetic No. 2:

1. The center tap connection on the LAN9311I side for the transmit channel must be connected to VDD33A2 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the secondary magnetics also connects to the receive channel center tap of the secondary magnetics.

2. The center tap connection on the LAN9311I side for the receive channel is connected to the transmit channel center tap on the secondary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the secondary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the secondary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the secondary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP2 (pin 126) of the LAN9311I XVTQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN2 (pin 127) of the LAN9311I XVTQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP2 (pin 123) of the LAN9311I XVTQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN2 (pin 124) of the LAN9311I XVTQFP.

10. When using the SMSC LAN931x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

11. In order to guarantee IEEE compliancy over the entire temperature range of operation, the magnetics used in conjunction with the LAN9311I must be rated for Industrial Temperature use.

RJ45 Connector No. 1 & No. 2:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN9311I XVTQFP are 7, 13, 21, 27, 33, 39, 46, 54, 64, 66, 72, 73, 81, 87, 93 & 100. They require a connection to +3.3V.

2. Each VDD33IO power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A1) pins for Phy No. 1 on the LAN9311I XVTQFP are pins 114 & 117. They require a connection to +3.3V through one ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

5. The analog supply (VDD33A2) pins for Phy No. 2 on the LAN9311I XVTQFP are pins 122 & 125. They require a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. Each VDD33A2 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

7. VDD33BIAS (pin 120), this pin serves as the master bias voltage supply for the LAN9311I. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

8. The VDD33BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

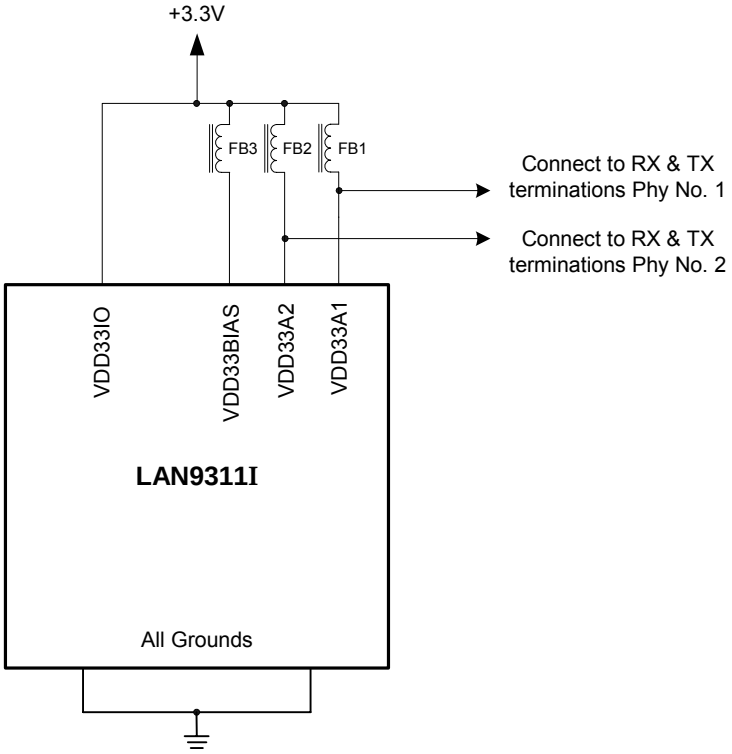

Figure 3 – LAN9311I +3.3V Power Connections

VDD18CORE:

1. VDD18CORE (pins 3, 14, 40, 65, 74, 88 & 104), these seven pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF bypass capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 74 requires a bulk capacitor placed as close as possible to pin 74. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 0.1 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9311I use only. **Do Not** power other circuits or devices with this supply.

2. VDD18PLL (pin 107), this pin supplies power for the core PLL. This pin must be connected to VDD18CORE through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD18PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18CORE to VDD18TX2. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9311I.

5. **Do Not**, under any circumstances, use either VDD18CORE or VDD18TX2 to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9311I only.

VDD18TX2:

1. VDD18TX2 (pin 121), this pin is used to provide bypassing for the +1.8V PHY regulator. This pin requires a 0.01 μF bypass capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 121 requires a bulk capacitor placed as close as possible to pin 121. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 0.1 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9311I use only. **Do Not** power other circuits or devices with this supply.

2. VDD18TX1 (pin 118), this pin supplies power to both PHY transmitters. This pin must be connected directly to the VDD18TX2 (pin 121) pin.

3. The VDD18TX1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9311I. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18TX2 to VDD18CORE. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9311I.

5. **Do Not**, under any circumstances, use either VDD18TX2 or VDD18CORE to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9311I only.

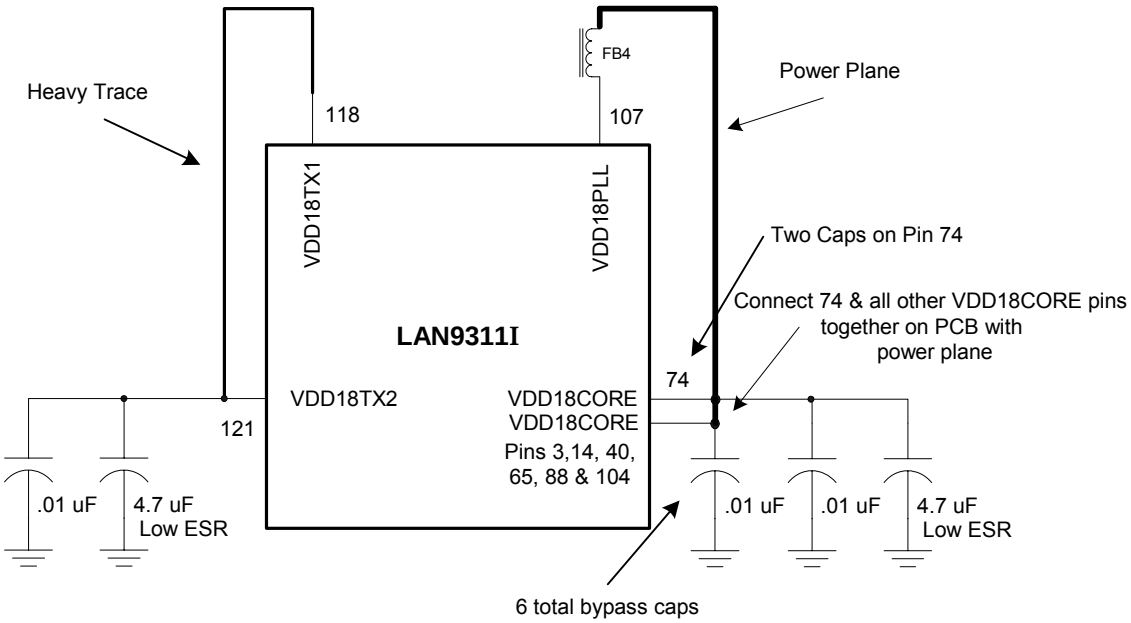

Figure 4 LAN9311I +1.8V Power Connections

Ground Connections:

1. The digital ground pins (VSS) on the LAN9311I XVTQFP are 18, 48, 80, 97, 112, 113 & 128. They need to be connected directly to a solid, contiguous ground plane.

2. Both the digital ground pins (VSS) and the GND_CORE pins on the LAN9311I XVTQFP are all connected internally to the exposed die paddle ground. The EDP Ground pad on the underside of the LAN9311I must be connected directly to a solid, contiguous digital ground plane.

3. We recommend that the Digital Ground pins and the EDP pin be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9311I XVTQFP. For exact specifications and tolerances refer to the latest revision LAN9311I data sheet.

2. XI (pin 105) on the LAN9311I XVTQFP is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 106) on the LAN9311I XVTQFP is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the crystal used in conjunction with the LAN9313I must be rated for Industrial Temperature use.

EEPROM Interfaces:

The LAN9311I supports two different types of EEPROM interfaces. Three pins configure the EEPROM interface on the LAN9311I XVTQFP:

1. EEPROM_TYPE (pin 98), functions as a configuration input and is used to select the EEPROM type. Upon the deassertion of reset, this pin selects the EEPROM type depending upon what state it is in.

   When this pin is high, the Philips I^2C EEPROM mode of operation is selected. For this mode, this pin must be pulled high with an external 10.0K Ω pull-up resistor.

   When this pin is low, the National Semiconductor Microwire™ EEPROM mode of operation is selected. For this mode, this pin must be pulled low with an external 10.0K Ω pull-down resistor.

2. EEPROM_SIZE_1 (pin 99), functions as a configuration input and is used to configure the high bit of the EEPROM size range. This bit is not used for I^2C EEPROMs. For Microwire EEPROMS, upon the deassertion of reset, the combination of this pin & the EEPROM_SIZE_0 (pin 101) pin, determines the EEPROM size. For example, configurations range from 128 x 8 for 00h to 2048 x 8 for 10h. 11h is currently reserved. See the LAN9311I Data Sheet for additional details.

3. EEPROM_SIZE_0 (pin 101), functions as a configuration input and is used to configure the low bit of the EEPROM size range. For I^2C EEPROMs, this bit is used solely. For Microwire EEPROMs, both size bits are utilized. For both types of EEPROMs, upon the deassertion of reset, this pin determines the EEPROM size. For example, for I^2C EEPROMs, configurations range from 16 x 8 when this pin is low through 65536 x 8 when this pin is latched high. See the LAN9311I Data Sheet for additional details.

4. The EEPROM_SIZE_1 & EEPROM_SIZE_2 pins do not have internal terminations (internal pull-ups or pull-downs). In order to select the proper configuration, external 10.0K Ω resistors must be used to terminate each pin either high or low. They should not be left as No Connects.

Microwire™ (3-wire) EEPROM Interface:

1. EECS (pin 101) on the LAN9311I XVTQFP connects to the external EEPROM's CS pin.

2. EECLK (pin 99) on the LAN9311I XVTQFP connects to the external EEPROM's serial clock pin.

3. EEDI (pin 96) on the LAN9311I XVTQFP connects to the external EEPROM's Data Out pin.

4. EEDO (pin 98) on the LAN9311I XVTQFP connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style EEPROM that matches the organization and size as determined by the configuration pins.

I^2C (2-wire) EEPROM Interface:

1. EE_SCL (pin 99) on the LAN9311I XVTQFP connects to the external I^2C EEPROM's serial clock pin.

2. EE_SDA (pin 96) on the LAN9311I XVTQFP connects to the external I^2C EEPROM's Data In/Out pin.

3. Be sure to select a 2-wire style EEPROM that matches the organization and size as determined by the configuration pins.

EXRES Resistor:

1. EXRES (pin 119) on the LAN9311I XVTQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 63) may require an external pull-up resistor if this output is programmed as an Open Drain type.

2. PME (pin 62) may require an external pull-up resistor if this output is programmed as an Open Drain type.

3. EE_SDA (pin 96) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode.

4. EE_SCL (pin 99) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode.

5. nP1LED0/GPIO0 (pin 92) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

6. nP1LED1/GPIO1 (pin 91) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

7. nP1LED2/GPIO2 (pin 90) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

8. nP1LED3/GPIO3 (pin 89) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

9. nP2LED0/GPIO4 (pin 86) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

10. nP2LED1/GPIO5 (pin 85) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

11. nP2LED2/GPIO6 (pin 84) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

12. nP2LED3/GPIO7 (pin 83) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

CPU Interface:

1. A1 – A9 Address Bus: Please refer to the latest revision of the LAN9311I Application Note for exact implementation of the CPU interface selected.

2. D0 – D15 Data Bus: Please refer to the latest revision of the LAN9311I Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN9311I Application Note for exact implementation of the CPU interface selected.

4. The LAN9311I is a native Little Endian device. It is the designers' responsibility to ensure that the selected CPU has compatible Endianess.

   END_SEL (pin 61), functions as a configuration input and is used to establish the Endianess of the Host Bus data byte lanes.

   With this pin low, the LAN9311I will operate in Little Endian mode. This can be considered the most typical application. This mode can be achieved with a 10.0K Ω pull-down resistor added to this pin.

   If this pin is high, the LAN9311I will operate in Big Endian mode. This mode can be achieved with a 10.0K Ω pull-up resistor added to this pin.

   This pin can also be changed dynamically. SMSC suggests an upper address line (A12) as a suitable control line. Please refer to the latest LAN9311I data sheet and design guides to determine compatibility.

Miscellaneous:

1. There are 24 No-Connect pins on the LAN9311I. It is very important that these pins remain as no-connects. These pins are 1, 2, 4, 5, 6, 8, 9, 10, 11, 12, 15, 16, 17, 19, 20, 22, 23, 24, 76, 94, 95, 102, 103 & 109.

   Caution: To ensure normal device operation, pin 102 must be low at all times. Pin 102 has an internal pull-down. Do not add any type of external pull-up or other circuit connection to this pin as this will result in configuring the device disabled. This pin must be left as a No-Connect.

2. FIFO_SEL (pin 60), when driven high, all accesses to the LAN9311I are to the RX or TX Data FIFOs. In this mode, the address input is ignored. Typical use will involve connecting an upper address line (A11 is recommended) to this pin to determine functionality. For normal operation (FIFO_SEL disabled), a 1.0K Ω external pull-down resistor must be attached to this pin.

3. LED_EN (pin 67), functions as a configuration input and is used to establish the functionality of the nPxLEDx/GPIOx pins. Upon the deassertion of reset, this pin selects the functionality depending upon what state it is in.

   With this pin low, the LAN9311I will configure all eight LED/GPIO pins as GPIOs. This mode can be achieved with a 1.0K Ω pull-down resistor added to this pin.

   If this pin is high, the LAN9311I will configure all eight LED/GPIO pins as LEDs. This mode can be achieved by leaving this pin as a no-connect as this pin has an internal pull-up.

4. PHY_ADDR_SEL (pin 68), functions as a configuration input and is used to establish the default MII Management address values for the three internal PHYs. See the LAN9311I data sheet for further details on PHY addressing. Upon the deassertion of reset, this pin selects the functionality depending upon what state it is in.

   With this pin low, the PHY addressing will start with 00h. This mode can be achieved with a 1.0K Ω pull-down resistor added to this pin.

   If this pin is high, the PHY addressing will start with 01h. This mode can be achieved by leaving this pin as a no-connect as this pin has an internal pull-up.

5. nRST (pin 71), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9311I. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9311I will rely on its internal power-on reset circuitry.

6. AUTO_MDIX_1 (pin 69), this pin enables the HP Auto MDIX feature of port 1 of the LAN9311I.

   This pin has a weak internal pull-up, so this pin can be left as a no-connection in order to take advantage of the Auto MDIX feature (Auto MDIX enabled).

   To disable the Auto MDIX feature, a 1.0K Ω external pull-down resistor must be attached to this pin.

7. AUTO_MDIX_2 (pin 70), this pin enables the HP Auto MDIX feature of port 2 of the LAN9311I.

   This pin has a weak internal pull-up, so this pin can be left as a no-connection in order to take advantage of the Auto MDIX feature (Auto MDIX enabled).

   To disable the Auto MDIX feature, a 1.0K Ω external pull-down resistor must be attached to this pin.

8. TEST1 (pin 75), this pin must be connected to +3.3V.

9. TEST2 (pin 108), this pin must be connected to +3.3V.

10. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

11. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

12. In order to guarantee IEEE compliancy over the entire temperature range of operation, all components used in the customer's application must be rated for Industrial Temperature use. Processors, crystals, oscillators, magnetics and all integrated circuits must be rated properly to avoid operational inconsistencies.

LAN9311I XVTQFP QuickCheck Pinout Table:

Use the following table to check the LAN9311I XVTQFP shape in your schematic.

LAN9311I XVTQFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC1	33	VDD33IO	65	VDD18CORE	97	VSS
2	NC2	34	D8	66	VDD33IO	98	EEDO
3	VDD18CORE	35	D7	67	LED_EN	99	EECLK
4	NC3	36	D6	68	PHY_ADDR_SEL	100	VDD33IO
5	NC4	37	D5	69	AUTO_MDIX_1	101	EECS
6	NC5	38	D4	70	AUTO_MDIX_2	102	NC22
7	VDD33IO	39	VDD33IO	71	nRST	103	NC23
8	NC6	40	VDD18CORE	72	VDD33IO	104	VDD18CORE
9	NC7	41	D3	73	VDD33IO	105	XI
10	NC8	42	D2	74	VDD18CORE	106	XO
11	NC9	43	D1	75	TEST1	107	VDD18PLL
12	NC10	44	D0	76	NC19	108	TEST2
13	VDD33IO	45	A9	77	GPIO11	109	NC24
14	VDD18CORE	46	VDD33IO	78	GPIO10	110	TXN1
15	NC11	47	A8	79	GPIO9	111	TXP1
16	NC12	48	VSS	80	VSS	112	VSS
17	NC13	49	A7	81	VDD33IO	113	VSS
18	VSS	50	A6	82	GPIO8	114	VDD33A1
19	NC14	51	A5	83	nP2LED3	115	RXN1
20	NC15	52	A4	84	nP2LED2	116	RXP1
21	VDD33IO	53	A3	85	nP2LED1	117	VDD33A1
22	NC16	54	VDD33IO	86	nP2LED0	118	VDD18TX1
23	NC17	55	A2	87	VDD33IO	119	EXRES
24	NC18	56	A1	88	VDD18CORE	120	VDD33BIAS
25	D15	57	nRD	89	nP1LED3	121	VDD18TX2
26	D14	58	nWR	90	nP1LED2	122	VDD33A2
27	VDD33IO	59	nCS	91	nP1LED1	123	RXP2
28	D13	60	FIFO_SEL	92	nP1LED0	124	RXN2
29	D12	61	END_SEL	93	VDD33IO	125	VDD33A2
30	D11	62	PME	94	NC20	126	TXP2
31	D10	63	IRQ	95	NC21	127	TXN2
32	D9	64	VDD33IO	96	EEDI	128	VSS
129				EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package			

Notes:

Reference Material:

1. SMSC LAN9311I Data Sheet; check web site for latest revision.
2. SMSC LAN9311I EVB Schematic, Assembly No. 6470; check web site for latest revision.
3. SMSC LAN9311I EVB PCB, Assembly No. 6470; order PCB from web site.
4. SMSC LAN9311I EVB PCB Bill of Materials, Assembly No. 6470; check web site for latest revision.
5. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.