AT91SAM7SE Microcontroller Series Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM7SE series of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM7SE Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontroller

Application Note

6261E–ATARM–18-Dec-07

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM7SE Series Microcontrollers on Atmel's Web site.

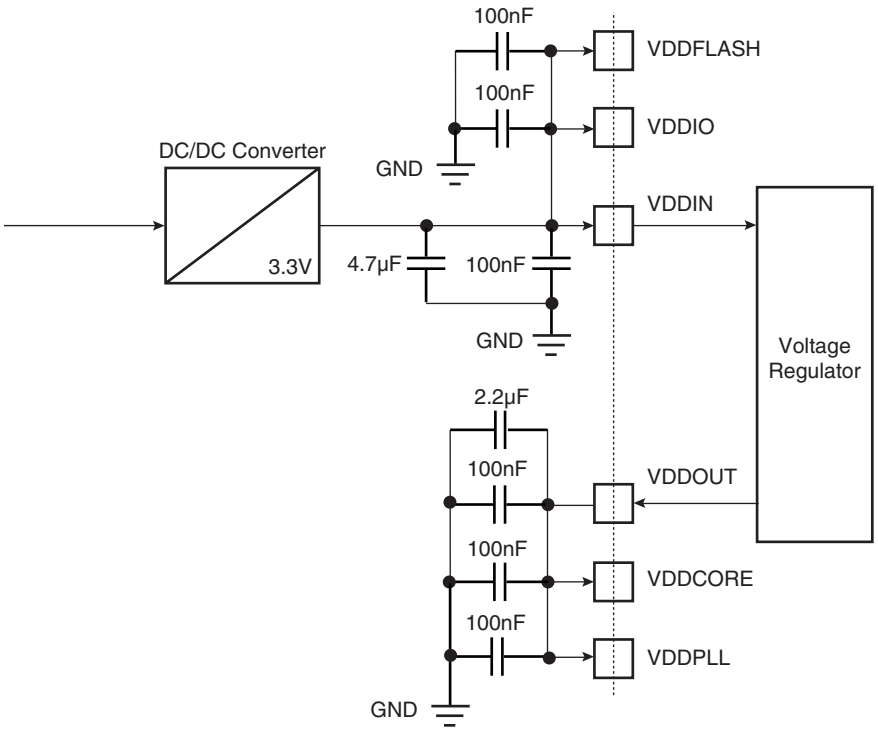
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM7SE Series Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI® Datasheet
Evaluation Kit User Guide	AT91SAM7SE-EK Evaluation Board User Guide
Using SDRAM on AT91SAM7SE Microcontrollers	Using SDRAM on AT91SAM7SE Microcontrollers
NAND Flash Support in AT91SAM7SE Microcontrollers	NAND Flash Support in AT91SAM7SE Microcontrollers

3. Schematic Check List

3.3V Single Power Supply Strategy (On-chip Voltage Regulator Used)
To reduce power consumption, voltage regulator can be put in standby mode.

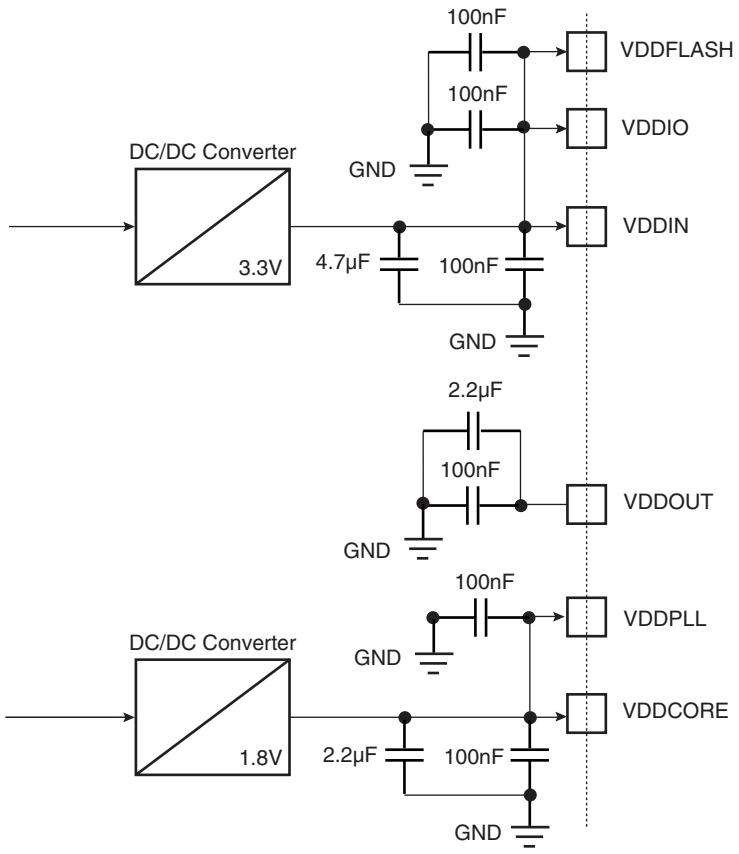


3.3V Single Power Supply Schematic Example:[1]
On-chip voltage regulator is used - power supply on VDDIO 3.3V

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	Powers on-chip voltage regulator and ADC. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to guarantee 1.8V stability
	VDDIO	3.0V to 3.6V or 1.65V to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers I/O lines. Dual voltage range supported.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers Flash (charge pump) and USB transceivers.

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF)[1][2]	Powers device and flash logic, on-chip RC.
	VDDPLL	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

3.3V and 1.8V Dual Power Supply Strategy (On-chip Voltage Regulator NOT Used and ADC Used)
To reduce power consumption, voltage regulator can be put in standby mode.

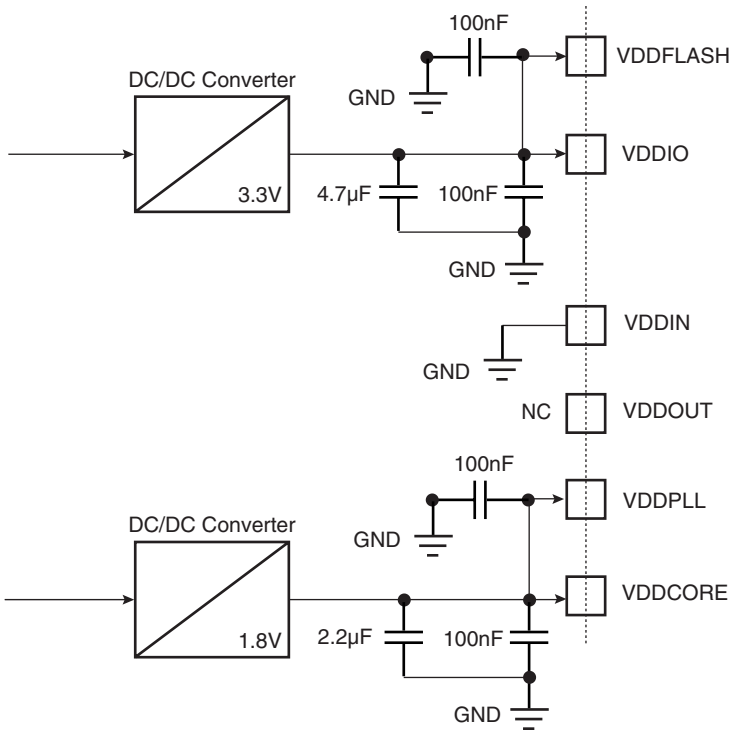


3.3V and 1.8V Dual Power Supply Schematic Example:(1)
On-chip voltage regulator is not used - ADC is used - power supply on VDDIO: 3.3V

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)(1)(2)	Powers ADC. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)(1)(2)	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to prevent on-chip voltage regulator oscillations.
	VDDIO	3.0V to 3.6V or 1.65V to 1.95V Decoupling capacitor (100 nF)(1)(2)	Powers I/O lines. Dual voltage range supported.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers Flash (charge pump) and USB transceivers. **$V_{VDDFLASH}$ must always be superior or equal to $V_{VDDCORE}$.**

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Powers device logic, on-chip RC and Flash. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

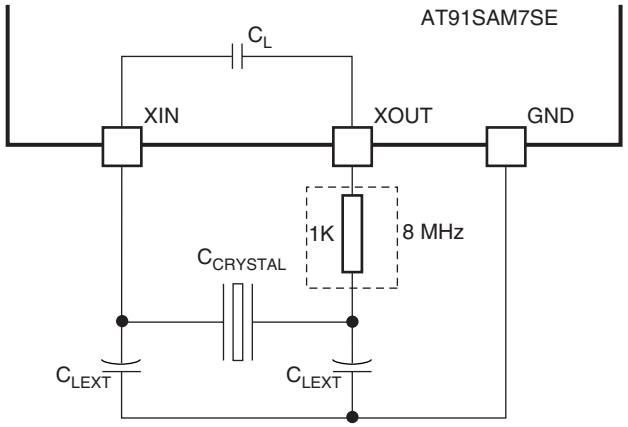
3.3V and 1.8V Dual Power Supply Strategy (On-chip Voltage Regulator and ADC NOT Used)

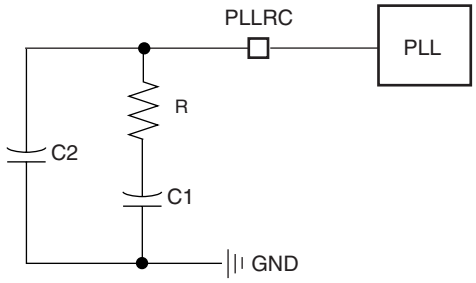


3.3V and 1.8V Dual Power Supply Schematic Example:(1)
On-chip voltage regulator is not used - ADC is not used - power supply on VDDIO: 3.3V

☑	Signal Name	Recommended Pin Connection	Description
	VDDIN	Connected to GND.	-
	VDDOUT	Can be left unconnected.	-
	VDDIO	3.0V to 3.6V or 1.65V to 1.95V Decoupling/Filtering capacitors (100 nF and 4.7µF)(1)(2)	Powers I/O lines. Dual voltage range supported. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers Flash (charge pump) and USB transceivers. **$V_{VDDFLASH}$ must always be superior or equal to $V_{VDDCORE}$.**

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Powers device logic, on-chip RC and Flash. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Internal Equivalent Load Capacitance (C_L): For the AT91SAM7SE512/256: C_L = 20 pF For the AT91SAM7SE32: C_L = 11 pF Crystal Load Capacitance to check ($C_{CRYSTAL}$).  Example: on the AT91SAM7SE512/256, for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$ = 20 pF, no external capacitors are required ($C_{CRYSTAL} = C_L$) Refer to the electrical specifications of the AT91SAM7SE series datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected.	1.8V Square wave signal (VDDPLL) External Clock Source up to 50 MHz Duty Cycle: 40 to 60%

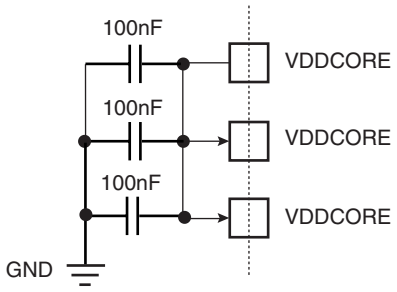
☑	Signal Name	Recommended Pin Connection	Description
	PLLRC	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: “ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  R, C1 and C2 must be placed as close as possible to the pins.

☑	Signal Name	Recommended Pin Connection	Description
		ICE and JTAG[3]	
	TCK	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TD0	Floating	Output driven at up to V_{VDDIO}
	JTAGSEL	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDIO} to enter JTAG Boundary Scan. Internal pull-down resistor (15 kOhm).
		Flash Memory	
	ERASE	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDIO} to erase the General Purpose NVM bits (GPNVMx), the whole flash content and the security bit (SECURITY). Internal pull-down resistor (15 kOhm). This pin is debounced by the RC oscillator to improve the glitch tolerance. Minimum debouncing time is 220 ms.
		Reset/Test	
	NRST	Application dependant. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIO} (100 kOhm) is available for User Reset and External Reset control.
[5]	TST	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDIO} to enter Fast Flash Programming (FFPI) mode[5] Internal pull-down resistor (15 kOhm).

☑	Signal Name	Recommended Pin Connection	Description
PIO			
	PAx - PBx - PCx	Application Dependant	All PIOs are pulled-up inputs at reset and are schmitt trigger inputs. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
ADC			
	ADVREF	2.6V to V_{VDDIN}. Decoupling capacitor(s).	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used, connect ADVREF to GND.
	AD0 to AD7	0V to V_{ADVREF}	AD0 to AD3 are digital pulled-up inputs at reset. AD4 to AD7 are pure analog inputs. To reduce power consumption, if ADC is not used, connect AD4, AD5, AD6 and AD7 to GND.
USB Device (UDP)			
	DDP	Application Dependant(6)	Integrated programmable pull-up resistor (UDP_TXVC) No internal pull-down resistor. To reduce power consumption, if USB Device is not used, DDP must be left unconnected.
	DDM	Application Dependant(6)	No internal pull-down resistor. To reduce power consumption, if USB Device is not used, DDM must be left unconnected.
SDRAM Controller (SDRAMC)			
	SDCK	–	SDRAM Clock This pin is tied low after reset. Maximum output frequency: 48.2 MHz for V_{VDDIO} from 3.0V to 3.6V 25 MHz for V_{VDDIO} from 1.65V to 1.95V

Notes: 1. These values are given only as a typical example.

2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.

5. See: Test Pin description in I/O Lines Considerations section of the AT91SAM7SE datasheet for more details on the different conditions to enter FFPI mode.
6. Example of USB Device connection:
   As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up.
   To prevent over consumption when the host is disconnected, an external pull-down can be added to DDP and DDM.
   A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM7SE datasheet.

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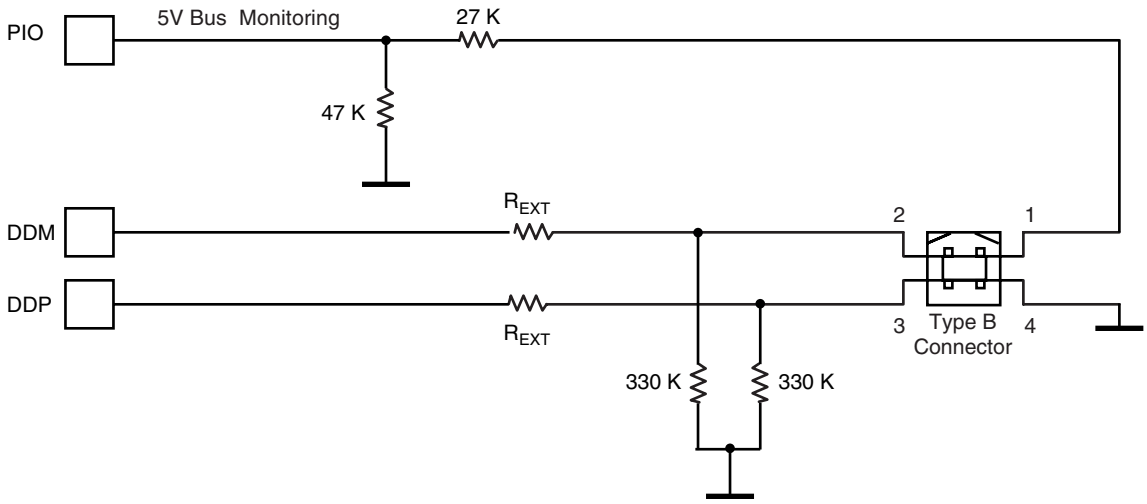

4. External Bus Interface (EBI) Hardware Interface

Table 4-1 details the connections to be applied between the EBI pins and the external devices for each Memory Controller:

Table 4-1. EBI Pins and External Static Devices Connections

Pin	Pins of the Interfaced Device						
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	SDRAM[1]	CompactFlash	CompactFlash True IDE Mode	NAND Flash[2]
Controller	**SMC**			**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0 - I/O7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8 - I/O15[3]
D16 - D31	–	–	–	D16 - D31	–	–	–
A0/NBS0	A0	–	NLB	DQM0	A0	A0	–
A1/NBS2	A1	A0	A0	DQM2	A1	A1	–
A2 - A9	A2 - A9	A1 - A8	A1 - A8	A0 - A7	A2 - A9	A2 - A9	–
A10	A10	A9	A9	A8	A10	A10	–
A11	A11	A10	A10	A9	–	–	–
SDA10	–	–	–	A10	–	–	–
A12	A12	A11	A11	–	–	–	–
A13 - A14	A13 - A14	A12 - A13	A12 - A13	A11 - A12	–	–	–
A15	A15	A14	A14	–	–	–	–
A16/BA0	A16	A15	A15	BA0	–	–	–
A17/BA1	A17	A16	A16	BA1	–	–	–
A18 - A20	A18 - A20	A17 - A19	A17 - A19	–	–	–	–
A21/NANDALE	A21	A20	A20	–	–	–	ALE
A22/REG/NANDCLE	A22	A21	A21	–	REG	–	CLE
NCS0	CS	CS	CS	–	CFRNW[4]	CFRNW[4]	–
NCS1/SDCS	CS	CS	CS	CS	–	–	–
NCS2/CFCS1	CS	CS	CS	–	CFCS1[4]	CFCS1[4]	–
NCS3/NANDCS	CS	CS	CS	–	–	–	CE[7]
NCS4/CFCS0	CS	CS	CS	–	CFCS0[4]	CFCS0[4]	–
NCS5/CFCE1	CS	CS	CS	–	CE1	CS0	–
NCS6/CFCE2	CS	CS	CS	–	CE2	CS1	–
NCS7	CS	CS	CS	–	–	–	–
NANDOE	–	–	–	–	–	–	RE
NANDWE	–	–	–	–	–	–	WE
NRD/CFOE	OE	OE	OE	–	OE	–	
NWR0/NWE/CFWE	WE	WE[5]	WE	–	WE	–	
NWR1/NBS1/CFIOR	WE	WE[5]	NUB	DQM1	IOR	IOR	–
NBS3/CFIOW	–	–	–	DQM3	IOW	IOW	–

Table 4-1. EBI Pins and External Static Devices Connections (Continued)

Pin	Pins of the Interfaced Device						
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	SDRAM[1]	CompactFlash	CompactFlash True IDE Mode	NAND Flash[2]
Controller	**SMC**			**SDRAMC**	**SMC**		
SDCK	–	–	–	CLK	–	–	–
SDCKE	–	–	–	CKE	–	–	–
RAS	–	–	–	RAS	–	–	–
CAS	–	–	–	CAS	–	–	–
SDWE	–	–	–	WE	–	–	–
NWAIT	–	–	–	–	WAIT	WAIT	–
Pxx[6]	–	–	–	–	CD1 or CD2	CD1 or CD2	–
Pxx[6]	–	–	–	–	–	–	CE[7]
Pxx[6]	–	–	–	–	–	–	RDY

Notes:
1. For SDRAM connection examples, refer to "Using SDRAM on AT91SAM7SE Microcontrollers", application note.
2. For NAND Flash connection examples, refer to "Interfacing NAND Flash with AT91SAM7SE Microcontrollers", application note.
3. I/O8 - I/O15 bits used only for 16-bit NAND Flash.
4. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
5. NWR1 enables upper byte writes. NWR0 enables lower byte writes.
6. Any free PIO line.
7. CE connection depends on the NAND Flash.
   For standard NAND Flash devices, it must be connected to any free PIO line.
   For "CE don't care" 8-bit NAND Flash devices, it can be either connected to NCS3/NANDCS or to any free PIO line.
   For "CE don't care" 16-bit NAND Flash devices, it must be connected to any free PIO line.

5. AT91SAM Boot Program Hardware Constraints

See AT91SAM Boot Program section of the AT91SAM7SE datasheet for more details on the boot program.

5.1 SAM-BA Boot

The SAM-BA™ Boot Assistant supports serial communication via the DBGU or the USB Device Port:

- DBGU Hardware Requirements: 3 to 20 MHz crystal or 1 to 50 MHz external clock.
- USB Device Hardware Requirements: 18.432 MHz crystal.

Revision History

Doc. Rev	Comments	Change Request Ref.
6261A	First issue	
6261B	Precision added to the pin descriptions of "TD0" and "NRST" on page 11. Added "External Bus Interface (EBI) Hardware Interface" on page 14.	3511
6261C	Table 4-1, "EBI Pins and External Static Devices Connections," on page 14, I/O[8:15] bits added in NAND Flash column. Note added to table: I/O8 - I/O15 bits used only for 16-bit NAND Flash.	3743
6261D	Section 3. "Schematic Check List" Precisions added to schematics of power supply strategies. Note added for use in harsh environments. Precisions added to ADC and USB descriptions. Table 4-1, "EBI Pins and External Static Devices Connections," on page 14 added notes to table for SDRAM, NAND FLash and references to pertinent app notes,	3859
	"Clock, Oscillator and PLL" on page 9, schematic updated C_L equations updated	approval loop
6261E	Updated Recommended Pin Connection for "JTAGSEL", "ERASE", "TST"	5073

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