VSC8512
Application Note
VSC8512 Design Guide

Contents

1 Revision History 1.0

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in May, 2010.

2 Introduction

This document provides useful guidelines for the design and layout of printed circuit boards utilizing the VSC8512 12-Port 10/100/1000BASE-T PHY, with the intent of allowing the reader to achieve first pass design success.

2.1 References

2.1.1 Vitesse Documents

- VSC8512 Datasheet

2.1.2 IEEE Standards

- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification

2.1.3 External Documents

- High Speed Digital Design, Author: Howard Johnson, PH.D., ISBN 0-13-395724-1

3 Key Item Checklist

The following items should be checked by the designer of any VSC8512 design to make sure the design has sufficiently accounted for the behavior. Failing to do so might result in extended prototype debug, board redesign, and production delays.

- Following are the required pin connections.
  - Coma ModeJTAG TRST pulled down
  - REFCLK selected
  - 3 REF_FILT & REF_REXT pairs connected
  - PHY Address configured
  - SMI MDIO and MDINT pulled up
- Check copper magnetics meets specifications and connection requirements
- Review VSC8512 Errata Document

4 Design Aids

This section describes the design aids of VSC8512.

4.1 Reference Design

Review the reference design (http://www.vitesse.com/products/download.php?fid=4394&number=VSC8512) for proper device connections and usage.

4.2 IBIS Model

The IBIS (Input/Output Buffer Information Specification) model is used to model the connections to the PHY.

Note: No SPICE model is provided for the PHY due to limited usefulness of such a model to the dynamically adapting interface.

4.3 BSDL File

The BSDL (Boundary Scan Description Language) file is used for JTAG testing. See the JTAG discussion in Section 10.7 and in the VSC8512 datasheet. Both IEEE 1149.1 and IEEE 1149.6 (AC-JTAG) are provided.

Note: JTAG does have register access capability on the VSC8512.

4.4 OrCAD Symbol

An OrCAD symbol is provided for the VSC8512 for use with Cadence PCB design tools.

Note: Design Aids will be made available on the VSC8212 product website as they become available.

5 Copper Magnetics Modules

The following relevant parameters are found in datasheets provided by manufacturers of copper magnetics modules. The values that Vitesse recommends for each are needed for correct operation with a typical board design.

Note: Board layout can have a negative impact on PHY copper interface performance.

5.1 Return Loss Parameter

The magnetics return loss is the key for proper PHY CAT5 operation. The Best column in the following table is based on performance characteristics of the Pulse H5008 discrete magnetics. The minimum return loss column is based on system minimum requirements specified by IEEE.

Note: Use of magnetics with minimum level performance characteristics should be carefully considered, as they may leave little to no margin for board design.

The following table lists the magnetics return loss requirements.

Table 1 • Magnetics Return Loss Requirements

Frequency (MHz)	Best (dB)	Minimum (dB)
1–30	–18	–16
40	–18	–16
50	–12	–10
60–80	–12	–10
100	–10	–8

5.2 Secondary Magnetics Parameters

- DM-CM ~30db marginal EMI to 100MHz
- Insertion Loss < 1.5 dB to 1 MHz–100 MHz
- CM-CM ~30 db marginal EMI to 100MHz
- Avoid primary side common mode chokes
- 12 core magnetics generally offers better EMI
- If only 10/100 Mbs operation then requirements decrease
- Crosstalk and CM-DM are not important in the selection

6 EMI Management

This section describes the EMI management of the VSC8512.

6.1 PHY EMI testing

When EMI test sweeps are performed the typical PHY frequency spike is at 125 MHz and at integer multiples to 1 GHz. Passing EMI testing requires attention to board layout and in particular to ground plane design.

6.2 MAC Interface Design Keys

- Short traces
- Keep differential pairs (n and p) the same length

6.3 Copper Interface Design Keys

- Short traces
- Keep differential pairs (n and p) the same length
- Consider adding small (< 5 pf) capacitors to ground only if needed based on testing results
- In order to pass the IEEE standard ESD tolerance tests it is important that the board ground and chassis ground be isolated across the Magnetic Module. However, it is recommended that a placeholder for a 0.1 µf capacitor be included in the design for reducing EMI if needed. The magnetic module used is very important to ensure good EMI performance. Contact your local Vitesse representative to get the datasheet and magnetics design checked.

6.4 Grounding Considerations

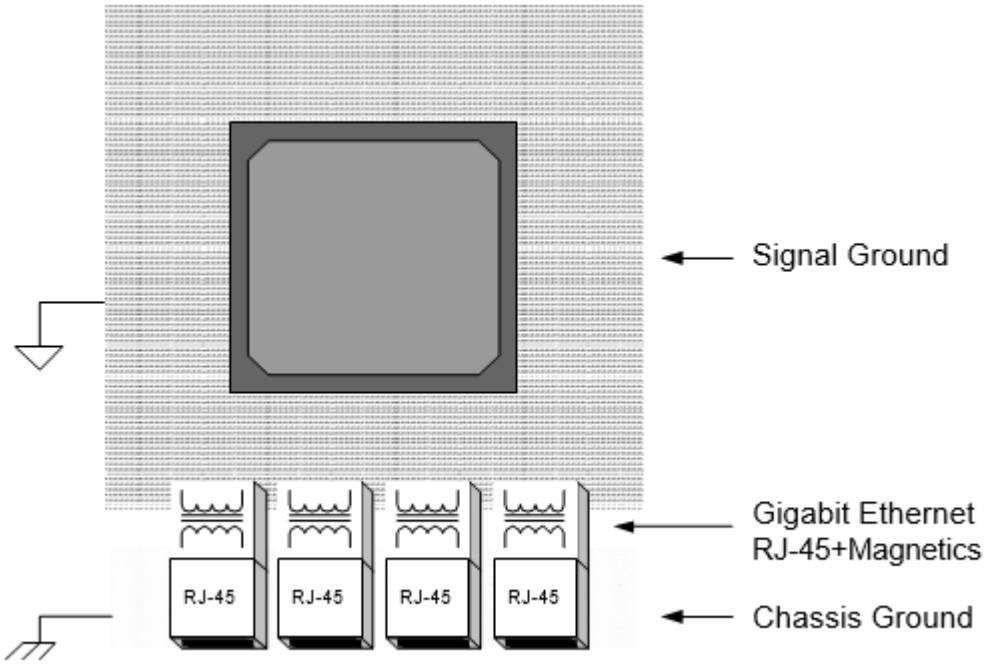
This section describes the grounding considerations.

6.4.1 Ground Isolation

A separate chassis ground region should be allocated in order to isolate the board from ESD events and to prevent a common-mode noise ground path. This separate chassis ground should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

The following figure illustrates the ground plane layout.

Figure 1 • Ground Plane Layout

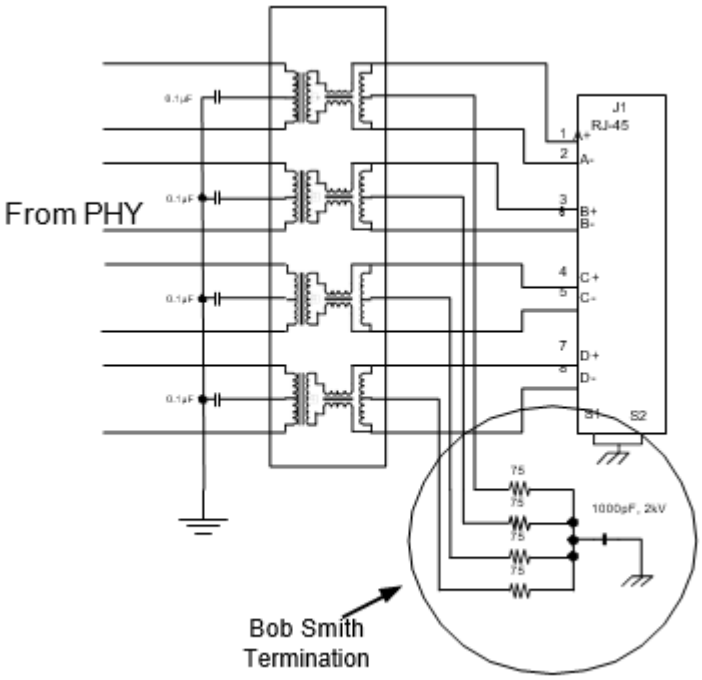


6.5 Bob Smith Termination

In addition, the “Bob Smith” termination impedance should be connected between the chassis ground and the cable-side center taps of the transformer module.

The following figure illustrates the Bob Smith termination diagram.

Figure 2 • Bob Smith Termination Diagram



7 Power Supply Considerations

This section describes the power supply considerations of the VSC8512.

7.1 Power Supply Planes

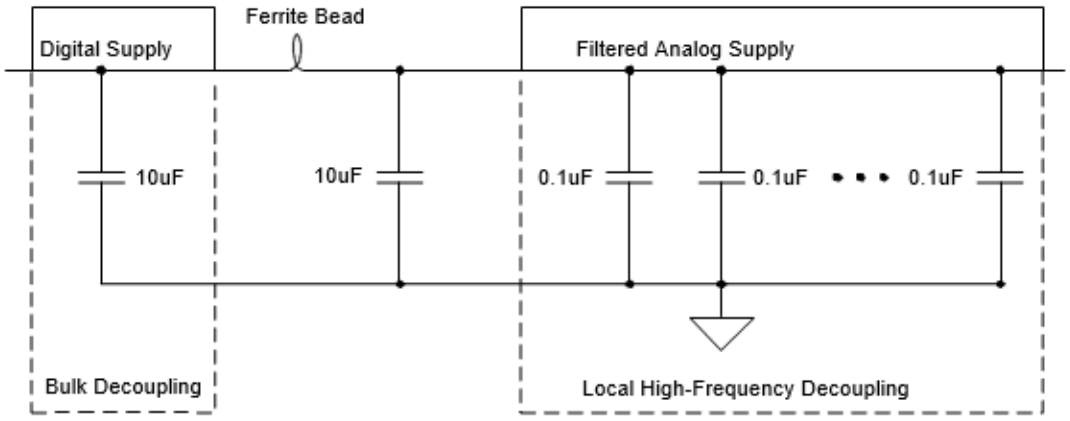
The VSC8512 requires four power supplies that connect to the power pins of the device: 2.5 V, 1.0 V, filtered analog 2.5 V, and 1.0 V. In four layer PCBs with only one designated power plane, proper design techniques must be followed to prevent random system events such as CRC errors. Each of these connections to the power pins of the VSC8512 requires the lowest resistive drop possible with properly placed local decoupling as described in Sections 6.2 and 6.3.

7.2 Analog Power Plane Filtering

A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

The following figure illustrates the filtered supply schematic.

Figure 3 • Filtered Supply Schematic



The beads should be chosen to have the following characteristics.

- Current rating of at least 150% of the maximum current of the power supply
- Impedance of 80 Ω to 100 Ω at 100 MHz

Recommended beads are as follows.

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with zero Ω resistors, once thorough evaluation of system performance is completed.

7.3 Local Decoupling

Bulk decoupling capacitors should be tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be placed as closed to the VSC8512's power pins as possible. The best location for local decoupling capacitors is on the bottom of the board, directly under the device.

7.4 Power Supply and Clock Sequencing

Power Supply voltages must be stable and clocking valid for 1 ms before releasing NRESET.

7.5 Power Supply Estimated Requirements

See the VSC8512 datasheet for specific application requirements.

The following table lists the PHY power supply estimates used for evaluation board power supply.

Table 2 • PHY Power Supply Estimates Used for Evaluation Board Power Supply

Power Supply	Voltage (V)	Maximum Current (A)	Maximum Power (W)
VDD	1.0	2.000	2.00
VDD_A	1.0	0.350	0.35
VDD_VS	1.0	0.200	0.20
VDD_IO	2.5	0.500	1.25
VDD_AL	1.0	0.900	0.90
VDD_AH	2.5	1.350	3.38
Total Power for PHY			**8.08**

8 Thermal Considerations

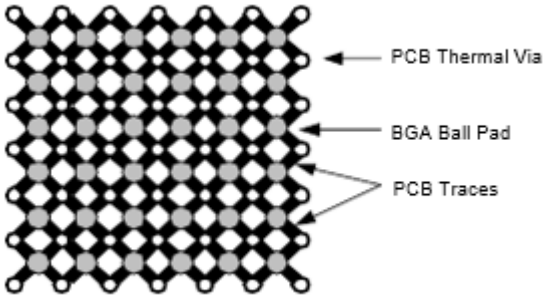
This section describes the thermal considerations of the VSC8512.

8.1 Heat Removal from Device

For proper cooling, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern (See the following figure). Each of these “thermal vias” should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB.

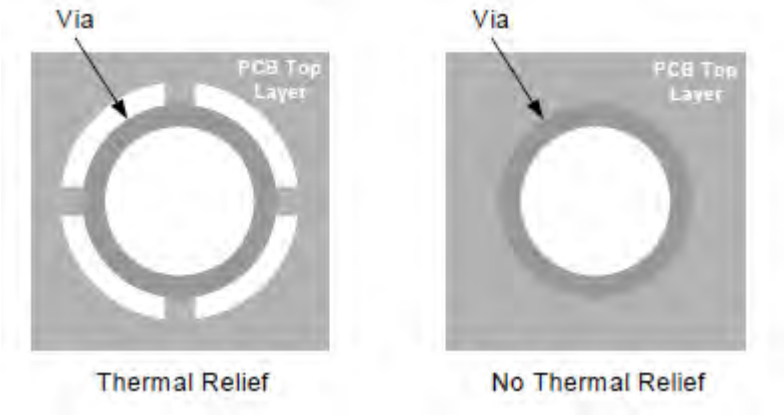
The following figure illustrates the thermal via layout.

Figure 4 • Thermal Via Layout



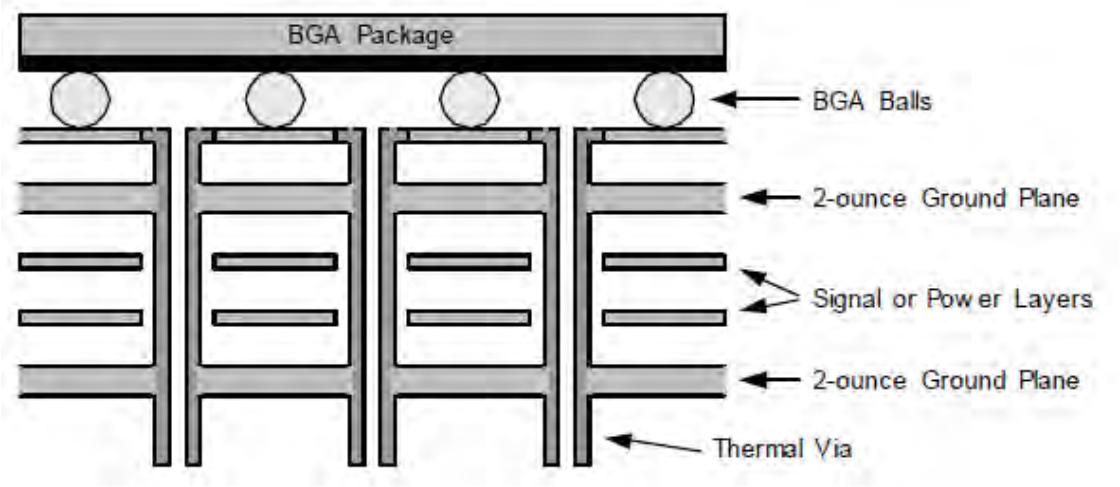
When connecting these thermal vias to ground planes, it is not advisable to use thermal-relief connection traces, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer, as shown in the following figure.

Figure 5 • Thermal Vias



In order to dissipate heat below the BGA package, the PCB thermal vias should connect to the solid ground planes within the board. It is recommended that each ground plane have a minimum thickness of two ounces for best θ_{JB} thermal dissipation, as shown in the following figure.

Figure 6 • Thermal Ground Plane Connections



8.2 Temperature Measurement

This section describes the temperature measurement of the VSC8512.

8.2.1 Temperature Diode Options

This section describes the temperature diode options of the VSC8512.

8.2.1.1 Built-in Diode with A/D Converter

See the VSC8512 datasheet for temperature diode register details. Key points are as follows.

- There are three temperature monitoring controllers: TMON0, TMON1, and TMON2. TMON0 is for PHY 0–3, TMON1 is for PHY 4–7, TMON2 is for PHY 8-12.
- Only one monitor can be checked or active at a time
- Register 28G
  - 28G.15:14-Selects the active thermal diode (or TMONx)
- Register 26G
  - 26G.5- Tells the A/D to read the selected thermal diode
    26G.6- Enables continual reading of the thermal diode and uses selected averaging method
    26G.1:0- Sets the mode of averaging (in general this is setting a window size for averaging). The wider the window, the slower the change.
- The alarm threshold in register 27G applies to the selected TMON only. The other two TMONs are not being read or do not have any digital functions performed with their values.
- Temperature C = 135.3–0.71 * (Reg28G.7:0) + DT
  (where DT is the Tolerance ± 8.2 °C maximum)

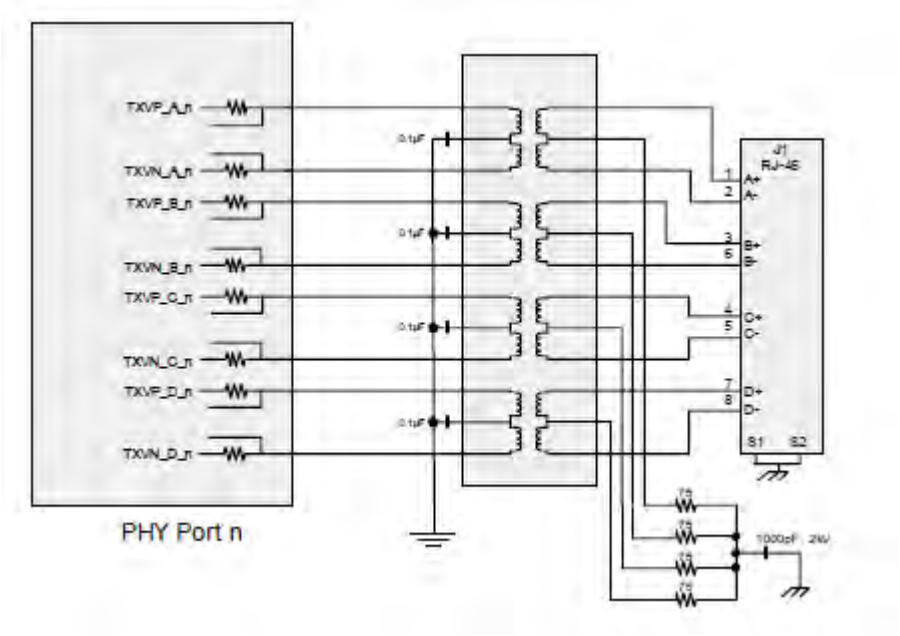
8.2.1.2 Discrete Diode

The pins THERMDA and THERMDC are the anode and cathode of an on-chip thermal diode. Note that the cathode is connected to the internal chip ground. The grounded cathode might not work with some thermal sensors which require complete control of the thermal diode. Vitesse PHY reference boards use the Maxim MAX6642 temperature sensor.

9 Copper Interface

The following figure illustrates the copper PHY media.

Figure 7 • Copper/CAT-5 Interface Diagram



9.1 Layout Considerations

The TXVPx_n and TXVNx_n pins interface to the external CAT5 cable and are organized in four differential pairs (x = A, B, C, and D) for each PHY port (n = 0…7). When routing these pairs on a PCB, the characteristics must match one of the following.

- Route each trace single-ended with a characteristic impedance of 50 Ω

referenced to ground

OR

- Route each positive and negative trace on each port as differential pairs with 100 Ω characteristic differential impedance.

Regarding modeling, less than 5 mm traces are not an issue, 5 mm–7 mm can be lumped capacitors, and greater than 7 mm should be treated as transmission lines.

The 10/100/1000BASE-T signals are routed from the PHY devices to the (possibly integrated) magnetics as four 100 Ω differential pairs for each port. It is important to keep these signals away from noise sources, as all differential (and some common- mode) noise coupled to these signals will find its way out to the unshielded twisted pair wires and radiate, with possible EMI problems as a result. It is also very important to keep the two traces that make up a differential pair exactly the same length, as any difference in length will result in differential-to-common mode conversion of the signal and this will radiate out on the UTP cables.

9.2 Using PHYs in Backplane Applications

It is possible to use the VSC8512 in applications where the VSC8512 copper interface is connected to another VSC8512's copper interface.

There are two options for connecting the VSC8512 to other Vitesse PHYs.

1. Capacitors should be used when connecting Vitesse PHYs to other Vitesse PHYs at a minimum . For this configuration 0.1 µf capacitors are recommend or 47 nf for best connection. This design should be tested for common mode compliance and BERR and EMI for longer connections.
2. The best option is to use a 1:1 transformer with no common mode chokes. A 0.1 µf capacitor should be connected from both the primary and secondary mid points to ground.

When connecting Vitesse PHYs (Voltage mode) to other PHYs (Current Mode) a 1:1 transformer must be used. The Vitesse PHY side must have a 0.1 µf capacitor at the midpoint connected to ground. The magnetics used for the other PHY must meet the other PHY vendor's requirements.

9.3 Surge Protection

Surge protection can be added to the CAT5 interface with care to not add devices with "too" much capacitance that might cause the path to fail or not pass the IEEE test suite. The unique board design aspects influence how much capacitance can be tolerated on each design. It is difficult to precisely quantify device parameters influenced by board design. Therefore, the designer should plan in the prototyping phase to assess and make adjustments in surge protection based on CAT5 behavior.

Pay close attention to the capacitance of the surge device. If the design has satisfactory magnetics parameters and passes IEEE testing, then up to 5 pf of capacitance should be fine. If the board uses "best" magnetics and passes IEEE testing with a wide margin, then up to 15 pf should be fine. See section 4for determining magnetics parameter requirements.

9.4 PHY Miscellaneous

The twisted pair interfaces on the copper PHY interfaces are fully compliant with the IEEE802.3-2005 specification for CAT-5 media. The Vitesse PHYs, unlike other traditional Gigabit PHYs, integrate all passive components required to connect the PHY's CAT-5 interface to an external 1:1 transformer and common mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The ports support auto-negotiation and can automatically detect the speed and duplex mode of a link and provide the appropriate connection in 10BASE-T half-duplex, 10BASE-T full duplex, 100BASE-T half-duplex, 100BASE-T full duplex or 1000BASE-T full duplex.

The ports include Automatic Crossover Detection functionality for all three speeds (HP Auto MDI/MDI-X function). They also include the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled, but can be disabled.

The ports support the IEEE standard range of 1 m to 100 m twisted pair cable.

1000BASE-T mode requires Category 5 enhanced cable in accordance to the cabling specifications defined by IEEE802.3-2005.

100BASE-TX mode requires Category 5.

10 MAC Interfaces

This section describes the MAC interfaces of the VSC8512.

10.1 QSGMII Interface

QSGMII multiplexes four SGMII interfaces together. Note the VSC8512 datasheet DC and AC QSGMII requirements.

QSGMII are LVDS compatible. Interfaces can be directly connected if they have compatible DC specifications; otherwise AC coupling capacitors must be used.

When implementing 5 Gbit/s QSGMII signals in a PCB layout, it is important to observe the following standard high-speed PCB layout techniques.

- PCB traces must be designed as 100 Ω differential pairs. Keep vias to a minimum, avoid stubs, and avoid routing QSGMII signals over plane splits.
- PCB traces must be as short (to minimize loss) and wide (to increase manufacturability of tightly impedance controlled 100 Ω traces, for example, 8 mil traces preferred over 4 mil traces) as possible.
- If possible, route receiver pairs on a different PCB layer than transmitter pairs in order to decrease crosstalk.
- Where possible add shield ground between the individual QSGMII lanes in order to decrease crosstalk. Stitch the shield ground “traces” to the internal ground plane. For example, every 17cm /ns /5 Ghz /6 = 5mm (at this frequency every trace, including a ground trace, easily becomes an antenna).

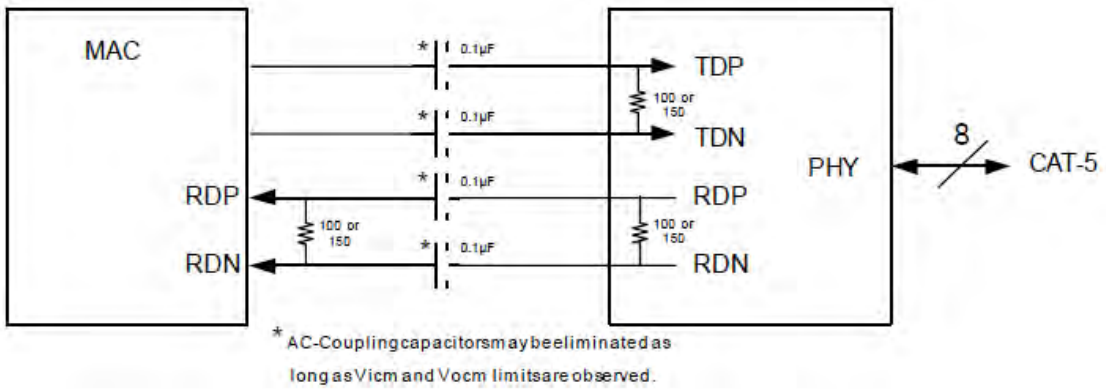
Post-layout board simulation using the Vitesse-supplied IBIS models is highly recommended.

10.2 SGMII/SerDes Interface

Key to the MAC interface is making sure the MAC and PHY connections DC and AC parameters will match. Often the DC parameters do not match well, creating the need for AC-coupling capacitors.

The following figure illustrates typical MAC-to-PHY serial interface of the VSC8512.

Figure 8 • Typical MAC-to-PHY Serial Interface



10.3 Design Rules

Best performance is acheived when SerDes traces are placed using the following design rules.

- Traces should be routed as 50 Ω (100 Ω differential) controlled impedance transmission lines (microstrip, or stripline).
- Traces should be of equal length on each differential pair and port to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Traces should avoid vias and layer changes.
- For applications not requiring a specific port's SGMII interface pins, these pins should be left floating (no-connects)

10.4 AC Coupling Capacitors

In general SerDes interfaces require series AC coupling capacitors to prevent common mode voltages from interfering with transmit and receive operation. If the common mode input and output specifications for the MAC and VSC8512 are compatible then the AC capacitors can be removed. Note that the VSC8512 has integrated AC coupling capacitors on the receive paths of the SerDes MAC and media interfaces. For more information, see the VSC8512 datasheet.

10.5 SerDes Media

The VSC8512 has an additional SerDes interface to support SerDes Media such as 1000BASE-X fiber, 100BASE-FX fiber, or 10/100/1000BASE-T copper SFPs. For more design implementation information, see the Vitesse Dual Copper/Fiber/SFP Guide. Section 10.3 of this document will apply to this interface.

10.5.1 Unidirectional for Streaming

This support is applicable to applications with no valid link in which only the receive or transmit side of a fiber connection is present, such as in a single direction streaming application. The Unidirectional feature can be used to defeat the link requirements of the PHY. The MAC interface in this mode also supports a single direction connection. No special hardware configuration is required. See the VSC8512 datasheet for further discussion.

11 Miscellaneous Design Considerations

This section describes the miscellaneous design considerations of the VSC8512.

11.1 SMI (MDC/MDIO) Device Address

The VSC8512 includes two external PHY address pins to allow control of multiple PHY devices on a system board that are sharing a common management bus. Based on the settings of these two address control pins, the internal PHYs in the VSC8512 take on the address ranges as shown in the following table.

Table 3 • PHY Address Range Selection

PHYADDR4	PHYADDR3	Internal PHY Addresses
0	0	0–11
0	1	12–23
1	0	4–15
1	1	20–31

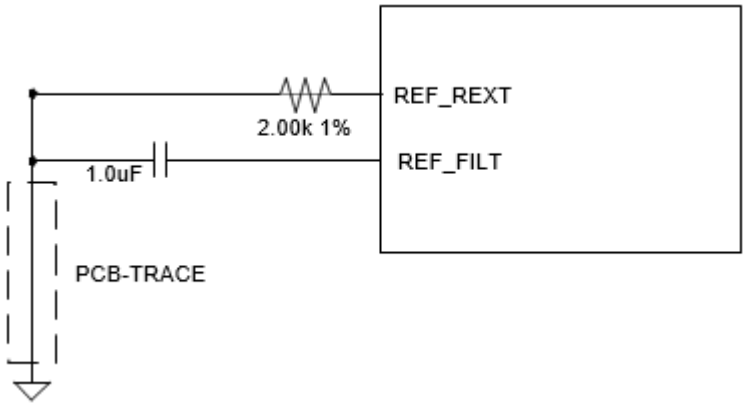
11.2 REF_FILT / REF_REXT Pins

For proper operation, the VSC8512 must generate an on-chip band-gap reference voltage at the REF_FILT pin. A REF_FILT and REF_REXT are required for each group of four PHYs in the VSC8512. Thus, a total of three sets of REF_REXT and REF_FILT pins are found on the VSC8512. The following components are required for each set of these pins in the VSC8512 system.

- 2.0 kΩ resistor, 1% tolerance, minimum 1/16 W
- 1 µF capacitor, 10% tolerance; NPO, X7R or X5R ceramic materials are all acceptable

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops that would cause inaccuracy of the reference voltage. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace, rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8512. See the following figure.

Figure 9 • Voltage Reference Schematic



11.3 Device Clock Input

The VSC8512 supports an input clock from an oscillator to the REFCLK pin only. No crystal support is available.

There are three selection pins to support a variety of input clocks. See the VSC8512 data sheet for further discussion and pin location.

The following table lists the REFCLK frequency selection.

Table 4 • REFCLK Frequency Selection

REFCLK_SEL[2]	REFCLK_SEL[1]	REFCLK_SEL[0]	REFCLK Frequency
0	0	0	125 MHz
0	0	1	156.25 MHz
0	1	0	250 MHz
0	1	1	312.25 MHz
1	0	0	25 MHz

When using QSGMII and single-ended or 25 MHz for the REFCLK input, care should be taken to make sure the input clock jitter is within tolerance.

REFCLK must be available before releasing NRESET.

11.3.1 Clock Power Supply Filtering

In oscillators with a VCC pin, in order to prevent power supply switching noise from coupling into the PHY, it is recommended that an RC filter be implemented. The RC circuit values should be set to filter out the supply's switching regulation frequency. For example, for a supply with a switching frequency of 350 kHz, use an R value = 2.2 Ω and a C value = 11 µF.

11.4 COMA_MODE

When NRESET is released, the PHYs and registers in the VSC8512 can go to their default states and begin operation, or the PHYs can be disabled by the state of the COMA_MODE pin so that behaviors can be programmed into registers before releasing the PHYs to operate. Typically this pin will be driven by a system GPIO controlled by the host microcontroller.

It is recommended that COMA_MODE have a 2k pull-up resistor.

If multiple devices supporting COMA_MODE are in a system, then consider connecting all COMA_MODE pins together. This starts them at the same time and can affect LED flashing synchronization.

11.5 CLKOUT Pin

The VSC8512 provides a selectable 125 MHz or 156.25 MHz clock out reference. The purpose of this pin is to drive MAC logic that requires an additional 125 MHz or 156.25 MHZ clock source. The clock is active only if the NRESET pin is de-asserted. If not used, then set this pin to be disabled (MII Register 18.0 = 1) to avoid potential EMI issues associated with having an un-terminated output driver.

This clock pin is also derived from the internal PLL of the VSC8512 and therefore is not recommended for use in clocking other devices that have internal PLLs.

11.6 Serial Management Interface (SMI)

The VSC8512 uses MDC and MDIO pins as a management interface as defined by the IEEE 802.3 standard.

The MDIO pin is an open-drain signal and requires an external pull-up resistor. Only a single pull-up resistor is needed for the system, regardless of the number of devices. The pull-up resistor for the MDIO pin must be chosen to match the characteristics of the system. Of critical importance is the rise time needed to charge the total capacitive load on the MDIO pin up to a logic '1' through the pull-up resistor. This time constant is defined simply as the following.

$\tau = R_{pu}C_{total}$

Therefore, as more devices are added to the bus, the rise time increases due to the increased bus capacitance. In order to lower the rise time, a smaller resistor value must be used. However, if too small a value is used, devices will be unable to transition the bus to logic '0'. This occurs when the current sinking capability of the pins in a logic '0' state is exceeded. For the VSC8512, the MDIO input capacitance is approximately 5 pF, and the maximum current sinking capacity is 10 mA.

Following are the typical values.

- For MDC frequencies of 2.5 MHz and below, a 2 kΩ pull-up resistor should be acceptable for most applications. This assumes the input capacitance of each device is between 5-10 pF and that each device can sink at least 1.65 mA of current from each of their MDIO pins.
- For faster MDC frequencies (> 2.5 MHz), a smaller pull-up is necessary. The smallest recommended pull-up resistor for use with the VSC8512 is 470 Ω.

11.7 JTAG (Boundary Scan) Design

The following section describes the JTAG (boundary scan) design.

11.7.1 JTAG Interface "Never" Used

If JTAG is never going to be used, all that is needed is to assert the TRST pin low. This can be done with a 2K pull-down resistor. The rest of the four other JTAG pins can be left floating.

11.7.2 JTAG Interface Used In Board Design

For designs that plan to use the JTAG interface for boundary scan testing, there are some design considerations to take into account.

Boundary scan controllers traditionally provide all five pins to control the JTAG chain designed on a board. It should be noted that the PHY datasheet was written based on five-pin boundary scan chains. Even though all five pins are to be connected, the user must still actively assert the TRST pin on the PHY if JTAG is to be used. The JTAG specification 1149.1 states that the TRST pin is optional, but only in the sense that it is an optional circuit from the perspective of the silicon chip design. To reset the TAP controller inside the chip, the chip has to either provide a TRST pin or an internal power-up reset circuit. Since the PHY provides a TRST pin, there is not an internal power-up reset circuit. Another way to reset the TAP controller is by clocking in 5 ones using the TCK (clock) and the TMS (held high). However, tying the TRST pin low guarantees that, when you power your system up, the PHY will come up in a "normal" operating state. If it is held high all the time, there will be no guarantee that the PHY will be operating in a "normal" state after power-up. If the TRST pin is held low all of the time, JTAG can never be used. To get around that, TRST can be held low for a period after power-up (100 ns with stable power supplies would be fine) and then left high. This can be implemented in several different ways, including jumpers, power-on reset circuits, etc.

For the case of a four-pin boundary scan controller, it should be noted that there is text in the datasheet that implies that TRST can be floated. When connecting a four- pin boundary scan controller to a five-pin JTAG interface, a design must still provide a way to actively assert the TRST pin after each power-up. See the previous paragraph for an explanation of ways in which this might be accomplished.

11.7.3 AC-JTAG

IEEE 1149.6 format BSDL is supported and provided.

11.8 LEDs

This section describes the LEDs of the VSC8512.

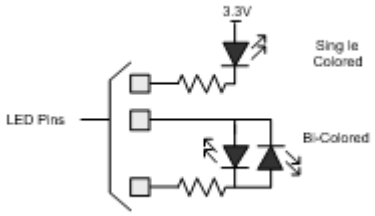
11.8.1 Dual LED per Port Option

Each VSC8512 PHY port can support two single-colored LEDs or one tri-colored LED, per port. Each LED pin sinks current when an indication is present and de-asserts when inactive. By design, each LED pin can also drive current when not active. This is very useful in the case of bi-colored LEDs. Each LED pin in the VSC8512 can be designated to indicate any of the possible LED status signals thereby further simplifying the overall design.

Each LED can sink or source 8 ma. The LED is required to have a series resistor in the range of 100 Ω–300 Ω. The diode drop is assumed to be 0.7 V.

The following figure illustrates the LED Configurations.

Figure 10 • LED Configurations



11.8.2 Serial LED Option

See the VSC8512 datasheet LED Interface discussion in the Feature Description section and register 25G for control options.

11.8.3 Adjustable Brightness LED

See the register 25G bits 15:8 in the VSC8512 datasheet for details.

11.9 GPIO and Multi Mode Pins

GPIO pins on the VSC8512 are provided to allow a user to eliminate unnecessary glue- logic for lower speed external control and status pins of support devices such as Power over Ethernet Controllers and SFPs. In addition, unused LED pins can be used as general-purpose outputs as well.

11.9.1 Fast Link Failure

For the quickest notification of loss of link, use the FastLink failure pins of the VSC8512. IEEE 802.3 permits up to 750 ms before signaling 1000BASE-T loss of link. Fast Link Failure will indicate loss of link in less than 1 ms.

11.10 CMODE Interface

The CMODE Interface is not supported on the VSC8512.

11.11 SyncE Support

The VSC8512 supports SyncE operation by way of providing the recovered clock from the media interfaces. See datasheet section 3.11 on Media Recovered Clock Outputs for details.

11.12 Controlling SFPs and Talking to I2C Devices

See the VSC8512 datasheet for more details about use of the built-in I²C multiplexer.

11.13 Unused PHY Ports

- Terminate CAT5 differential pair with 100 Ω impedance
- Leave SGMII disconnected
- Power down PHY port, set Register 0.11 = 1

12 Software Considerations

This section describes the software considerations of the VSC8512.

12.1 Resources

- Feature discussion and register description in VSC8512 datasheet
- PHY_API
- VSC8512 Errata document

12.2 Configuration

12.3 Minimum Register Configuration

The following describes the minimum register settings that are needed to configure the PHY to normal operation. This assumes changes that are made from the default settings that are set during reset. Also, to decrease the configuration time period, the broadcast write bit (MII Register 22.0) can be set which allows writing to all PHYs from one location. This can be the first register bit set.

1. If MAC interface configuration changes are needed such as disabling SGMII auto-negotiation, the first register writes should be to Register 23.
2. If the MAC interface settings in Register 23 are changed, then the next step is to perform a Software Reset (MII Register 0.15 = 1).
3. After the reset completes, any required initialization scripts from the Errata document are to be written at this time.
4. At this step, other user-defined configuration settings can be applied such as LED changes.

12.4 Power Management Software Features

12.4.1 EEE

12.4.2 ActiPHY

12.4.3 PerfectReach

12.4.4 LED Pulse Width Modulation

12.4.5 Turning a Port Off

12.4.6 PICMG 2.16

12.5 Advanced Software Features

12.5.1 Interrupts

13 Debugging Your Prototype

This section describes debugging the prototype.

13.1 PHY Bring-up, Testing Steps and Options

The following steps can be followed to debug a new design prototype.

1. Exit reset. Check:
   - Power supply level and ripple
   - Clock for proper frequency and jitter within tolerance
   - Board components
   - CAT5 pin levels
2. Read and Write MDC/MDIO Registers
3. JTAG control of registers
4. Check out interfaces with loop backs.
   - Testing CAT5—Far End Loop Back
   - Testing Fiber—SerDes Loop backsTesting MAC – Near End Loop back
   - Ethernet Packet Generator
   - Use Interrupt status register to identify issue
   - CRC and other error counters

13.2 Reset Sequence

The following events occur in the order listed when the VSC8512 is brought out of reset. This is triggered by a low-to-high transition of the NRESET pin.

1. Several milliseconds after reset, the analog reference voltages and current stabilize. This is seen on the REF_REXT and REF_FILT pins.
2. Once a stable analog reference is established, the internal PLL will require 50 microseconds to lock. The PLL provides the device its internal clocks.
3. With a locked PLL, the analog-to-digital blocks are calibrated. This usually requires approximately two ms.
4. Once the ADC is calibrated, the CLKOUT pin is activated.
5. The device is now in normal operation and its MDC and MDIO pins are operational.
6. Read device ID registers 3 and 4. Read and write register 25.

Important Note: It is required that the power supply is stable before the rising edge of nRESET. Therefore, if nRESET is tied directly to logic high on the PCB, the VSC8512 will behave unpredictably. If a design requires the NRESET pin to remain high at all times, a small RC circuit can be added to this line to provide the necessary delay.

nRESET (active low) must be de-asserted no less than 20 ms after the power supplies and the reference clock are valid. For this reason a POR/delay circuit must be used on the nRESET pin. The MAX811 can be used to provide the POR.

Note: There are no power sequencing requirements for the VSC8512.

13.3 Using Loopbacks to Divide Problems

- MAC to PHY side testing use Near End Loop Back
- Media to PHY side testing use Far End Loop Back

13.4 Diagnostic Features

See Feature discussion in VSC8512 datasheet for the following other testing features.

- Ethernet Packet Generator

- CRC Counters
- 100FX Halt code testing

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

VPPD-01611