dsPIC33FJ32MC202 to dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 Migration Guide

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INTRODUCTION

This section provides an overview of considerations for migrating from the dsPIC33FJ32MC202 motor control device to the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 families of motor control devices.

If you are undertaking this migration, it is recommended that you download the data sheets (see the Note) and errata documents for these devices from the Microchip web site (www.microchip.com).

The code developed for dsPIC33FJ32MC202 devices can be ported to dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices after making the appropriate changes outlined in this document.

Note: The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices have been designed to perform to the parameters specified in either the *"dsPIC33FJ16MC101/102 Data Sheet"* (DS70652) or the *"PIC24FJ16MC101/102 Data Sheet"* (DS39997), and have been tested to electrical specifications designed to determine their conformance with these parameters.

Due to manufacturing process differences, these devices may have different performance characteristics than their earlier versions. These differences may cause these devices to perform differently in your application than their earlier versions. For example, the user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or oscillator mode may be required.

MIGRATION CONSIDERATIONS SUMMARY

This migration guide discusses enhancements, changes, and application considerations when migrating from the dsPIC33FJ32MC202 device to the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 families of devices.

Some key migration considerations of the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are:

- Lower speed: 16 MIPS versus 40 MIPS
- Three additional Comparators
- Smaller Flash memory
- Less RAM: 1K versus 2K
- No 12-bit ADC module
- No voltage reference (VREF) inputs
- No QEI module
- One less IC
- Additional CTMU and RTCC modules
- High-accuracy LPRC and FRC oscillators
- No PWM pin state configuration initialization
- Simple security
- 4x Phase-Locked Loop (PLL) only

PACKAGE MIGRATION CONSIDERATIONS

The key differences in the functionality of the pins for the 28-pin SPDIP, SOIC and SSOP packages, are listed in Table 1.

- VREF+ and VREF- pins are only available in the dsPIC33FJ32MC202 device
- PGED2 and PGEC2 pins 21 and 22 in the dsPIC33FJ32MC202 device are located on pins 2 and 3 in the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- PGED3 and PGEC3 pins 14 and 15 in the dsPIC33FJ32MC202 device are located on pins 11 and 12 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- JTAG pins TCK, TDO, TDI and TMS are multiplexed on pins 17, 18, 21, 22 and are not available in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- PWM2H1/PWM2L1 pins are not present in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, as PWM Generator 2 is not available in these devices
- Comparator inputs A, B, C, and D are located on pins 2, 3, 4, 5, 6, and 7 in the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no comparators.
- CTMU External Edge Input 1 and 2 are multiplexed with pins 2 and 3 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no CTMU.
- CTMU Timing Comparator Input is multiplexed with pin 4 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no CTMU.
- CVREFIN Comparator Voltage Positive Reference Input is multiplexed on pin 5 along with CVREFOUT in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 has no comparator.
- Fault input pins $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ are fixed on pins 14 and 15 on dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. Fault pins are remappable in the dsPIC33FJ32MC202 device.
- SPI pins SCK1, SDO1, SDI1 are multiplexed on pins 16, 17, and 18 on dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. SPI pins are remappable in the dsPIC33FJ32MC202 device.
- RTCC output is multiplexed on pin 25 on dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no RTCC.

TABLE 1: 28-PIN SPDIP, SOIC, AND SSOP DEVICE DIFFERENCES

Pin #	dsPIC33FJ32MC202 28-pin SPDIP, SOIC, SSOP	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 28-pin SPDIP, SOIC, SSOP
1	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$
2	AN0/**VREF+**/CN2/RA0	**PGED2**/AN0/**C3INB/C1INA/CTED1**/CN2/RA0
3	AN1/**VREF-**/CN3/RA1	**PGEC2**/AN1/**C3INA/C1INB/CTED2**/CN3/RA1
4	PGED1/AN2/C2IN-/RP0/CN4/RB0	PGED1/AN2/**C2INA**/**C1INC**/RP0/CN4/RB0
5	PGEC1/AN3/C2IN+/RP1/CN5/RB1	PGEC1/AN3/**CVREFIN/CVREFOUT/C2INB/C1IND**/RP1/CN5/RB1
6	AN4/RP2/CN6/RB2	AN4/**C3INC/C2INC**/RP2/CN6/RB2
7	AN5/RP3/CN7/RB3	AN5/**C3IND/C2IND**/RP3/CN7/RB3
8	VSS	VSS
9	OSC1/CLKI/CN30/RA2	OSCI/CLKI/CN30/RA2
10	OSC2/CLKO/CN29/RA3	OSCO/CLKO/CN29/RA3
11	SOSCI/RP4/CN1/RB4	**PGED3**/SOSCI/RP4/CN1/RB4
12	SOSCO/T1CK/CN0/RA4	**PGEC3**/SOSCO/T1CK/CN0/RA4
13	VDD	VDD
14	**PGED3**/ASDA1/RP5/CN27/RB5	**$\overline{\text{FLTB1}}$/**ASDA1/RP5/CN27/RB5
15	**PGEC3**/ASCL1/RP6/CN24/RB6	**$\overline{\text{FLTA1}}$/**ASCL1/RP6/CN24/RB6
16	INT0/RP7/CN23/RB7	**SCK1**/INT0/RP7/CN23/RB7
17	**TCK/PWM2H1**/SCL1/RP8/CN22/RB8	SCL1/**SDO1**/RP8/CN22/RB8
18	**TDO/PWM2L1**/SDA1/RP9/CN21/RB9	SDA1/**SDI1**/RP9/CN21/RB9
19	VSS	VSS
20	VCAP	VCAP
21	**PGED2/TDI**/PWM1H3/RP10/CN16/RB10	PWM1H3/RP10/CN16/RB10
22	**PGEC2/TMS**/PWM1L3/RP11/CN15/RB11	PWM1L3/RP11/CN15/RB11
23	PWM1H2/RP12/CN14/RB12	PWM1H2/RP12/CN14/RB12
24	PWM1L2/RP13/CN13/RB13	PWM1L2/RP13/CN13/RB13
25	PWM1H1/RP14/CN12/RB14	PWM1H1/**RTCC**/RP14/CN12/RB14
26	PWM1L1/RP15/CN11/RB15	PWM1L1/RP15/CN11/RB15
27	AVSS	AVSS
28	AVDD	AVDD

Legend: Pin names shown in **Bold** type denote the key differences between the two device families.

The key differences in the functionality of the pins for the 28-pin QFN package, are also listed in Table 2.

- PGED1/EMUD1 and PGEC1/EMUC1 are multiplexed on pins 1 and 2 in the dsPIC33FJ32MC202 device
- PGED2/EMUD2 and PGEC2/EMUC2 are multiplexed on pins 18 and 19 on PWM2H1/PWM2L1; PGED2 and PGEC2 are multiplexed on pins 27 and 28 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- PGED3/EMUD3 and PGEC3/EMUC3 are multiplexed on pins 11 and 12 on the dsPIC33FJ32MC202 device and are located on pins 8 and 9 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- JTAG pins TCK, TDO, TDI, and TMS are multiplexed on pins 14, 15, 18, and 19, respectively in dsPIC33FJ32MC202 and are not available in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- PWM Generator 2 PWM2H1/PWM2L1 output pins are multiplexed on pins 14 and 15 in the dsPIC33FJ32MC202 device and are not available in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- VREF+ and VREF- pins are multiplexed on pins 27 and 28 in the dsPIC33FJ32MC202 device and are not available in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- Comparator inputs A, B, C, and D are located on pins 1, 2, 3, 4, 27, and 2 of the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no comparators.
- CVREFIN Comparator Voltage Positive Reference Input is multiplexed on pin 2 along with CVREFOUT in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices
- Fault input pins $\overline{\text{FLTA1}}$ and $\overline{\text{FLTB1}}$ are fixed on pins 11 and 12 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. Faults are remappable in the dsPIC33FJ32MC202 device.
- SPI pins SCK1, SDO1, and SDI1 are multiplexed on pins 13, 14, and 15 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. SPI pins are remappable in the dsPIC33FJ32MC202 device.
- RTCC output is multiplexed on pin 22 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no RTCC.
- CTMU External Edge Input 1 and 2 are multiplexed with pins 27 and 28 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no CTMU.
- CTMU Timing Comparator Input is multiplexed with pin 1 in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The dsPIC33FJ32MC202 device has no CTMU.

TABLE 2: 28-PIN QFN DEVICE DIFFERENCES

Pin #	dsPIC33FJ32MC202 (28-pin QFN)	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 (28-pin QFN)
1	PGED1/**EMUD1**/AN2/C2IN-/RP0/CN4/RB0	PGED1/AN2/**C2INA/C1INC**/RP0/CN4/RB0
2	PGEC1/**EMUC1**/AN3/C2IN+/RP1/CN5/RB1	PGEC1/AN3/**CVREFIN/CVREFOUT/C2INB/C1IND**/RP1/CN5/RB1
3	AN4/RP2/CN6/RB2	AN4/**C3INC/C2INC**/RP2/CN6/RB2
4	AN5/RP3/CN7/RB3	AN5/**C3IND/C2IND**/RP3/CN7/RB3
5	VSS	VSS
6	OSC1/CLKI/CN30/RA2	OSCI/CLKI/CN30/RA2
7	OSC2/CLKO/CN29/RA3	OSCO/CLKO/CN29/RA3
8	SOSCI/RP4/CN1/RB4	**PGED3**/SOSCI/RP4/CN1/RB4
9	SOSCO/T1CK/CN0/RA4	**PGEC3**/SOSCO/T1CK/CN0/RA4
10	VDD	VDD
11	**PGED3/EMUD3**/ASDA1/RP5/CN27/RB5	**$\overline{\text{FLTB1}}$**/ASDA1/RP5/CN27/RB5
12	**PGEC3/EMUC3**/ASCL1/RP6/CN24/RB6	**$\overline{\text{FLTA1}}$**/ASCL1/RP6/CN24/RB6
13	INT0/RP7/CN23/RB7	**SCK1**/INT0/RP7/CN23/RB7
14	**TCK/PWM2H1**/SCL1/RP8/CN22/RB8	SCL1/**SDO1**/RP8/CN22/RB8
15	**TDO/PWM2L1**/SDA1/RP9/CN21/RB9	SDA1/**SDI1**/RP9/CN21/RB9
16	VSS	VSS
17	VCAP	VCAP
18	**PGED2/EMUD2/TDI**/PWM1H3/RP10/CN16/RB10	PWM1H3/RP10/CN16/RB10
19	**PGEC2/EMUC2/TMS**/PWM1L3/RP11/CN15/RB11	PWM1L3/RP11/CN15/RB11
20	PWM1H2/RP12/CN14/RB12	PWM1H2/RP12/CN14/RB12
21	PWM1L2/RP13/CN13/RB13	PWM1L2/RP13/CN13/RB13
22	PWM1H1/RP14/CN12/RB14	PWM1H1/**RTCC**/RP14/CN12/RB14
23	PWM1L1/RP15/CN11/RB15	PWM1L1/RP15/CN11/RB15
24	AVSS	AVSS
25	AVDD	AVDD
26	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$
27	AN0/**VREF+**/CN2/RA0	**PGED2**/AN0/**C3INB/C1INA/CTED1**/CN2/RA0
28	AN1/**VREF-**/CN3/RA1	**PGEC2**/AN1/**C3INA/C1INB/CTED2**/CN3/RA1

Legend: Pin names shown in **Bold** type denote the key differences between the two device families.

SYSTEM CONSIDERATIONS

While the dsPIC33FJ32MC202 components are only available as a dsPIC® Digital Signal Controller (DSC), the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are available either as dsPIC DSCs or as PIC24F Microcontrollers (MCUs).

The main difference between the two families is that the PIC24F devices contain no Digital Signal Processing (DSP) core.

These processors are a perfect fit for applications where the particular control algorithm used does not consume a lot of resources. This is the case of many low-cost motor control applications.

The supply voltage range for the dsPIC33FJ32MC202 device is 3.0V to 3.6V. The voltage range for the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 is from 3.0V to 3.6V.

Table 3 summarizes the main system differences between the device families.

TABLE 3: SYSTEM DIFFERENCES

Feature	dsPIC33FJ32MC202	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102
Operating Voltage	3.0V-3.6V (-40ºC to +85ºC)	3.0V-3.6V (-40ºC to +85ºC)
	3.0V-3.6V (-40ºC to +125ºC)	3.0V-3.6V (-40ºC to +125ºC)
Maximum Speed	40 MIPS	16 MIPS
Flash	32K	16K
RAM	2K	1K
Pins	28 and 44	18(1), 20, 28, and 36
Packages	28-pin SPDIP, SOIC, SSOP, and QFN-S 44-pin QFN and TQFP	18-pin PDIP and SOIC(1) 20-pin SPDIP, SOIC, and SSOP 28-pin SPDIP, SOIC, SSOP, and QFN 36-pin TLA
Watchdog Timer	Yes	Yes
Power-on Reset (POR)	Yes	Yes
Brown-out Reset (BOR)	Yes	Yes

Note 1: dsPIC33FJ16MC101 devices only.

CPU ARCHITECTURE AND INSTRUCTION SET

The processor core of the dsPIC33FJ32MC202 device is the same as the processor core for the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. Therefore, no differences need to be considered.

FLASH MEMORY

The dsPIC33FJ32MC202 device features 32 Kbytes of Flash memory, while the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices feature 16 Kbytes of Flash memory.

RTSP PROGRAMMING

The Flash program memory array for the dsPIC33FJ32MC202 device and the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time.

The key difference is that while for the dsPIC33FJ32MC202 device, it is possible to program one row or one word at a time, for dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, it is only possible to program one word at a time.

For the dsPIC33FJ32MC202 device, the 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively. The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary. In case of the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, the 8-row erase pages are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes.

Table 4 summarizes the write and erase time differences.

As a consequence of the different way the Flash memory is managed, the NVMOP register control bits are slightly different. Table 5 summarizes these differences.

TABLE 4: WRITE AND ERASE TIME DIFFERENCES (AT 100ºC)

Parameter	dsPIC33FJ32MC202	dsPIC33FJ16MC102
Word write time	55.9 µs maximum	48.8 µs maximum
Row write time	1.79 ms maximum	—
Page erase time	26.5 ms maximum	26.5 ms maximum

TABLE 5: NVMOP BIT SETTING DIFFERENCES

dsPIC33FJ32MC202	dsPIC33FJ16MC102
NVMOP<3:0> Setting If ERASE = 1: 1111 = Memory bulk erase operation 1101 = Erase General Segment 1100 = Erase Secure Segment 0011 = No operation 0010 = Memory page erase operation 0001 = No operation 0000 = Erase a single Configuration register byte If ERASE = 0: 1111 = No operation 1101 = No operation 1100 = No operation 0011 = Memory word program operation 0010 = No operation 0001 = Memory row program operation 0000 = Program a single Configuration register byte	**NVMOP<3:0> Setting** If ERASE = 1: 1111 = No operation 1101 = Erase General Segment 1100 = No operation 0011 = No operation 0010 = Memory page erase operation 0001 = No operation 0000 = No operation If ERASE = 0: 1111 = No operation 1101 = No operation 1100 = No operation 0011 = Memory word program operation 0010 = No operation 0001 = No operation 0000 = No operation

DATA MEMORY

The dsPIC33FJ32MC202 device features 2 Kbytes of RAM data memory, while the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices feature 1 Kbyte of RAM data memory.

POWER-UP TIMER

In the dsPIC33FJ32MC202 device, the power-up timer has a programmable interval from 2 ms to 128 ms, with seven steps. The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices have a fixed power-up timer interval of 64 ms. Table 6 summarizes the performances and also shows the PWRT bit values in the Configuration register, FPOR.

TABLE 6: POWER-UP TIMER DIFFERENCES

dsPIC33FJ32MC202/204	dsPIC33FJ16MC101/102 PIC24FJ16MC101/102
Power-on Reset (POR) Timer Value	
111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled	64 ms fixed

OSCILLATOR CONFIGURATION

A relevant difference between the dsPIC33FJ32MC202 device and the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices is the maximum operating speed.

The dsPIC33FJ32MC202 device can reach 40 MIPS, while the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices operate at a maximum speed of 16 MIPS, which in most cases, is more than enough to run motor control algorithms. Migrating from one family to the other will require a new computation of the Oscillator and Phase-Locked Loop (PLL) parameters. Table 7 summarized the main differences between the clock sources.

PHASE-LOCKED LOOP (PLL)

In the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, the PLL, when enabled, has a fixed multiplying factor of four. The dsPIC33FJ32MC202 PLL factor can be varied, as shown in Equation 1.

EQUATION 1:

$$FOSC = \left(\frac{M}{(N1 \times N2)}\right)$$

where:
M is the PLLDIV value
*N*1 is the PLLPRE value
*N*2 is the PLLPOST value

TABLE 7: OSCILLATOR DIFFERENCES

Feature	dsPIC33FJ32MC202	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102
Internal High-Speed Oscillator	7.37 MHz ±2% (-40ºC ≤T ≤+85ºC) 7.37 MHz ±5% (-40ºC ≤T ≤+125ºC)	7.37 MHz ±1.5% (-40ºC ≤T ≤+85ºC) 7.37 MHz ±2% (-40ºC ≤T ≤+125ºC)
Internal Low-Speed Oscillator	32,768 ±15% (-15ºC ≤T ≤+85ºC) 32,768 ±40% (-40ºC ≤T ≤+125ºC)	32,768 ±20% (-40ºC ≤T ≤+85ºC) 32,768 ±30% (-40ºC ≤T ≤+125ºC)
PLL	Variable Gain PLL	4x Fixed PLL
Clock Monitor	Yes	Yes

FRC AND LPRC ACCURACY

The FRC for the dsPIC33FJ32MC202 device and the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices has a frequency of 7.37 MHz.

The accuracy of the FRC and LPRC on dsPIC33FJ16MC101/102 and PIC24FJ16MC101/102 devices has been improved (see Table 7).

All families of devices have an internal low frequency oscillator running at 32.768 kHz.

INTERRUPTS

There is no difference in external interrupts between all families of devices.

I/O PORTS

Table 8 summarizes the available remappable input pins.

TABLE 8:

Input Name	Function Name	Register Name	dsPIC33FJ32MC202	dsPIC33FJ16MC101/102 PIC24FJ16MC101/102
External Interrupt 1	INT1	RPINR0	Yes	Yes
External Interrupt 2	INT2	RPINR1	Yes	Yes
Timer2 External Clock	T2CK	RPINR3	Yes	Yes
Timer3 External Clock	T3CK	RPINR3	Yes	Yes
Input Capture 1	IC1	RPINR0	Yes	Yes
Input Capture 2	IC2	RPINR7	Yes	Yes
Input Capture 3	IC3	RPINR7	No	Yes
Input Capture 7	IC7	RPINR10	Yes	No
Input Capture 8	IC8	RPINR10	Yes	No
Output Compare Fault	OCFA	RPINR11	Yes	Yes
PWM1 Fault	FLTA1R	RPINR12	Yes	No
PWM2 Fault	FLTA2R	RPINR13	Yes	No
QEI1 Phase QEA	QEA	RPINR14	Yes	No
QEI1 Phase B QEB	QEB	RPINR14	Yes	No
QEI1 Index INDX	INDX	RPINR15	Yes	No
UART1 Receive	U1RX	RPINR18	Yes	Yes
UART1 Clear To Send	$\overline{\text{U1CTS}}$	RPINR18	Yes	Yes
SPI1 Data Input	SDI1	RPINR20	Yes	No
SPI1 Clock Input	SCK1	RPINR20	Yes	No
SPI1 Slave Select Input	$\overline{\text{SS1}}$	RPINR21	Yes	Yes

TIMERS

All devices are equipped with the same number of timers, of which there are two distinct types: Timer1 and Timer2/3.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter.

The Timer2/3 feature allows the timers to also be configured as a 32-bit timer with selectable operating modes.

INPUT CAPTURE

All devices implement the same Input Capture module; however, the dsPIC33FJ32MC202 device is equipped with four, while the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices have three.

OUTPUT COMPARE

No differences.

PWM MODULE

The difference in maximum speed of all devices is also reflected in different maximum frequencies for the PWM generators. Table 9 provides a list of the differences between devices.

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices have six outputs with a single time base, whereas the dsPIC33FJ32MC202 device has one time base with up to six outputs and another time base with two outputs.

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices implement a write protection safety feature, which is implemented for the PWMxCON1, PxFLTACON and PxFLTBCON registers. The write protection feature prevents inadvertent writes to these registers and can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>) in the FOSCSEL Configuration register. The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK = 0.

The user application can gain access to these locked registers either by configuring PWMLOCK = 0, or by performing the unlock sequence. To perform the unlock sequence, the user application must write two consecutive values of 0xABCD and 0x4321 to the PWMxKEY register.

The initial PWM pin state cannot be set using the Configuration bits on the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. The initial state of all PWM pins is always high-impedance. Pull-up or pull-down resistors must be used to ensure that the power switches remain in the OFF state during a device Reset. The PWMPIN Configuration bit determines the ownership of the PWM pins after the device comes out of Reset. A setting of PWMPIN = 1 assigns ownership of the PWM pins to the GPIO module and makes them an input, while a setting of PWMPIN = 0 assigns ownership to the PWM module and makes them an output, with the state defined by the HPOL and LPOL Configuration bits.

On dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices the PWM pins are 5V-compatible in the open drain configuration.

QEI MODULE

The Quadrature Encoder Interface Module (QEI) is not implemented in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices. Users would need an alternative peripheral for position and speed feedback that does not utilize the QEI module.

TABLE 9: PWM MODULE DIFFERENCES

dsPIC33FJ32MC202	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102
8 channels, two different time bases	6 channels, one time base
Complimentary mode	Complimentary mode
Dead time	Dead time
ADC synchronization	ADC synchronization
Initial PWM pin status is set by Configuration bits	Initial state of all PWM pins is always high-impedance
Two remappable Fault inputs	Up to two Faults (Class B requirement compliant)
No PWM registers are write-protected	Selected PWM registers are write-protected
1220 Hz, 16-bit resolution (@40 MIPS, Edge-Aligned mode)	488 Hz, 16-bit resolution (@16 MIPS, Edge-Aligned mode)
610 Hz, 16-bit resolution (@40 MIPS, Center-Aligned mode)	244 Hz, 16-bit resolution (@16 MIPS, Center-Aligned mode)
39.1 kHz, 11-bit resolution (@40 MIPS, Edge-Aligned mode)	15.63 kHz, 11-bit resolution (@16 MIPS, Edge-Aligned mode)
19.55 kHz, 11-bit resolution (@40 MIPS, Center-Aligned mode)	7.81 kHz, 11-bit resolution (@16 MIPS, Center-Aligned mode)

SPI MODULE

The SPI module SDO1, SDI1, and SCK1 functions are not remappable on dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices.

I²C™ MODULE

No differences.

UART MODULE

No differences.

ADC MODULE

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are equipped with a 10-bit ADC, while the dsPIC33FJ32MC202 device is equipped with a 10/12-bit ADC. The maximum sampling frequency is 1.1 Msps for both 10-bit ADCs. As a consequence, in dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, the AD1CON1 register does not have the AD12B bit, which is used to enable or disable the 12-bit operation of the ADC. Table 10 lists the available register selections for the sample clock source selection.

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices allow an additional selection for the sample clock source select bits, which is the CTMU peripheral.

The ADC module can be operated using the system clock input or using the internal RC oscillator. If the system clock is used, users need to consider the maximum system clock frequency when calculating ADC conversion clock registers.

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices do not have the VREF+ and VREF- pins. The ADC uses internal AVSS and AVDD as the ADC reference.

Simultaneous sampling of up to four channels in 10-bit mode is supported on all devices. Table 11 lists the differences.

For dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, only AVDD and AVSS can be selected as reference voltages for the ADC. The dsPIC33FJ32MC202 device has a wider selection and combination, including external references. Table 12 summarizes these options.

The selection of the input analog channels varies slightly. Refer to the specific data sheet for details.

TABLE 10: ADC CONTROL REGISTER BIT DIFFERENCES

Register	dsPIC33FJ32MC202	dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102
AD1CON1<7:5> (SSRC<2:0>)	111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = Reserved 101 = Motor Control PWM2 interval ends sampling and starts conversion 100 = Reserved 011 = Motor Control PWM1 interval ends sampling and starts conversion 010 = GP Timer3 compare ends sampling and starts conversion 001 = Active transition on INT0 pin ends sampling and starts conversion 000 = Clearing sample bit ends sampling and starts conversion	111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = CTMU 101 = Reserved 100 = Reserved 011 = Motor Control PWM1 interval ends sampling and starts conversion 010 = GP Timer3 compare ends sampling and starts conversion 001 = Active transition on INT0 pin ends sampling and starts conversion 000 = Clearing sample bit ends sampling and starts conversion

TABLE 11: ADC MODULE DIFFERENCES

dsPIC33FJ32MC202	dsPIC33FJ16MC101/102	PIC24FJ16MC101/102
1 ADC	1 ADC	1 ADC
6 or 9 channels	4 or 6 channels	4 or 6 channels
10-bit, 1.1 Msps and 12-bit, 500 Ksps	10-bit, 1.1 Msps	10-bit, 1.1 Msps
Up to four simultaneous samples	Up to four simultaneous samples	Up to four simultaneous samples
Internal or external reference	AVDD/AVSS only	AVDD/AVSS only

TABLE 12: VOLTAGE REFERENCE INPUTS FOR THE dsPIC33FJ32MC202

Bit Setting	ADREF+	ADREF-
1xx	AVDD	AVSS
011	External VREF+	External VREF-
010	AVDD	External VREF-
001	External VREF+	AVSS
000	AVDD	AVSS

TABLE 13: VOLTAGE REFERENCE INPUTS FOR THE dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102

Bit Setting	ADREF+	ADREF-
xxx	AVDD	AVSS

COMPARATOR

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are equipped with a Comparator module that consists of three comparators, with each featuring blanking and filtering options.

RTCC MODULE

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are equipped with a Real-Time Clock and Calendar (RTCC).

The RTCC module is intended for applications where accurate time must be maintained for extended periods of time with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

CTMU MODULE

The dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices are equipped with a Charge Time Measurement Unit (CTMU).

The CTMU is a flexible analog peripheral that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. It can be efficiently used to implement human interface (sliders, buttons) or as a sensitive temperature sensor.

FAULT PINS (CLASS B OPERATION)

The Motor Control PWM module of the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices incorporates up to two Fault inputs, FLTA1 and FLTB1. These Fault inputs are implemented with Class B safety features and are not remappable as in the dsPIC33FJ32MC202 device. These features ensure that the PWM outputs enter a safe state when either of the fault inputs is asserted. The FLTA1 and FLTB1 pins, when enabled and having ownership of a pin, also enable a soft internal pull-down resistor. The soft pull-down provides a safety feature by automatically asserting the Fault should a break occur in the Fault signal connection.

CONFIGURATION WORDS

The dsPIC33FJ32MC202 device provides nonvolatile memory implementation for device Configuration bits. The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000. Note that address 0xF80000 is beyond the user program memory space. It belongs to the configuration memory space (0x800000 0xFFFFFF), which can only be accessed using table reads and table writes.

In dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices, the Configuration Shadow register bits can be configured (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These read only bits are mapped starting at program memory location 0xF80000. Note that address 0xF80000 is beyond the user program memory space and belongs to the configuration memory space (0x800000-0xFFFFFF) which can only be accessed using table reads. In dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102 devices, the configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in the two words at the top of the on-chip program memory space, known as the Flash Configuration Words. These are packed representations of the actual device Configuration bits, whose actual locations are distributed among several locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during device Resets. When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

MEMORY PROTECTION

The dsPIC33FJ32MC202 device offers memory protection, enabling multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property (IP) in collaborative system designs. When coupled with software encryption libraries, memory protection can be used to securely update Flash even when multiple IPs reside on the single chip. The memory protection features are controlled by the Configuration registers: FBS and FGS. Secure segment and RAM protection is not implemented in the dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices.

ELECTRICAL CHARACTERISTICS

The maximum I/O pin source/sink output current is 4 mA for the dsPIC33FJ32MC202 device and 8 mA for dsPIC33FJ16MC101/102 or PIC24FJ16MC101/102 devices.

APPENDIX A: REVISION HISTORY

Revision A (August 2011)

This is the initial released version of this document.

Revision B (September 2011)

This revision includes updates to text and formatting for clarification purposes.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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