
Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8221 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8221 in a new design. A summary of these items is provided in [Section 10.0, "Hardware Checklist Summary"](#). Detailed information on these subjects can be found in the corresponding sections:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power"](#)
- [Section 4.0, "Twisted Pair Media Interface \(CAT5\)"](#)
- [Section 5.0, "SGMII/SerDes MAC Interface"](#)
- [Section 6.0, "Device Clocks"](#)
- [Section 7.0, "Hardware Configuration Using CMODE Pins"](#)
- [Section 8.0, "Digital Interface"](#)
- [Section 9.0, "Miscellaneous"](#)

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8221 implementor should have the following documents on hand:

- *VSC8221 Single-Port 10/100/1000BASE-T PHY with 1.25 Gbps SerDes for SFPs/GBICs Data Sheet*
- VSC8221 device documents (at <https://www.microchip.com/en-us/product/VSC8221#document-table>)
- VSC8221EV EVB documents, including the schematics, PCB file, BOM, etc. (at <https://my.microsemi.com/AWeI-come/FileDownload.aspx>)

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

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3.0 POWER

Table 3-1 shows the power supply pins for the VSC8221.

TABLE 3-1: POWER SUPPLY PINS

Pin Name	Pin	Description	Comments
Digital I/O Power Pins			
VDDIO	H4	3.3V or 2.5V Power for the RXLOS/SIGDET and MODDEF0/CLKOUT pins	Digital I/O, no ferrite bead
VDDIOMICRO	H8	3.3V or 2.5V Power for SMI, EEPROM interface, and CLKOUTMICRO clock	Digital I/O, no ferrite bead
VDDIOCTRL	C4	3.3V or 2.5V Power for JTAG I/O	Digital I/O, no ferrite bead
Digital Core Power Pin			
VDD12	G10, F3, G3, F8, H7	1.2V Power for internal digital logic, PLL, and SerDes/SGMII I/O Power	Digital core power, no ferrite bead
Analog Power Pins			
VDD33A	C8, D9	3.3V Power for MDI, CMODE, PLL, and LED blocks	Analog, use ferrite bead
VDDREG	C9	3.3V Power for on-chip switching regulator	Analog, use ferrite bead
VDD12A	E9	1.2V Power for internal PLL and ADC	Analog core power, use ferrite bead
On-Chip Regulator Control and Output Pins			
REGEN	C10	On-chip regulator enable	Tie to VDD33A (3.3V) to enable the internal 1.2V regulator for normal chip operation.
REGOUT	D10	On-chip regulator supply output	This is the output of the on-chip switching regulator, which generates the primary 1.2V power supply voltage VDD12 . REGOUT must be connected to an off-chip “LC” filter.
Ground Pins			
VSS	D4, D5, D6, D7, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7, C6, C7, D8, E8, H6	0V, general device ground for all blocks	—

3.1 Current and Power Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. Refer to [Table 3-2](#), [Table 3-3](#), [Table 3-4](#), [Table 3-5](#), [Table 3-6](#), [Table 3-7](#), and [Table 3-8](#) for different system configurations. Use one table as a reference for the system power design based on system configuration. Note that the power dissipation values in the table need 25% to 30% more margin at least in the system design.

TABLE 3-2: VDDIO AT 3.3 V, SERDES-CAT5, SCLK DISABLED

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	367 mA
Analog Power	3.3V for VDD33A/VDDREG	114.5 mA
Analog Core Power	1.2V for VDD12A	39 mA
Total Power Dissipation (PD)	—	908 mW

TABLE 3-3: VDDIO AT 3.3 V, SGMII-CAT5 (1000 MBPS), SCLK DISABLED

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	367 mA
Analog Power	3.3V for VDD33A/VDDREG	114.5 mA
Analog Core Power	1.2V for VDD12A	39 mA
Total Power Dissipation (PD)	—	908 mW

TABLE 3-4: VDDIO AT 3.3 V, SGMII-CAT5 (100 MBPS), SCLK DISABLED

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	135 mA
Analog Power	3.3V for VDD33A/VDDREG	94.5 mA
Analog Core Power	1.2V for VDD12A	28 mA
Total Power Dissipation (PD)	—	550 mW

TABLE 3-5: VDDIO AT 3.3 V, SGMII-CAT5 (10 MBPS), SCLK DISABLED

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	61 mA
Analog Power	3.3V for VDD33A/VDDREG	155.5 mA
Analog Core Power	1.2V for VDD12A	28 mA
Total Power Dissipation (PD)	—	661 mW

TABLE 3-6: VDDIO AT 3.3 V SERDES-CAT5, SCLK ENABLED

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	379 mA
Analog Power	3.3V for VDD33A/VDDREG	114.5 mA
Analog Core Power	1.2V for VDD12A	39 mA

TABLE 3-6: VDDIO AT 3.3 V SERDES-CAT5, SCLK ENABLED (CONTINUED)

Power Rail Classification	Voltage	Maximum mA and PD
Total Power Dissipation (PD)	—	920 mW

TABLE 3-7: VDDIO AT 3.3 V SERDES-CAT5, SFP MODE ON

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Digital Core Power	1.2V for VDD12	283 mA
Analog Power	3.3V for VDD33A/VDDREG	114.5 mA
Analog Core Power	1.2V for VDD12A	39 mA
Total Power Dissipation (PD)	—	806 mW

TABLE 3-8: VDDIO AT 3.3 V SERDES-CAT5, SFP MODE ON, REGULATOR ON

Power Rail Classification	Voltage	Maximum mA and PD
Digital I/O Power	3.3V for VDDIO/MICRO/CTRL	12.5 mA
Analog Power	3.3V for VDD33A	114 mA
Analog Power	3.3V for VDDREG	129.5 mA
Total Power Dissipation (PD)	—	846 mW

3.2 Power Supply Planes

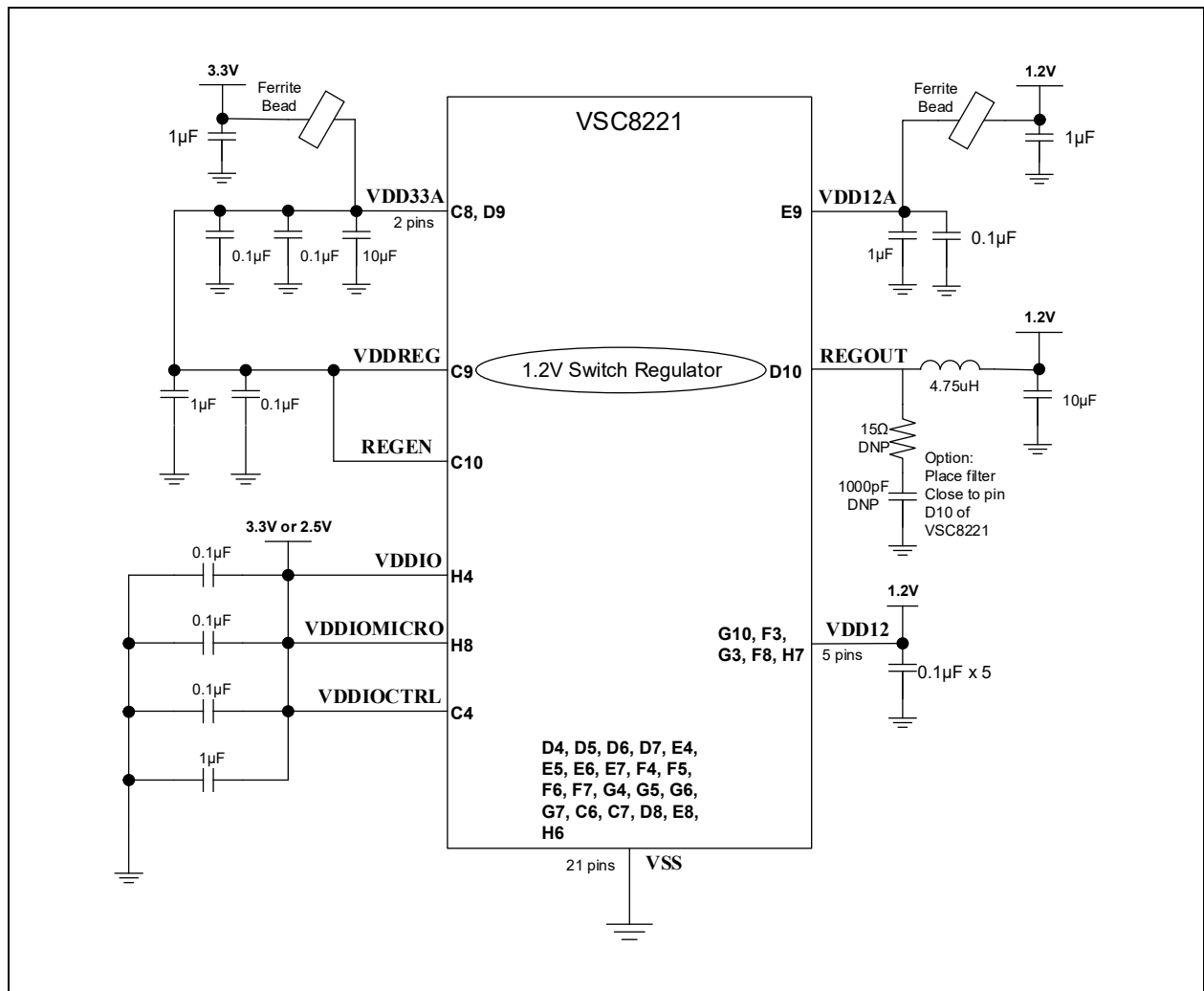
- The VSC8221 requires two power rails of 3.3V and 1.2V or three power rails of VDDIO 2.5V, 3.3V, and 1.2V. The filtered analog 1.2V and 3.3V (or 2.5V) supplies should not be shorted to any other digital supply at the package or PCB level. See [Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"](#).
- The most important PCB design and layout considerations are as follows:
 - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
 - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
 - Minimize resistive drop while efficiently conducting away heat from the device using one ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power the pins of the device with correctly positioned local decoupling. For more information, see [Section 3.4, "Bulk Decoupling Capacitors"](#).
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are:
 - VDD33A
 - VDDREG
 - VDD12A
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended for digital supplies VDDIO, VDDIOMICRO, VDDIOCTRL, and VDD12.

The power and ground connections are shown in [Figure 3-1](#).

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8221's power pins.
- Make sure that enough bulk capacitors (1 µF to 22 µF) are incorporated in each power rail of the power supply.
- If the VSC8221 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 TWISTED PAIR MEDIA INTERFACE (CAT5)

4.1 10/100/1000 Mbps Interface Connection

The VSC8221 has one GPHY that supports 10/100/1000Base-T Ethernet Gigabit port. Details on the pin numbers for this GPHY are described as follows:

- **TXVNA (B9):** This pin is the transmit/receive negative connection from Pair A of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPA (A9):** This pin is the transmit/receive positive connection from Pair A of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNB (B8):** This pin is the transmit/receive negative connection from Pair B of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPB (A8):** This pin is the transmit/receive positive connection from Pair B of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNC (B7):** This pin is the transmit/receive negative connection from Pair C of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPC (A7):** This pin is the transmit/receive positive connection from Pair C of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVND (B6):** This pin is the transmit/receive negative connection from Pair D of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPD (A6):** This pin is the transmit/receive positive connection from Pair D of the internal GPHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

There are two types of 10/100/1000 Mbps channel connection solutions. As shown in [Figure 4-1](#), the first solution is for cases wherein no electrical noise external environment and ESD are taken into consideration. The second solution, on the other hand, is for instances wherein electrical noise external environment and ESD are considered. See [Figure 4-2](#).

FIGURE 4-1: FIRST SOLUTION FOR 10/100/1000 MBPS CHANNEL CONNECTION

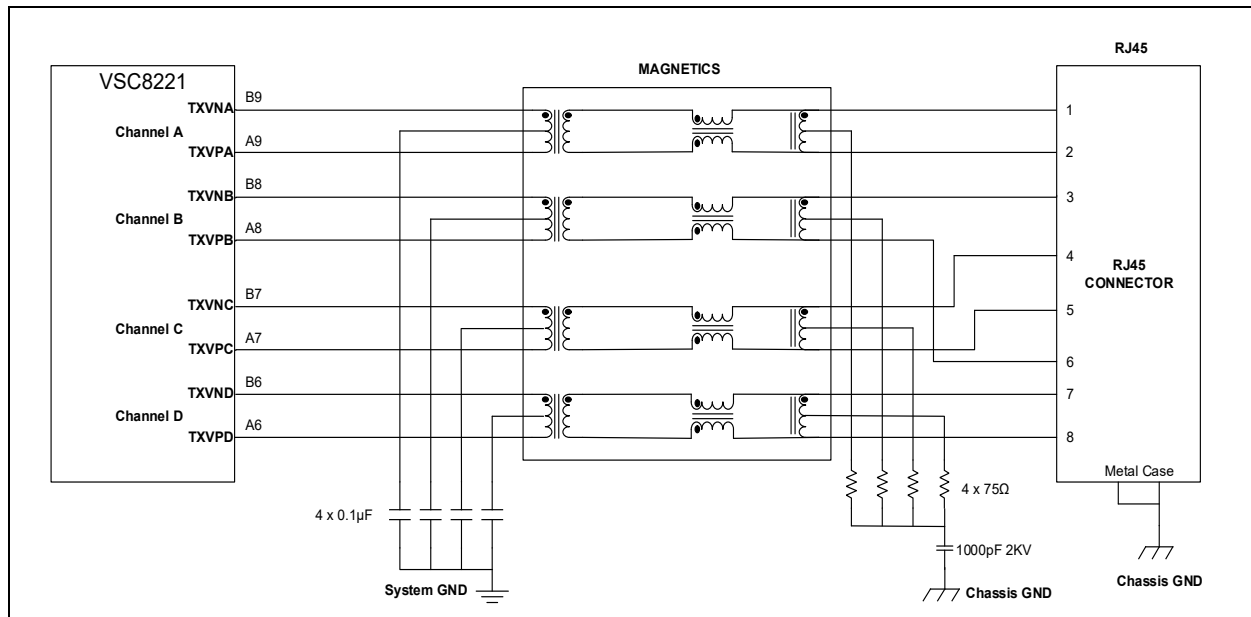
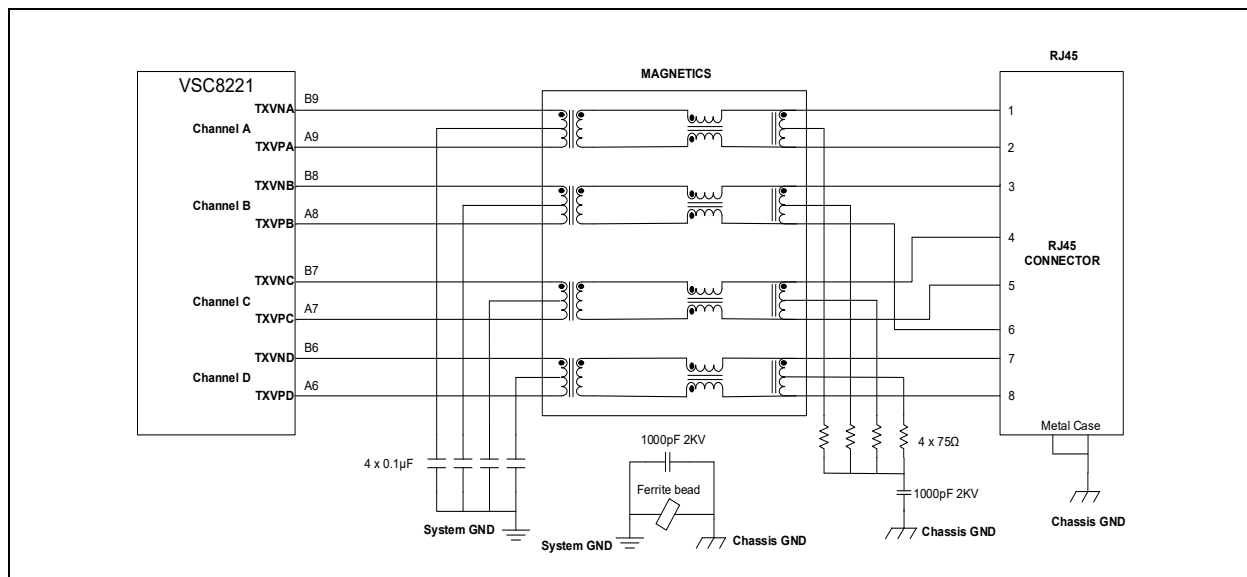


FIGURE 4-2: SECOND SOLUTION FOR 10/100/1000 MBPS CHANNEL CONNECTION



4.2 10/100/1000 Magnetics and RJ45 Connector Connection

- The center tap connection on the VSC8221 side for Pair A channel only connects a 0.1 μF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8221 side for Pair B channel only connects a 0.1 μF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8221 side for Pair C channel only connects a 0.1 μF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8221 side for Pair D channel only connects a 0.1 μF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetics should not be connected together. The reason is the common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- It is recommended that the center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead should connect between the chassis ground and the system ground.
- The RJ45 shield should connect to the chassis ground. This includes RJ45 connectors with or without integrated magnetics. See [Section 4.3, "PCB Layout Considerations"](#) for guidance on how the chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on Microchip Technology product page) for reference.

4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss that requires a PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each member of a pair should be matched in length to prevent mismatch in delay that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8221 device or other sensitive devices in the PCB layout placement for better ESD.

5.0 SGMII/SERDES MAC INTERFACE

5.1 SGMII/SerDes MAC Pins and Connection

- The VSC8221 device supports one SGMII MAC or one SerDes MACs.
- Refer to [Table 5-1](#) for pin number details. For SGMII/SerDes interface connections, see [Figure 5-1](#) and [Figure 5-2](#).

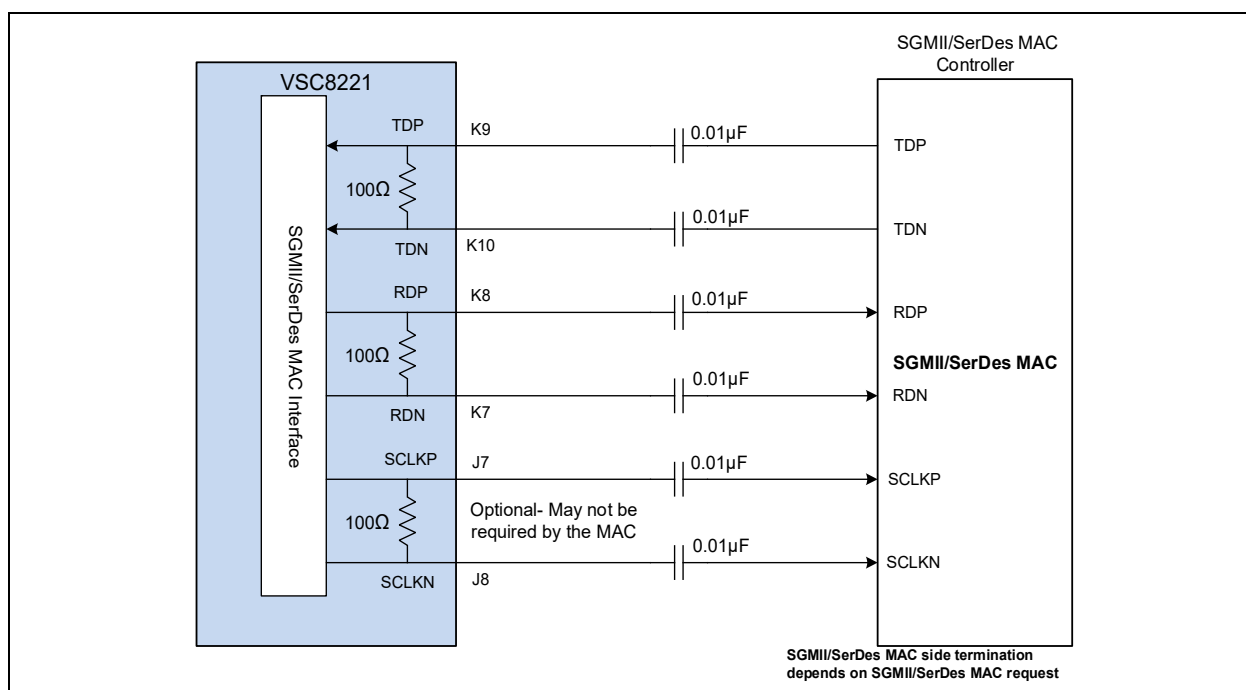
TABLE 5-1: REFCLK FREQUENCY SELECTION

Pin Name	Pin Number	Type	Description
RDN	K7	Output	Receiver data differential output pair
RDP	K8	Output	
TDN	K10	Input	Transmitter data differential input pair
TDP	K9	Input	
SCLKN	J8	Output	SGMII clock differential output pair
SCLKP	J7	Output	

5.2 SGMII/SerDes MAC

- When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8221 device can be connected to an SGMII/SerDes-compatible MAC.

FIGURE 5-1: SGMII/SERDES MAC INTERFACE CONNECTIONS



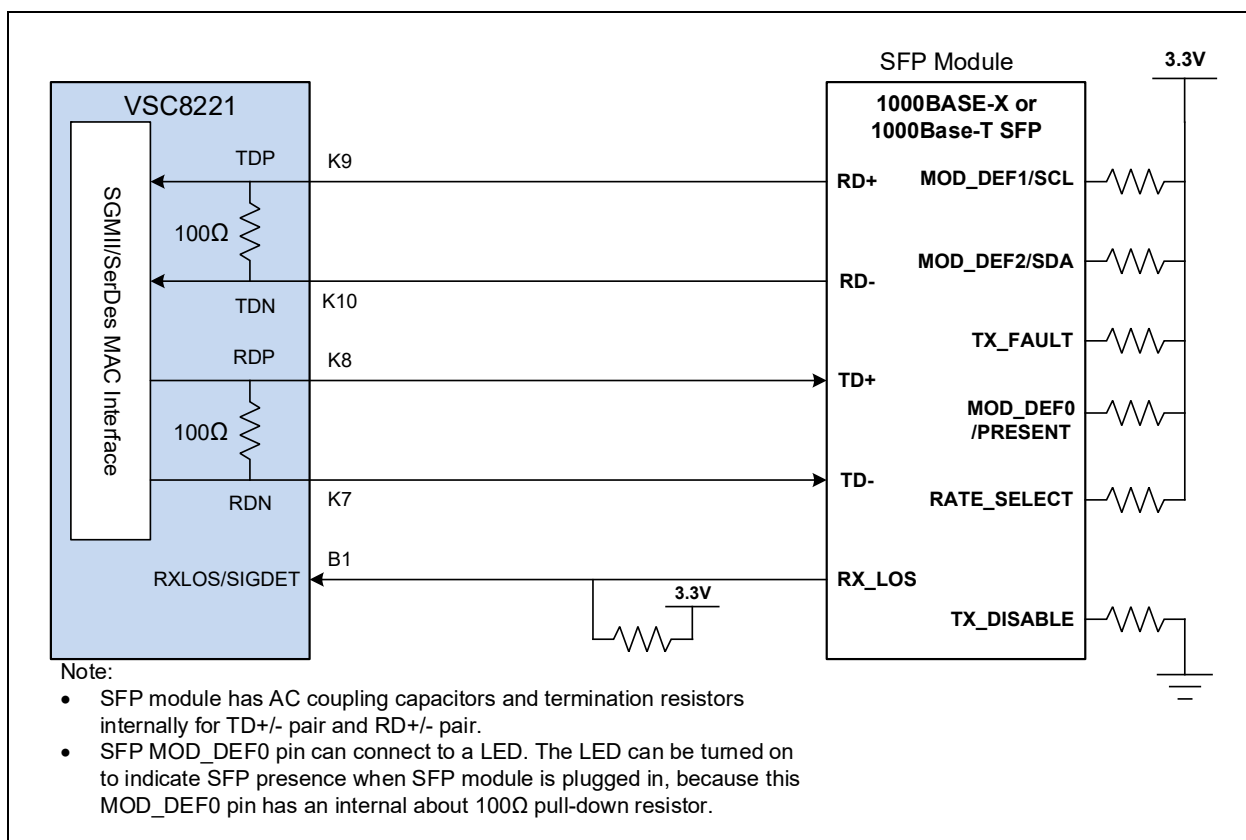
5.3 SerDes MAC Interface to SFP

- When connected to a SerDes MAC-compliant to 1000BASE-X, the VSC8221 device provides data throughput at a rate of 1000 Mbps only. 10 Mbps and 100 Mbps rates are not supported.
- For additional pin in SerDes MAC interface to SFP fiber transceiver module, see [Table 5-2](#). [Figure 5-2](#) shows the SerDes MAC interface connection to 1000Base-X SFP or 1000Base-T SFP.

TABLE 5-2: ADDITIONAL PIN RXLOS FOR SERDES TO SFP

Pin Name	Pin Number	Type	Description
RXLOS/SIGDET	B1	I/O	The customer can connect the SIGDET pin from a Fiber module (or the RXLOS from an SFP). See Table 7-4 for information on using CMODE configuration pin CMODE1[3] to set either RXLOS or SIGDET .
			RXLOS – Receiver Loss of Signal Output (valid in SFP mode, when MII Register 21E.15 = 1) RXLOS pin is input, the receiving loss signal comes from the output of SFP LOS pin. This active-high signal is asserted when receiving signal loss.
			SIGDET – SerDes Signal Detect (I/O) (valid in IEEE Mode, when MII Register 21E.15= 0) SIGDET can be configured as an input or output and can be set to function as active-low or active-high by using CMODE1[1] and CMODE1[3] at startup. See Table 7-3 and Table 7-4 for details.
			SIGDET as Input: When used as an input, the SIGDET signal is meant to be connected to the signal detect output of the fiber optic transceiver. If SIGDET is high, this indicates received activity on the fiber optic transceiver. If SIGDET is not used as an input, the PHY internally generates the signal detect function from the incoming data on the TDP and TDN signal pins. SIGDET as Output: For Serial MAC to CAT5 Media PHY Operating modes, SIGDET is asserted if a valid CAT5 link has been established.

FIGURE 5-2: SERDES MAC INTERFACE TO 1000BASE-X SFP OR 1000BASE-T SFP CONNECTIONS



5.4 SGMII/SerDes MAC Interface Design Rules

- Use AC coupling with 0.01 μ F capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50 Ω (100 Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce cross-talk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If the SGMII/SerDes port is unused, both the **RDx** pair and **TDx** pair pins can be left floating (no-connect).

6.0 DEVICE CLOCKS

6.1 Reference Clock

- The device reference clock supports both 25 MHz and 125 MHz clock signals.
- Refer to [Table 6-1](#) for pin details. For information on reference circuit connection, see [Figure 6-1](#), [Figure 6-2](#), and [Figure 6-3](#).

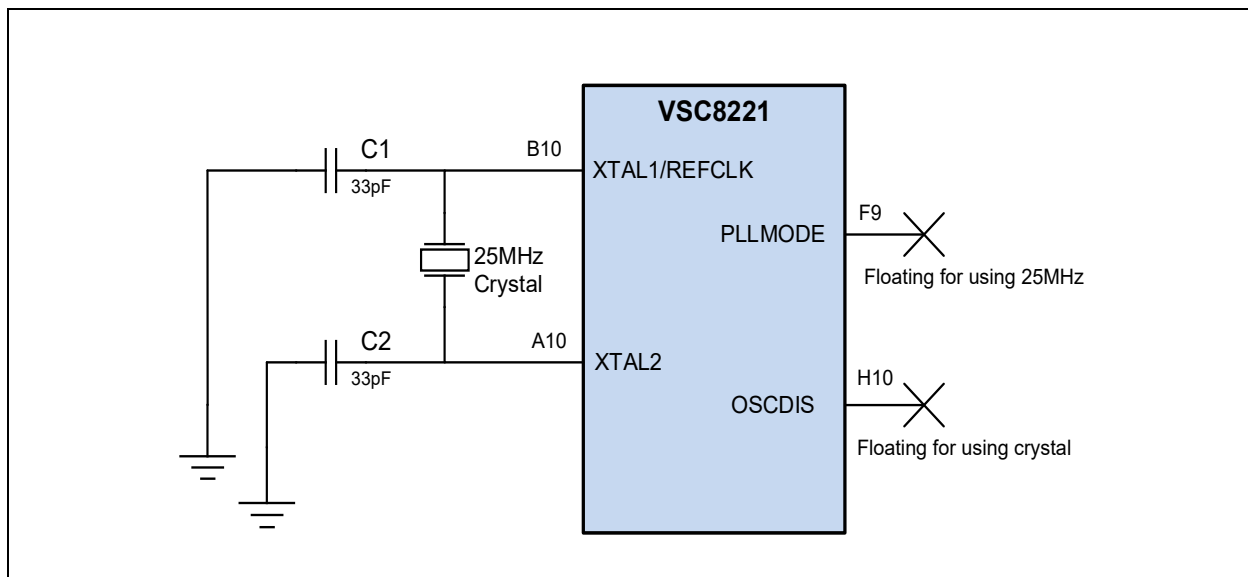
TABLE 6-1: REFERENCE CLOCK RELATED PINS

Pin Name	Pin Number	Type	Description
XTAL1/REFCLK	B10	I	XTAL1/REFCLK – Crystal or Oscillator Input XTAL1 is used as 25 MHz crystal circuit input. REFCLK is used as 25 MHz or 125 MHz oscillator clock input.
XTAL2	A10	O	XTAL2 Crystal Output XTAL2 is used for 25 MHz crystal circuit output.
EECLK/PLLMODE	F9	O, IPD	PLLMODE – PLL Mode Select Input 0: When low (default), a reference clock of 25 MHz is expected at the REFCLK pin from either an 25 MHz crystal or a 25 MHz oscillator. 1: When PLLMODE is high, the PHY expects a 125 MHz clock input as the PHY's reference clock.
CLKOUTMICRO/OSCDIS	H10	O, IPU	OSCDIS – Active Low On-chip Oscillator Disable Input 1: When high (default), the PHY enables the internal on-chip oscillator allowing operation with a 25 MHz crystal by using XTAL1 and XTAL2. 0: When low, the PHY's oscillator is turned off and the PHY must be supplied with an external 25 MHz or 125 MHz oscillator clock on the REFCLK pin.

6.2 25 MHz Crystal Circuit

The **OSCDIS** strap pin should be high (default). A 25 MHz parallel resonant crystal with a ± 50 ppm frequency tolerance should be connected between **XTAL1** and **XTAL2** pins. Each pin requires a capacitor to ground directly when a crystal is used. Since every system is unique, the capacitor values are system independent based on the CL specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. For more information on this topic, refer to the article titled, *Calculating Crystal Load Capacitor* at microchipsupport.force.com. The **PLLMODE** pin should be left floating (or pulled low) for using 25 MHz clock frequency. See [Figure 6-1](#) for details.

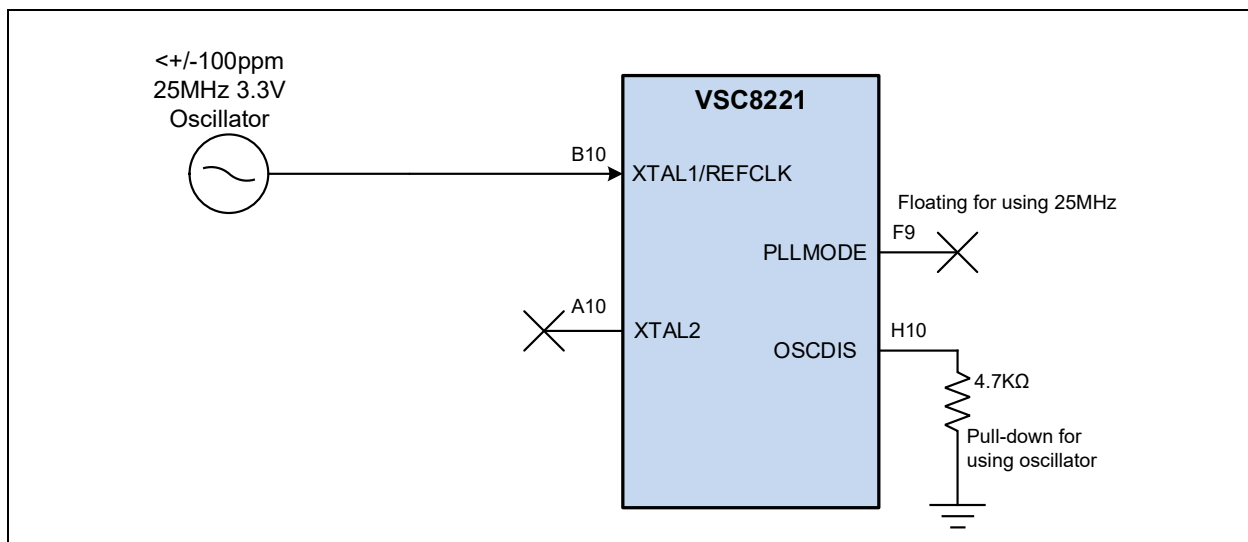
FIGURE 6-1: 25 MHz CRYSTAL CIRCUIT AND CONFIGURATION



6.3 25 MHz Oscillator Circuit

To use a single-ended reference clock from a 25 MHz oscillator, refer to the configurations for a single-ended **REFCLK** in [Figure 6-2](#). The **PLLMODE** pin should be left floating (or pulled low) on Reset for using 25 MHz clock frequency. The **OSCDIS** pin should have an external pull-down resistor for using an oscillator.

FIGURE 6-2: 25 MHz OSCILLATOR CIRCUIT AND CONFIGURATION

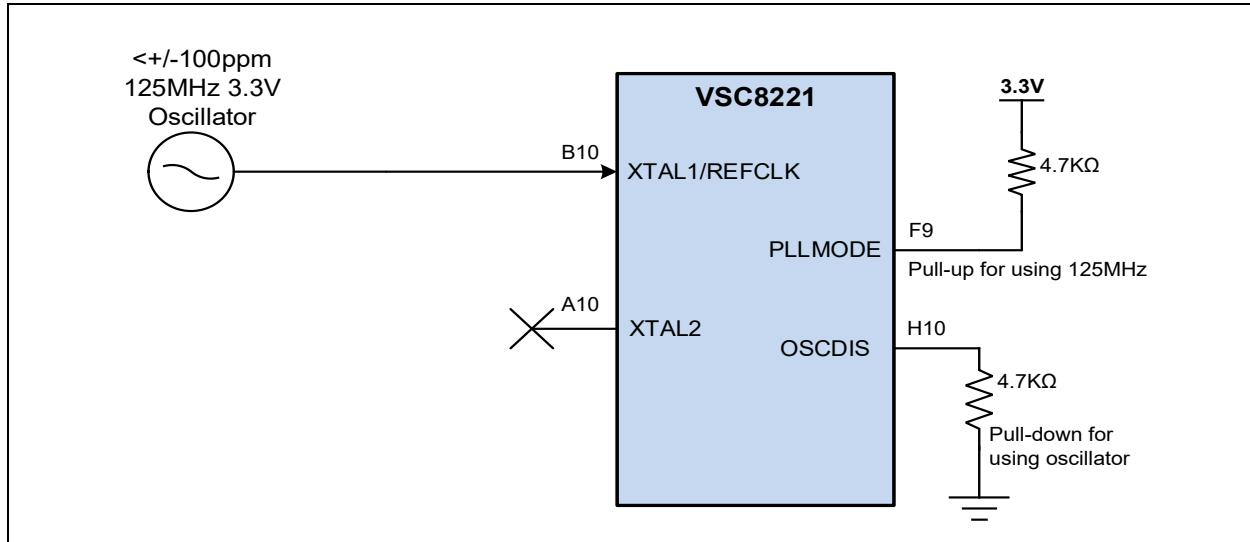


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6.4 125 MHz Oscillator Circuit

To use a single-ended reference clock from a 125 MHz oscillator, refer to the configurations for a single-ended **REFCLK** in [Figure 6-3](#). The **PLLMODE** pin should be high with a pull-up resistor on Reset for using 125 MHz clock frequency. The **OSCDIS** pin should have an external pull-down resistor for using an oscillator.

FIGURE 6-3: 125 MHZ OSCILLATOR CIRCUIT AND CONFIGURATION



7.0 HARDWARE CONFIGURATION USING CMODE PINS

7.1 CMODE Pins and Description

- Each of the four CMODE pins (CMODE [3:0]) is used to latch a four-bit value at PHY Reset. A total of 16 CMODE configuration bits are set at Reset based on pull-down and pull-up resistors values. Each CMODE bit represents the default value of a particular PHY register bit and therefore sets a default PHY operating condition at startup. See [Table 7-1](#) for pin details.

TABLE 7-1: CMODE PINS AND DESCRIPTION

Pin Name	Pin Number	Type	Description
CMODE0	A5	I	Pull up/down different resistor values to get different CMODE0[3:0] value
CMODE1	B5	I	Pull up/down different resistor values to get different CMODE1[3:0] value
CMODE2	C5	I	Pull up/down different resistor values to get different CMODE2[3:0] value
CMODE3	B4	I	Pull up/down different resistor values to get different CMODE3[3:0] value

7.2 Select Mode Pins Pull-Up and Pull-Down Resistor Value for System Design

- The CMODE bits are set by connecting each CMODE pin to either VDD33A or VSS (ground) through an external 1% resistor. The four-bit value latched by the PHY on each CMODE pin depends upon the value of the resistor used to pull up or pull down the CMODE pin. CMODE resistor values and connections are defined in [Table 7-2](#).

TABLE 7-2: CMODE PIN PULL-UP /PULL-DOWN RESISTOR VALUE VS. CMODE BITS VALUE

CMODE Pin Pull-Down Resistor Values (kΩ)	CMODE Pin Pull-Up Resistor Values (kΩ)	CMODEx [3:0] Values (X = 0,1,2, and 3)	CMODE 0,1,2,3 Pin Bit [3]	CMODE 0,1,2,3 Pin Bit [2]	CMODE 0,1,2,3 Pin Bit [1]	CMODE 0,1,2,3 Pin Bit [0]
0	—	0000	0	0	0	0
2.26	—	0001	0	0	0	1
4.02	—	0010	0	0	1	0
5.90	—	0011	0	0	1	1
8.25	—	0100	0	1	0	0
12.1	—	0101	0	1	0	1
16.9	—	0110	0	1	1	0
22.6	—	0111	0	1	1	1
—	0	1000	1	0	0	0
—	2.26	1001	1	0	0	1
—	4.02	1010	1	0	1	0
—	5.90	1011	1	0	1	1
—	8.25	1100	1	1	0	0
—	12.1	1101	1	1	0	1
—	16.9	1110	1	1	1	0
—	22.6	1111	1	1	1	1

7.3 CMODE Bits

Table 7-3 outlines the mapping of each CMODE bit to a PHY operating condition parameter. Each of the PHY operating condition parameters is described in detail in Table 7-3 and Table 7-4.

TABLE 7-3: CMODE PINS AND BITS OPERATION CONDITION PARAMETER DESCRIPTIONS

CMODE Pin Name	Description for Every Bit of each CMODE Pin			
	Bit [3]	Bit [2]	Bit [1]	Bit [0]
CMODE0	PHY Address [3]	PHY Address [2]	PHY Address [1]	PHY Address [0]
CMODE1	SFP Mode Disable 0: See Table 7-4 for details. 1: See Table 7-4 for details.	PHY Address [4]	SIGDET pin direction 0: Input 1: Output	SerDes line impedance 0: 50Ω 1: 75Ω
CMODE2	PHY Operating Mode [3]	PHY Operating Mode [2]	PHY Operating Mode [1]	PHY Operating Mode [0]
CMODE3	LED Control [1] 0: See Table 7-4 for details. 1: See Table 7-4 for details.	SQE Enable 0: SQE Disable (default) 1: SQE Enable (10BT Half-Duplex mode only)	Reserved	Auto-Negotiation Advertisement Control [1] 0: 10/100/1000 HDX, FDX 1: 10/100 HDX, FDX

TABLE 7-4: OTHER OPERATION CONDITION PARAMETER DESCRIPTIONS

Name	CMODE Pin Name and Bit Position	CMODE Bit Value	Description
PHY Address [4:0]	CMODE1[2] + CMODE0 [3:0]	31-0	Sets the PHY Address used to access PHY Registers when the PHY's SMI is in IEEE mode.
PHY Operating Mode [3:0]	CMODE2 [3:0]	—	The value latched is reflected in the MII Register 23. 15:12 + 2:1.
		0000	802.3z SerDes to CAT5 Media, MAC interface Clause 37 auto-negotiation auto-sense enabled
		0100	802.3z SerDes to CAT5 Media, Clause 37 disabled
		0101	SGMII to CAT5 Media, SCLK enabled
		1010	802.3z SerDes to CAT5 Media, Media Connector mode
		1110	802.3z SerDes to CAT5 Media, Clause 37 enabled
		1111	SGMII to CAT5 Media, SCLK disabled

TABLE 7-4: OTHER OPERATION CONDITION PARAMETER DESCRIPTIONS (CONTINUED)

Name	CMODE Pin Name and Bit Position	CMODE Bit Value	Description
SFP Mode Disable	CMODE1[3]	This CMODE bit sets the default value of MII Register 21E.15.	
		0	This sets MII Register 21E.15 = 1. Sets the following PHY defaults: a) TXDIS/SRESET is active-high and behaves like TXDIS . b) MODDEF0/CLKOUT pin functions like MODDEF0 . This pin is asserted low by the PHY once the EEPROM interface is released for access through the SMI. c) RXLOS/SIGDET pin functions like the RXLOS . d) The SMI is set in MSA mode.
		1	This sets MII Register 21E.15 = 0. Sets the following PHY defaults: a) TXDIS/SRESET is active-low and behaves like SRESET . b) MODDEF0/CLKOUT pin functions like CLKOUT and drives out a 125 MHz clock. c) RXLOS/SIGDET pin functions like the SIGDET . d) The SMI is set in IEEE mode.
LED Control [1]	CMODE3[3]	This sets the default behavior of LED pins LED [2:0] by setting the startup values of MII Register Bit Register 27 (1Bh) – LED Control Register.	
		0	LED [2:0] = {Link10/Activity, Link100/Activity, Link1000/Activity} (MII Reg 27 = 0000h)
		1	LED [2:0] = {Link/Activity, Link/Activity, Fault} (MII Reg 27 = AA80h)

8.0 DIGITAL INTERFACE

8.1 Dual Mode Serial Management Interface (SMI)

- The Serial Management Interface provides access to the PHY registers for device configuration and status information. It also provides access to the EEPROM connected to the **EEDAT** and **EECLK** pins (EEPROM interface) of the PHY. For details on EEPROM access through the SMI, refer to [Table 8-1](#). There are dual modes of MSA and IEEE by setting the MII register 21E.15 at startup. For MSA mode-related and IEEE mode-related pins and settings, see [Table 8-2](#) and [Table 8-3](#).
- The **MODDEF1/MDC**, **MODDEF2/MDIO**, and **MDINT** pins comprise the SMI. See [Table 8-1](#) for details on SMI pin descriptions.

TABLE 8-1: SMI PINS

Pin Name	Pin Number	Type	Description
MODDEF1/ MDC	J10	I	The functionality of this pin is determined by the value of MII register 21E.15 'SFP MODE' set at startup using CMODE hardware configuration or via the EEPROM interface.
MODDEF2/ MDIO	J9	I/O	The functionality of this pin is determined by the value of MII register 21E.15 'SFP MODE' set at startup using CMODE hardware configuration or via the EEPROM interface.
MDINT	H9	OD	Management Data Interrupt MDINT is asserted whenever there is a change in the operating status of the device. This open-drain signal indicates a change in the PHY's link operating conditions for which a station manager must interrogate to determine further information.

8.1.1 PHY REGISTER ACCESS WITH SMI IN MSA MODE

- In this mode, the PHY registers are accessed using the standard MSA-compliant protocol. This protocol is generally used for reading and writing to Microchip's AT24 series-compatible EEPROMs.
- In this SMI in MSA mode, the SMI pin functions are described in [Table 8-2](#). Refer to the table for the pin numbers and additional information on SMI MSA mode.

TABLE 8-2: SMI PINS FOR MSA MODE

Pin Name	Pin Number	Type	Description
MODDEF1	J10	I	MODDEF1 – Serial MSA Clock (Set CMODE1[3]=0 in SFP Mode or set MII Register 21E.15=1) MODDEF1 is the clock input of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the protocol specified in the MSA specification. Although typically operated at 100 kHz, MODDEF1 can be operated at a maximum of 1 MHz.
MODDEF2	J9	I/O	MODDEF2 – Serial I/O Data (Set CMODE1[3]=0 in SFP Mode or set MII Register 21E.15=1) MODDEF2 is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the protocol specified in the MSA specification. This pin normally requires a 1.5 kΩ to 4.7 kΩ pull-up resistor to VDDIOMICRO at the station manager. The value of the pull-up resistor depends on the MODDEF1 frequency and the capacitive load on the MODDEF2 line.

TABLE 8-2: SMI PINS FOR MSA MODE (CONTINUED)

Pin Name	Pin Number	Type	Description
MDINT	H9	OD	Management Data Interrupt The assertion polarity of MDINT is determined by the presence of a pull-up or pulldown on the MDINT pin. If the MDINT pin is pulled up to VDDIOMICRO using a 4.7 k Ω to 10 k Ω resistor, it becomes an active-low signal. If the MDINT pin is pulled down using a 4.7 k Ω to 10 k Ω resistor, then it becomes an active-high signal.

8.1.2 PHY REGISTER ACCESS WITH SMI IN IEEE MODE

- In IEEE mode, the SMI is fully compliant with the IEEE 802.3-2000 MII specifications.
- In this SMI with IEEE mode, the SMI pin functions are described as follows. Refer to [Table 8-3](#) for the pin numbers and more information in SMI IEEE mode.

TABLE 8-3: SMI PINS FOR IEEE MODE

Pin Name	Pin Number	Type	Description
MDC	J10	I	MDC – Management Data Clock (Set CMODE1 [3]=1 in IEEE Mode or set MII Register 21E.15=0) MDC is the clock input of the two wires serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. Although typically operated at less than 100 kHz due to frequency limitations of the EEPROM used with the PHY, the PHY registers can be accessed at a maximum frequency of 1 MHz.
MDIO	J9	I/O	MDIO – Serial I/O Data (Set CMODE1[3]=1 in IEEE Mode or set MII Register 21E.15=0) MDIO is the data line of the two-wire serial interface for accessing the PHY's registers or the EEPROM connected to the EEPROM interface using the Serial Management Interface protocol specified in the IEEE 802.3 specification. This pin normally requires a 1.5 k Ω to 4.7 k Ω pull-up resistor to VDDIOMICRO at the Station Manager. The value of the pull-up resistor depends on the MDC frequency and the capacitive load on the MDIO line.
MDINT	H9	OD	Management Data Interrupt The assertion polarity of MDINT is determined by the presence of a pull-up or pulldown on the MDINT pin. If the MDINT pin is pulled up to VDDIOMICRO using a 4.7 k Ω to 10 k Ω resistor, it becomes an active-low signal. If the MDINT pin is pulled down using a 4.7 k Ω to 10 k Ω resistor, then it becomes an active-high signal.

8.2 EEPROM Interface

- The EEPROM interface consists of the **EEDAT** and **EECLK** pins of the PHY. If this interface is used, these pins should connect to the **SDA** and **SCL** pins, respectively, of a serial EEPROM that is compatible with the AT24xxx series of Microchip EEPROMs. The EEPROM interface on the VSC8221 serves the following purposes:
 - It provides the PHY with the ability to configure its self-internal registers.
 - The system manager can access the EEPROM to obtain information pertaining to the system or module configuration.
 - A single EEPROM can be shared among multiple PHYs for their custom configuration.
- The PHY detects the EEPROM based on the presence of a pull-up on the **EEDAT** pin. It is initialized using the configuration EEPROM (if present) under the three conditions: (1) **RESET** deassertion, (2) **TXDIS/SRESET** deassertion, and (3) S/W Reset (MII Register 0.15 is asserted). See [Table 8-4](#) for detailed EEPROM interface pin descriptions.

TABLE 8-4: EEPROM INTERFACE PINS

Pin Name	Pin Number	Type	Description
EECLK/PLLM-ODE	F9	Ozc/lpd	EECLK – EEPROM Clock Output This output is the clock line of the two-wire, MSA-compliant serial EEPROM interface. This pin should be connected to the SCL input pin of the AT24 series of Microchip EEPROMs. PLLMODE – PLL Mode Select input PLLMODE is sampled during the device power-up sequence or on Reset. When PLLMODE pin is high, the PHY expects a 125 MHz clock input as the PHY's reference clock. When default with internal pull-down, 25 MHz is expected at REFCLK pin from either an external crystal or oscillator.
EEDAT	G9	Ozc/lpd	EEPROM Serial I/O Data This bidirectional signal is the data line of the two-wire, MSA-compliant serial EEPROM interface. This pin should be connected to the SDA pin of the AT24 series of Microchip EEPROMs. The PHY determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when RESET is deasserted. If EEDAT has a 4.7 kΩ to 10 kΩ external pull-up resistor (to VDDIOMICRO), it assumes that an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.

8.3 JTAG Interface

- If JTAG is not used, $\overline{\text{TRST}}$ should be pulled low by a pull-down resistor. Refer to [Table 8-5](#) for details on JTAG pin information.

TABLE 8-5: JTAG PINS

Pin Name	Pin Number	Type	Description
TCK	C2	I, PU	JTAG Test Clock This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be pulled down with a 2 k Ω pull-down resistor in designs that require JTAG functionality. This pin should be tied low in designs that do not require JTAG functionality.
TDI	C3	I, PU	JTAG Test Data Serial Input Data Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
TDO	B2	O	JTAG Test Data Serial Output Data Serial test data from the PHY is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
TMS	D3	I, PU	JTAG Test Mode Select This input pin sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high to VDDIOCTRL in designs that do not require JTAG functionality.
$\overline{\text{TRST}}$	E3	I, PU	JTAG Reset This active-low input pin serves as an asynchronous Reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up (to VDDIOCTRL) resistor. Because of the internal pull-up, if the JTAG controller on the printed circuit board does not utilize the $\overline{\text{TRST}}$ signal, then the device will still function correctly when the $\overline{\text{TRST}}$ pin is floating. If the JTAG port of the PHY is not used on the printed circuit board, then this pin should be pulled down with a 2 k Ω pull-down resistor to ground.

9.0 MISCELLANEOUS

9.1 Reset

- The VSC8221 must be reset at power-up. One option is to hold **RESET** low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **RESET** low for a minimum of 2 ms after power-up. **RESET** is typically driven by a voltage monitor device or by the management processor or FPGA Reset circuit. See [Table 9-1](#) for more information on this pin.

TABLE 9-1: RESET PIN

Pin Name	Pin Number	Type	Description
RESET	A2	I	Device Reset. Active-low input that powers down the device and sets all register bits to their default state.

9.2 LED Pins

- The PHY has dedicated **LED** pins [2:0] to drive 3 LEDs directly. For power savings, all LED outputs can be configured to pulse at 5 kHz with a 20% duty cycle. All LED outputs are active-low and driven with 3.3V from the **VDD33A** power supply when deasserted.
- Because the 100BASE-FX mode uses 100BASE-T resources, its indications are those of the 100BASE-T mode.
- Four different functions have been assigned to each **LED** pin. Selection is done through CMODE hardware configuration or through MII Register 27 (1Bh) – LED Control Register. Refer to [Table 9-2](#) for **LED** pin information.

TABLE 9-2: LED PINS AND BASIC DEFAULT FUNCTION

Pin Name	Pin Number	Type	Description
LED0	B3	O	LED – Direct-Drive LED Outputs After Reset, these pins serve as the direct drive, low EMI, LED driver output pins. All LED pins are active-low and driven at a 3.3V logic-high through the VDD33A analog power supply. The function of each LED can be set by using hardware configuration CMODE3 pins and CMODE3[3] value. See Table 7-4 for more details on LED modes. Refer to MII Register 27 LED configuration bits.
LED1	A3	O	
LED2	A4	O	

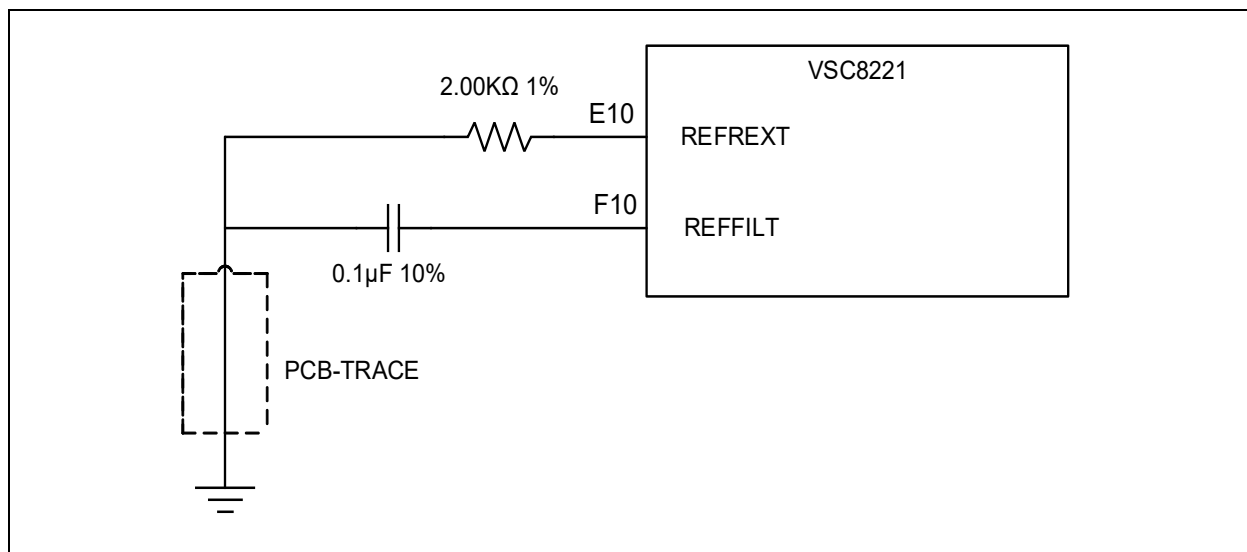
9.3 Analog Bias Pins for Voltage Reference

- The **REFREXT** pin (pin E10) on the VSC8221 should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0% and minimum 1/16W. This pin is used to set up critical bias currents for the Ethernet physical device.
- The **REFILT** pin (pin F10) on the VSC8221 should connect to the system ground through a 0.1 μF capacitor with 10% tolerance, NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane) as shown in [Figure 9-1](#). This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8221.
- Refer to [Table 9-3](#) for details on pin description. See [Figure 9-1](#) for the analog bias pin connections.

TABLE 9-3: BIASING PIN DETAILS

Pin Name	Pin Number	Type	Description
REFREXT	E10	ABIAS	REFREXT – Reference External Resistor Bias pin connects through external 2 k Ω (1%) resistor to system ground.
REFFILT	F10	ABIAS	REFFILT – Reference Filter Filters internal reference through an external 0.1 μ F (10%) capacitor to system ground

FIGURE 9-1: VOLTAGE REFERENCE SCHEMATIC



9.4 MODDEF0/CLKOUT Pin

- This pin is used as either a PHY ready indicator output or a 125 MHz clock output. See [Table 9-4](#) for more information on this pin.

TABLE 9-4: MODDEF0/CLKOUT PIN DETAILS

Pin Name	Pin Number	Type	Description
MODDEF0/ CLKOUT	A1	O	MODDEF0 – Active Low PHY Ready indicator Output Use the CMODE configuration pin to set CMODE1[3] =0 or set the MII Register 21E.15=1 to SFP mode. CLKOUT – 125 MHz Clock Output Use the CMODE configuration pin to set CMODE1[3] =1 or set MII Register 21E.15=0 to IEEE mode. The PHY drives a 125 MHz clock output after the PHY startup sequence has completed. This clock can be disabled by clearing MII Register 18.0. The voltage levels of this clock are determined by the VDDIO power supply.

9.5 TXDIS/SRESET Pin

- When this pin is asserted, it places the PHY in a Low-Power state, which includes disabling the SerDes interface. Although the device is powered down, non-volatile Serial Management Interface registers retain their values. See [Table 9-5](#) for more information on this pin.

TABLE 9-5: TXDIS/SRESET PIN

Pin Name	Pin Number	Type	Description
<u>TXDIS/</u> <u>SRESET</u>	G8	IPU	TXDIS – Transmit Disable Use the CMODE configuration pin to set CMODE1[3] =0 or set MII Register 21E.15=1 to SFP mode. When TXDIS/SRESET is active-high, the pin behaves like TXDIS . SRESET –Software Reset Use the CMODE configuration pin to set CMODE1[3] =1 or set MII Register 21E.15=0 to IEEE mode. When TXDIS/SRESET is active-low, the pin behaves like SRESET .

9.6 Unused and No-Connection Pins

- The NC pins (pins C1, D1, E1, F1, G1, H1, J1, K1, D2, E2, F2, G2, H2, J2, K2, H3, J3, K3, J4, K4, H5, J5, K5, J6, and K6) are unconnected and must be left floating.

9.7 General External Pull-Up and Pull-Down Resistors

- If no pull-up resistor value is specified, it is recommended to use a 4.7 kΩ resistor.
- If no pull-down resistor value is specified, it is recommended to use a 1 kΩ or 4.7 kΩ resistor.

NOTES:

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	✓	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current and Power Requirements"	Refer to Table 3-1 to ensure that the power pins are correct. Select the correct power components with at least about 25% to 30% margin based on system configuration. Select one of Table 3-2 , Table 3-3 , Table 3-4 , Table 3-5 , Table 3-6 , Table 3-7 , and Table 3-8 as a reference for the system power design.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection, decoupling capacitors, bulk capacitors, and filtering.		
	Section 3.4, "Bulk Decoupling Capacitors"	If doing a PCB layout, check this section for the bulk decoupling capacitors required.		
Section 4.0, "Twisted Pair Media Interface (CAT5)"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pin connections for the Ethernet port circuit design based on product design requirements. Select the design based on Figure 4-1 and Figure 4-2 .		
	Section 4.2, "10/100/1000 Magnetics and RJ45 Connector Connection"	Verify the magnetics and the common-mode capacitor connections based on Figure 4-1 and Figure 4-2 .		
	Section 4.3, "PCB Layout Considerations"	Use this section for PCB layout design reference, and check if the Gigabit copper port PCB layout request is met.		
Section 5.0, "SGMII/SerDes MAC Interface"	Section 5.1, "SGMII/SerDes MAC Pins and Connection"	Refer to Figure 5-1 to make sure you are using the correct pins for the SGMII/SerDes MAC interface in design.		
	Section 5.2, "SGMII/SerDes MAC"	Read this section and refer to Figure 5-1 for SGMII/SerDes MAC interface to connect to an external SGMII or SerDes MAC in design.		
	Section 5.3, "SerDes MAC Interface to SFP"	Read this section and refer to Table 5-2 and Figure 5-2 for SerDes MAC interface to connect to one 1000Base-X SFP or connect to one 1000Base-T SFP in design.		
	Section 5.4, "SGMII/SerDes MAC Interface Design Rules"	Read this section for SGMII/SerDes MAC interface PCB design reference.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Device Clocks"	Section 6.1, "Reference Clock"	Refer to Table 6-1 to select the reference clock circuit-related pins in the design.		
	Section 6.2, "25 MHz Crystal Circuit"	Refer to Figure 6-1 for 25 MHz crystal clock circuit design and make sure to use correct strapping for PLLMODE pin and OSCDIS pin.		
	Section 6.3, "25 MHz Oscillator Circuit"	Refer to Figure 6-2 for 25 MHz oscillator clock circuit design and make sure to use the correct strapping for PLLMODE pin and OSCDIS pin.		
	Section 6.4, "125 MHz Oscillator Circuit"	Refer to Figure 6-3 for 125 MHz oscillator clock circuit design and make sure to use correct strapping for PLLMODE pin and OSCDIS pin.		
Section 7.0, "Hardware Configuration Using CMODE Pins"	Section 7.1, "CMODE Pins and Description"	Refer to Table 7-1 to make sure that the correct CMODE pin numbers in the hardware configuration are used.		
	Section 7.2, "Select Mode Pins Pull-Up and Pull-Down Resistor Value for System Design"	Refer to Table 7-2 to select the correct pull-up and pull-down resistor values for each CMODE pin to get the needed 4-bit value for each CMODE pin.		
	Section 7.3, "CMODE Bits"	Refer to Table 7-2 , Table 7-3 , and Table 7-4 to perform the hardware configuration based on system design.		
Section 8.0, "Digital Interface"	Section 8.1, "Dual Mode Serial Management Interface (SMI)"	Refer to Table 8-1 for SMI pin description and verify the correct use of pin numbers.		
	Section 8.1.1, "PHY Register Access with SMI in MSA Mode"	Refer to Table 8-2 for SMI in MSA mode pin description if SMI in MSA mode is selected.		
	Section 8.1.2, "PHY Register Access with SMI in IEEE Mode"	Refer to Table 8-3 for SMI in IEEE mode pin description if SMI in IEEE mode is selected.		
	Section 8.2, "EEPROM Interface"	Refer to Table 8-4 for EEPROM interface pin description. Make sure to use the correct pin numbers, and check if there is a pull-up resistor on EEDAT pin if using EEPROM.		
	Section 8.3, "JTAG Interface"	Refer to Table 8-5 and the description in this section for all JTAG pins in the circuit design.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Miscellaneous"	Section 9.1, "Reset"	Refer to Table 9-1 for using the correct RESET pin and see if the designed Reset circuit meets the Reset time requirement.		
	Section 9.2, "LED Pins"	Check if the correct LED pins are used based on Table 9-2 and refer to Table 7-4 for CMODE3[3] settings based on LED function required in the system design.		
	Section 9.3, "Analog Bias Pins for Voltage Reference"	Check if the correct pull-down resistor value is used for the REFREXT pin and if the correct pull-down capacitor value is used for REFFILT pin based on Table 9-3 and Figure 9-1 .		
	Section 9.4, "MODDEF0/CLKOUT Pin"	Refer Table 9-4 to see if this pin is used correctly in the design.		
	Section 9.5, "TXDIS/SRESET Pin"	Refer Table 9-5 to see if this pin is used correctly in the design.		
	Section 9.6, "Unused and No-Connection Pins"	Verify if all unused pins and NC pins are unconnected.		
	Section 9.7, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004409A (02-08-22)	Initial release	

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