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DOCUMENT DESCRIPTION
Component Placement Checklist for the LAN8720I, 24-pin QFN Package

 	SMSC 80 Arkay Drive Hauppauge, New York 11788	
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Component Placement Checklist for LAN8720I

Information Particular for the 24-pin QFN Package

LAN8720I QFN Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXP, pin 21) as close to the LAN8720I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXN, pin 20) as close to the LAN8720I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.
3. Place the 49.9 Ω RX termination pull-up (RXP, pin 23) as close to the LAN8720I as possible.
4. Place the 49.9 Ω RX termination pull-up (RXN, pin 22) as close to the LAN8720I as possible.
5. See Figure No. 1 for the placement of the termination resistors for the differential pairs for the LAN8720I Phy. These resistors are R1, R2, R3 & R4 in Figure No. 1.
6. Place the four optional, low-valued, common mode capacitors for each differential signal as close as possible to the magnetics. They should be placed as to create the smallest possible stub. These caps are C1, C2, C3 & C4 in Figure No. 1.
7. All the components discussed in this section should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design.

LAN8720I QFN Magnetics:

1. Place the 0.022 μ F TX Channel Center Tap termination capacitor as close to the magnetics as possible.
2. Place the 75 Ω cable side center tap termination resistors and the 1000 pF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.
3. See Figure No. 1 below for the placement of the center tap termination components for the LAN8720I Phy. These resistors/capacitors are C5, R6, R7 & C6 in Figure No. 1.
4. C5 in this section should be considered a critical component. To ensure the best signal integrity and good EMI performance, this critical component should be placed on the component side of the PCB. This will ensure that this component will be referenced to a contiguous ground plane reference on Layer 2 of the design.
5. R6, R7 & C6 may be considered non-critical components. These components make up part of the high voltage barrier for the Ethernet front end. The best location for these components is typically on the solder side of the PCB. They should be placed such that none of the resultant routing crosses the differential pairs. These components have both ESD and EMI implications.

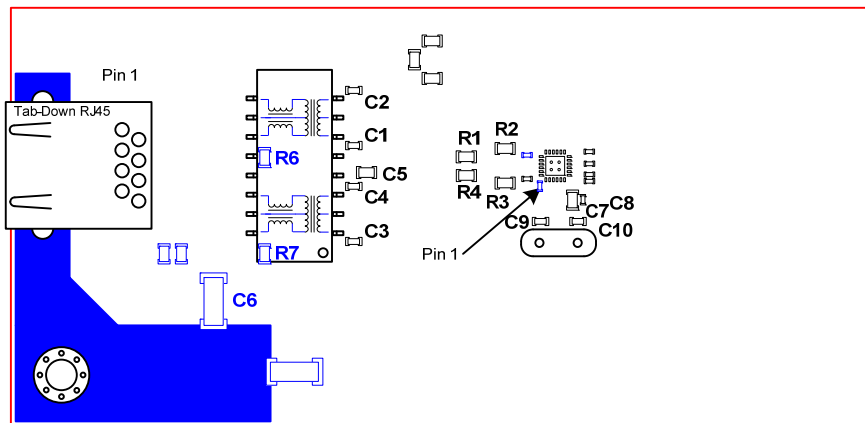


Figure No. 1

RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN8720I QFN as close together as possible.
2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN8720I QFN.
3. See Figure No. 2 below for minimum distance requirements related to the RJ45 connector, the magnetics and the LAN8720I Phy.
4. The distance from the RJ45 connector to the magnetics should be 0.50" at a minimum and 0.75" at a maximum.
5. The distance from the magnetics to the LAN8720I should be 1.0" at a minimum and 3.0" at a maximum.
6. Select and place the magnetics as to set up the best routing scheme from the LAN8720I QFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.
7. Place the Unused Wire Pair termination resistors and the 1000 μ F, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.
8. The Unused Wire Pair termination resistors may be considered as non-critical components. These components make up part of the high voltage barrier for the Ethernet front end. The best location for these components is typically the solder side of the PCB. They should be placed such that none of the resultant routing crosses the differential pairs. These components have both ESD and EMI implications.
9. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

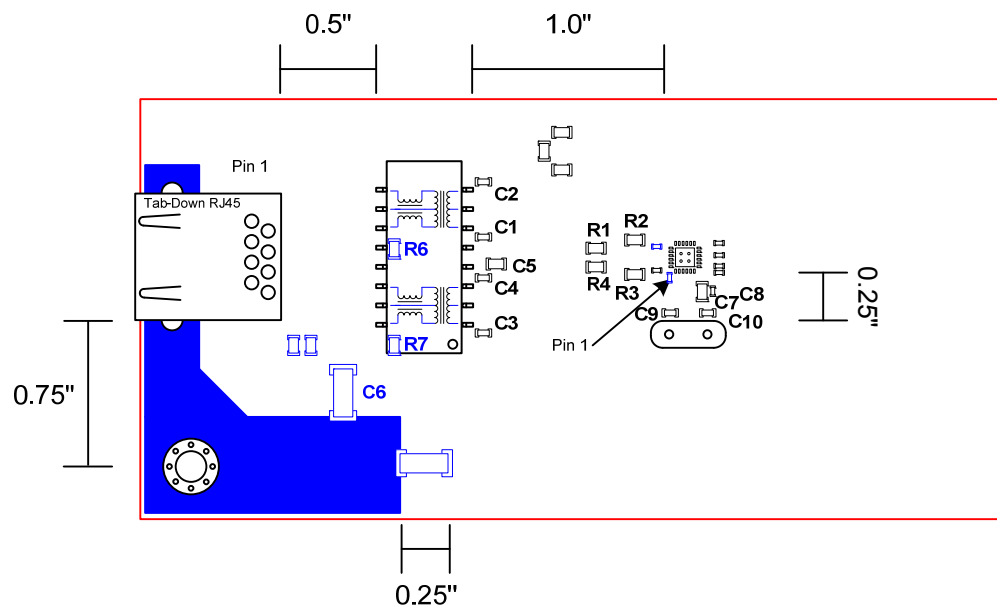


Figure No. 2

Power Supply Connections:

1. Place the (1) VDDIO decoupling capacitor for the LAN8720I QFN as close to the power pin as possible. Using an SMD_0402 package will make this task easier.
2. Place the (2) VDD1A & VDD2A decoupling capacitors for the LAN8720I QFN as close to each separate power pin as possible. Using an SMD_0402 package will make this task easier.
3. Decoupling capacitors, in general, are best placed on the component side of the PCB. This should allow the board designer to minimize the use of vias and provide a short, direct copper connection from the capacitor to the power pin.

Ground Connections:

1. There are no component placement issues associated with the LAN8720I QFN ground connections. The LAN8720I has an Exposed Die Paddle ground connection on the package bottom. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

VDDCR:

1. VDDCR (pin 6) requires a 470 pF decoupling capacitor and a low ESR 1.0 μ F bulk capacitor placed as close as possible to pin 6.
2. These caps are shown as C7 & C8 in Figure No. 3 below.
3. These bulking and bypassing capacitors, in general, are best placed on the component side of the PCB. This should allow the board designer to minimize the use of vias and provide a short, direct copper connection from the capacitor to the power pin.

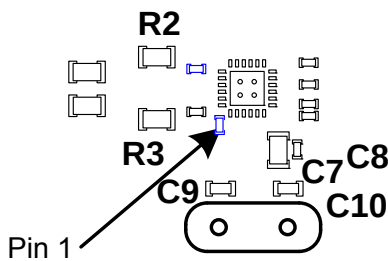


Figure No. 3

Crystal Connections:

1. Place the 25.000 MHz crystal and the associated 15 – 33 pF capacitors as close together as possible and as close to the LAN8720I QFN (XTAL1, pin 5 & XTAL2, pin 4) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.). Refer to Figure No. 3 for crystal component placement (C9 & C10).
2. See Figure No. 2 for distance requirements related to the LAN8720I Phy. The crystal and associated components should be located within 0.25" of the LAN8720I.
3. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all crystal components are referenced to the same reference plane.
4. The 33 ohm series termination for the REFCLKO signal should be placed as close as possible to pin 14 of the LAN8720I.

Clock Oscillator Connections:

1. Place the 50 MHz clock oscillator approximately half-way between the LAN8720I and the RMII MAC in the application. This should ensure relatively matched clock runs to each.
2. Place any series terminations for splitting the 50 MHz clock as close as possible to the clock oscillator in the design.
3. As controlled by the different component placements, the two resultant clock traces should be matched to within 0.10" and have an overall trace length of less than 6.0".

MAC REFCLK Connections:

1. Place the series termination for the 50 MHz REFCLK clock as close as possible to the MAC in the design.

RBIAS Resistor:

1. Place the RBIAS resistor as close to pin 24 of the LAN8720I QFN as possible.
2. The RBIAS resistor should be considered a critical component. This critical component should be placed on the component side of the PCB. This will ensure that this component will be referenced to a contiguous ground plane reference on Layer 2 of the design.

RMII Interface:

1. When physically placing the LAN8720I in an RMII application, the designer should be aware of the relative trace lengths determined by the relationship of the Phy and the MAC in the application. By placing the MAC too far away from the LAN8720I, this may result in operational problems associated with excessive trace lengths.
2. The designer has some latitude in the placement of the LAN8720I with respect to the magnetics; see Figure 2. This should allow for some adjustment on the Phy-to-MAC RMII interface, should this be necessary. By moving the Phy farther away from the magnetics, the RMII interface can be shortened.
3. SMSC recommends the final RMII interface trace lengths to remain under 6" long. When compared to the MII interface, due to the higher operational frequencies involved, the trace lengths in the RMII interface are much more critical.

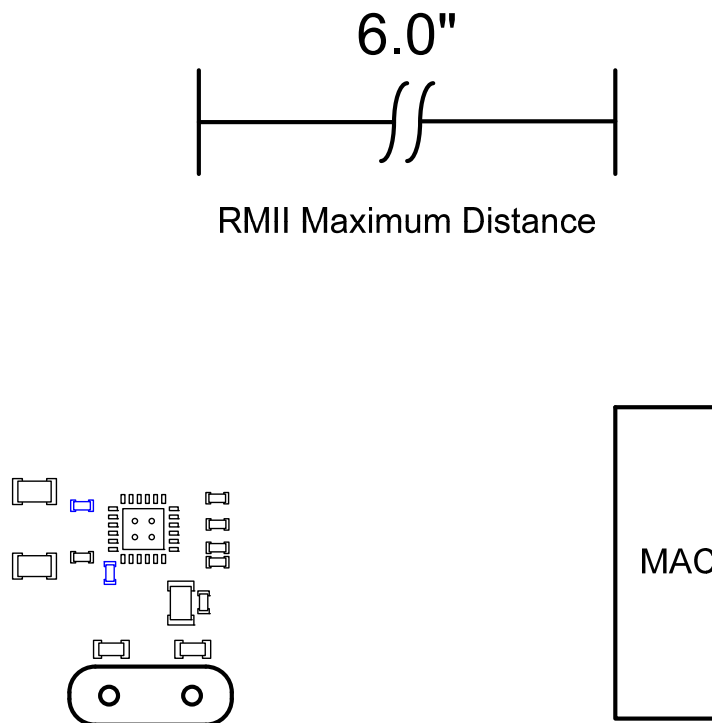


Figure No. 4

RMII Series Terminations:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.
2. The RMII Series Terminations should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design. This will also minimize the use of vias in routing these signals.

Required External Pull-ups:

1. Typically, there are no component placement issues associated with the LAN8720I QFN External Pull-up connections.

Mode Pins:

1. Since the MODE Pins are shared with the RXD[1..0] and the CRS_DV signals of the LAN8720I, any resistor used for termination for the power-on-reset MODE selection, should be placed on the component side of the PCB. This will minimize vias and ensure the reference plane remains constant.
2. Any stub added to the RMII lines due to MODE pin terminations should be kept to a minimum.

Phy Address Pins:

1. Phy Address pin PHYAD0 should be considered critical. This pin is shared with the RX_ER function of the RMII interface. Any resistor used for termination for the power-on-reset Phy Address selection, should be placed on the component side of the PCB. This will minimize vias and ensure the reference plane remains constant for this RMII signal.
2. Any stub added to the RMII line due to Phy Address pin terminations should be kept to a minimum.

LED Pins:

1. There are no component placement issues associated with the LAN8720I LED pins.

Interrupt Functionality:

1. There are no component placement issues associated with the LAN8720I Interrupt Functionality.

Miscellaneous:

1. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes. Typically, this component is placed on the back of the PCB. This component has both ESD and EMI implications.
2. Bulk capacitors for each power plane can reside anywhere on the plane they serve.