AN3773

Dual Row Quad Flat No-Lead Package (DRQFN) Surface Mount Assembly

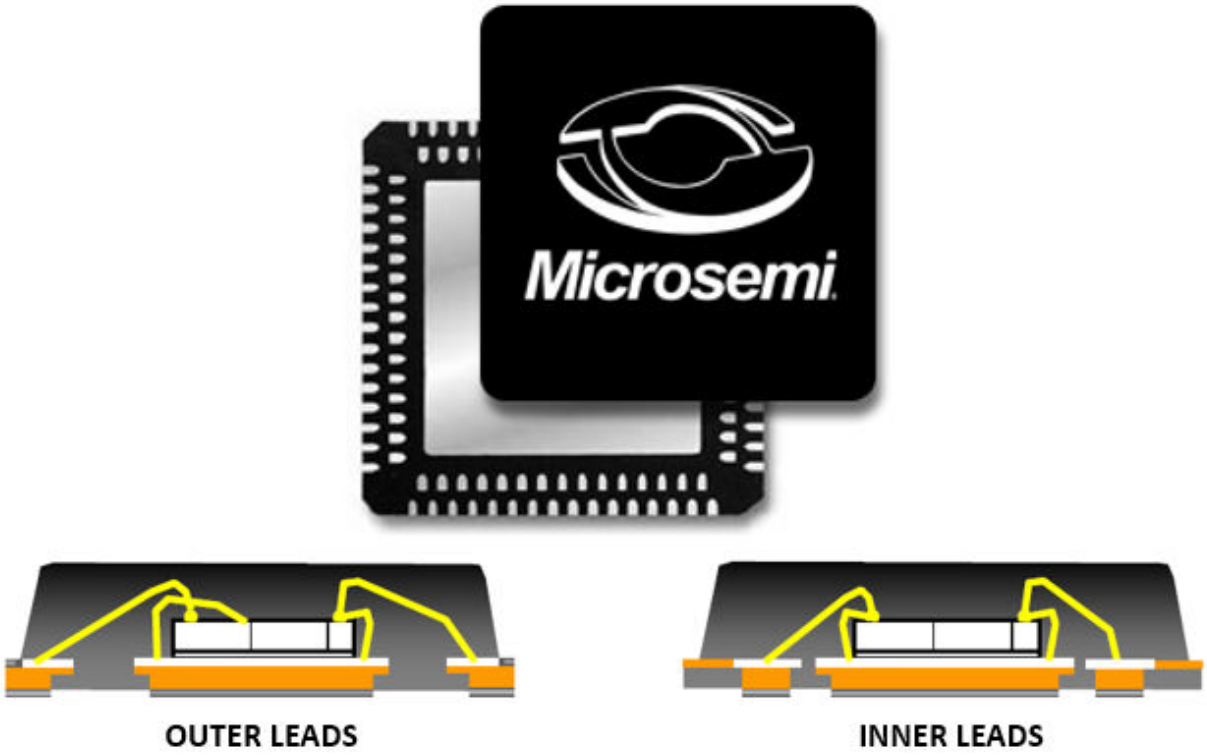
Introduction

The purpose of this document is to provide surface mount guidelines for the 13 mm x 13 mm, 172-lead Dual Row Quad Flat No-Lead Package (DRQFN) used for Microsemi's Ethernet switch products VSC7511 and VSC7512.

The DRQFN is a near chip-scale package (CSP), plastic-encapsulated with a copper leadframe substrate. This package extends the leadless, single row quad flat no-leads (QFN) package where electrical contact to the printed circuit board (PCB) is made by soldering lands on the bottom surface of the package to the PCB with an additional row of leads on the package. The exposed die attach paddle on the bottom is directly attached to the PCB, efficiently conducting heat and providing a stable ground through downbonds and electrical connections through conductive die attach material.

The following figure shows the package cross-section.

Figure 1. DRQFN Cross-Section



For optimum thermal, electrical, and board-level performance, special design considerations are required for proper PCB design and package mounting. For enhanced thermal, electrical, and board-level performance, the exposed pad on the package needs to be soldered to the PCB using a corresponding thermal pad on the PCB. Furthermore, for proper heat conduction through the PCB, thermal vias need to be incorporated in the thermal pad design. The PCB footprint design needs to be considered from dimensional tolerance due to package, PCB, and assembly.

Table of Contents

1. PCB Design

The following section includes detailed PCB land pattern information, recommended escape routing, and center exposed pad layout guidelines. Stencil design information and the package rework procure are described in Surface Mount Guidelines, page 7.

Note:
The reference board design VSC5634EV (Ocelot Unmanaged Reference Design) does not use this recommended footprint, as it was not available when the reference board was designed.

1.1 PCB Land Pattern

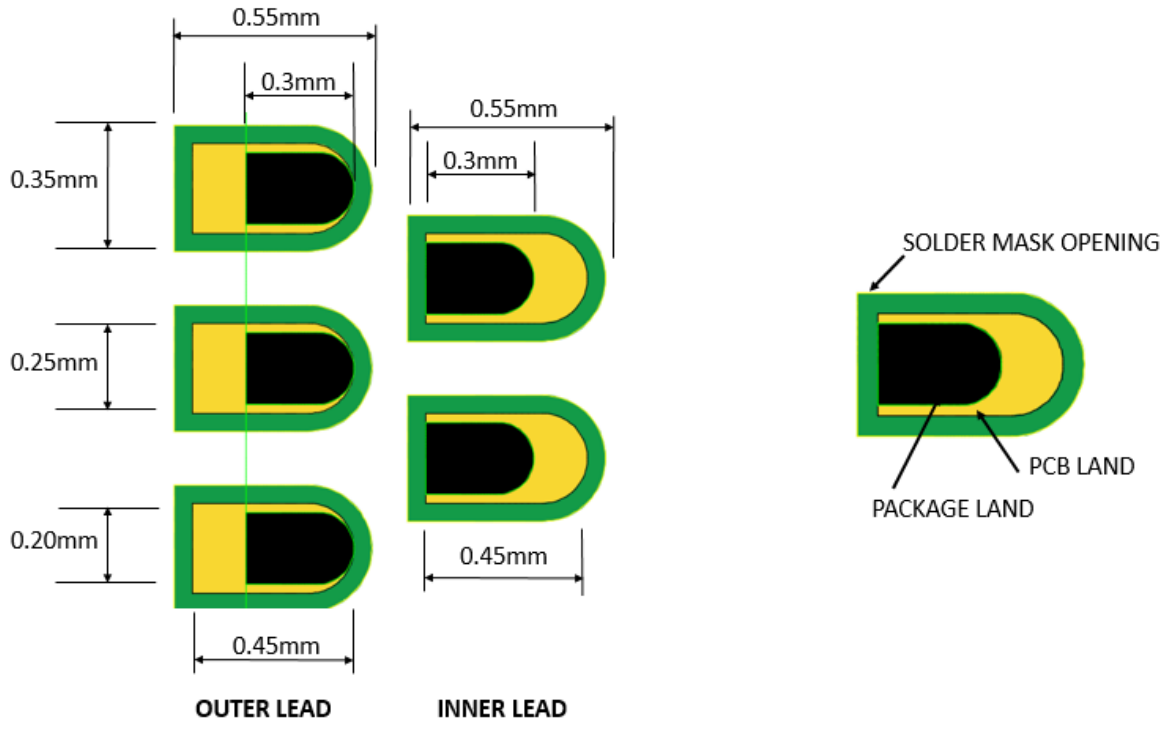
The DRQFN has two rows of lands. The package lands are 0.2 mm x 0.3 mm. The pitch of the lands is 0.5 mm, and is the same dimension in both the X and Y directions.

The PCB lands are 0.25 mm x 0.45 mm. The dimensions are larger than the package land, and allow for adequate solder fillet to be formed on the edges of the leads, which is necessary for better solder joint reliability.

There are two basic types of PCB land pads: non-solder mask defined (NSMD) and solder mask defined (SMD). NSMD pads are recommended because of the tighter dimensional controls of the copper etching process than the solder masking process. NSMD pads also improve solder joint reliability because solder wraps around the side of the metal pads. The clearance of the solder mask opening and PCB lands is 50 µm.

The following illustration shows the land dimensions.

Figure 1-1. Land Dimensions



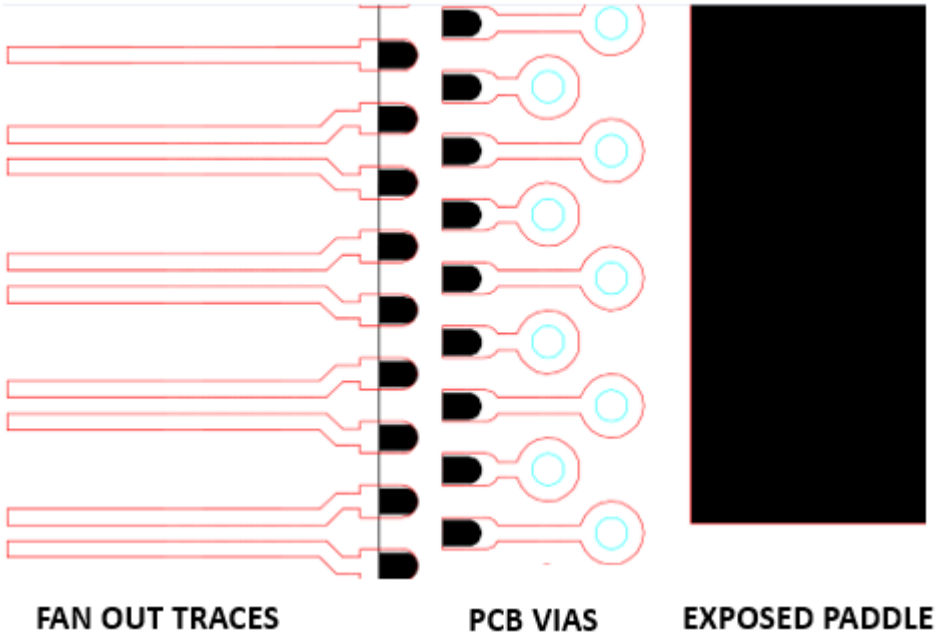
1.2 Inner Lands Routing

The land pitch of these packages is 0.5 mm. It is not possible to route between lands without using advanced PCB design rules.

A fan out/fan in approach can be used for the outer and inner lands using standard PCB design rules.

The following illustration shows the inner and outer land routing on the PCB.

Figure 1-2. Escape Routing



The outer lands are directly routed out on the top PCB layer. The inner row lands are routed through vias to inner layers of the PCB.The vias are staggered between the inner lands and exposed pad. Do not align the vias- this will break up the inner layer of the PCB.

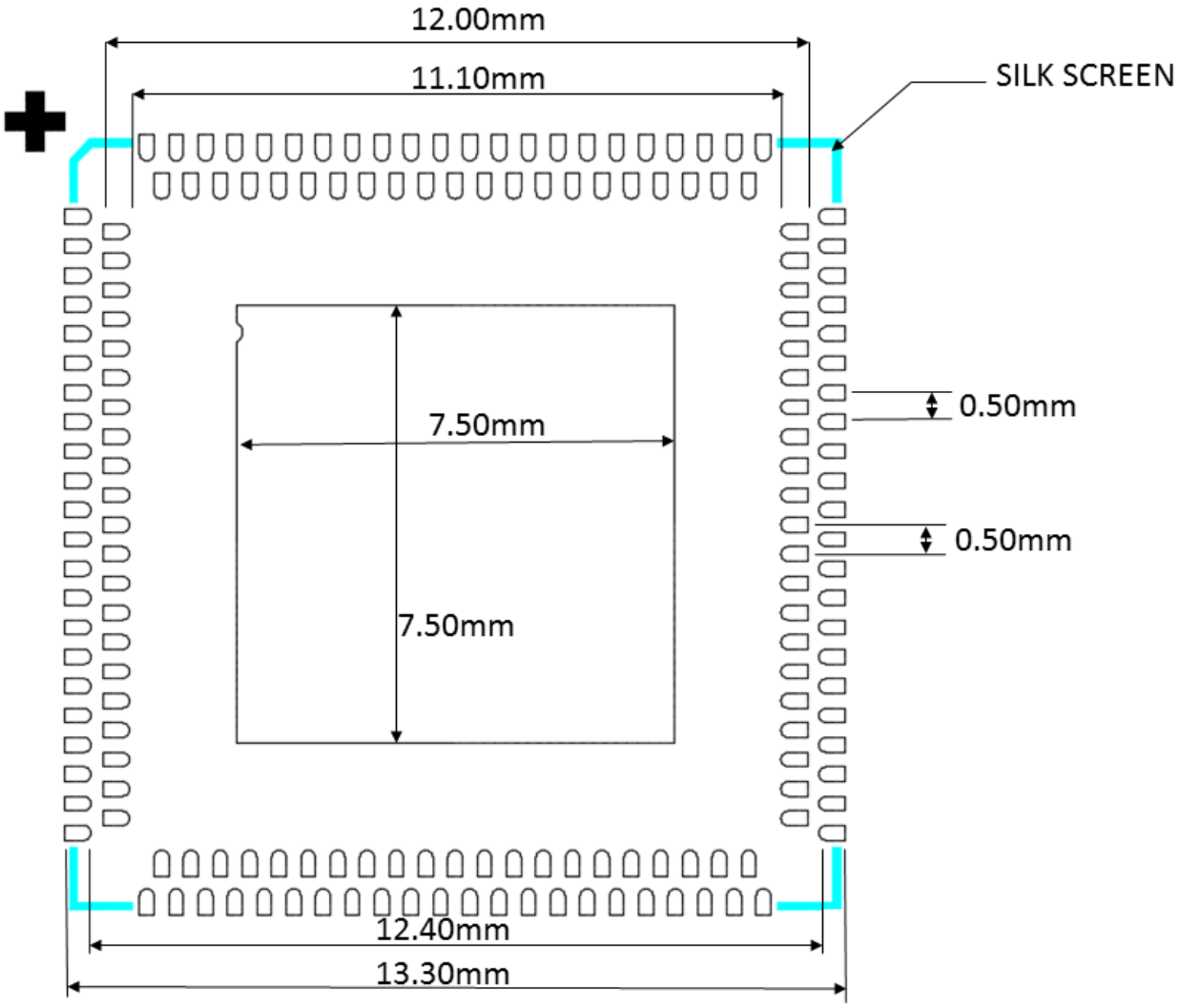
1.3 Center Exposed Pad

The center exposed pad metal should be 7.5 mm x 7.5 mm. For maximum heat dissipation, the solder mask should not be on the exposed pad.

It is recommended that the thermal pad on the exposed pad be NSMD to allow a solder fillet to form on the exposed pad edges and improve solder joint reliability. The solder mask opening of the exposed pad is 7.63 mm x 7.63 mm.

The dimensions of the inner and outer lands and the exposed paddle of the PCB are shown in the following illustration.

Figure 1-3. PCB Land Pattern

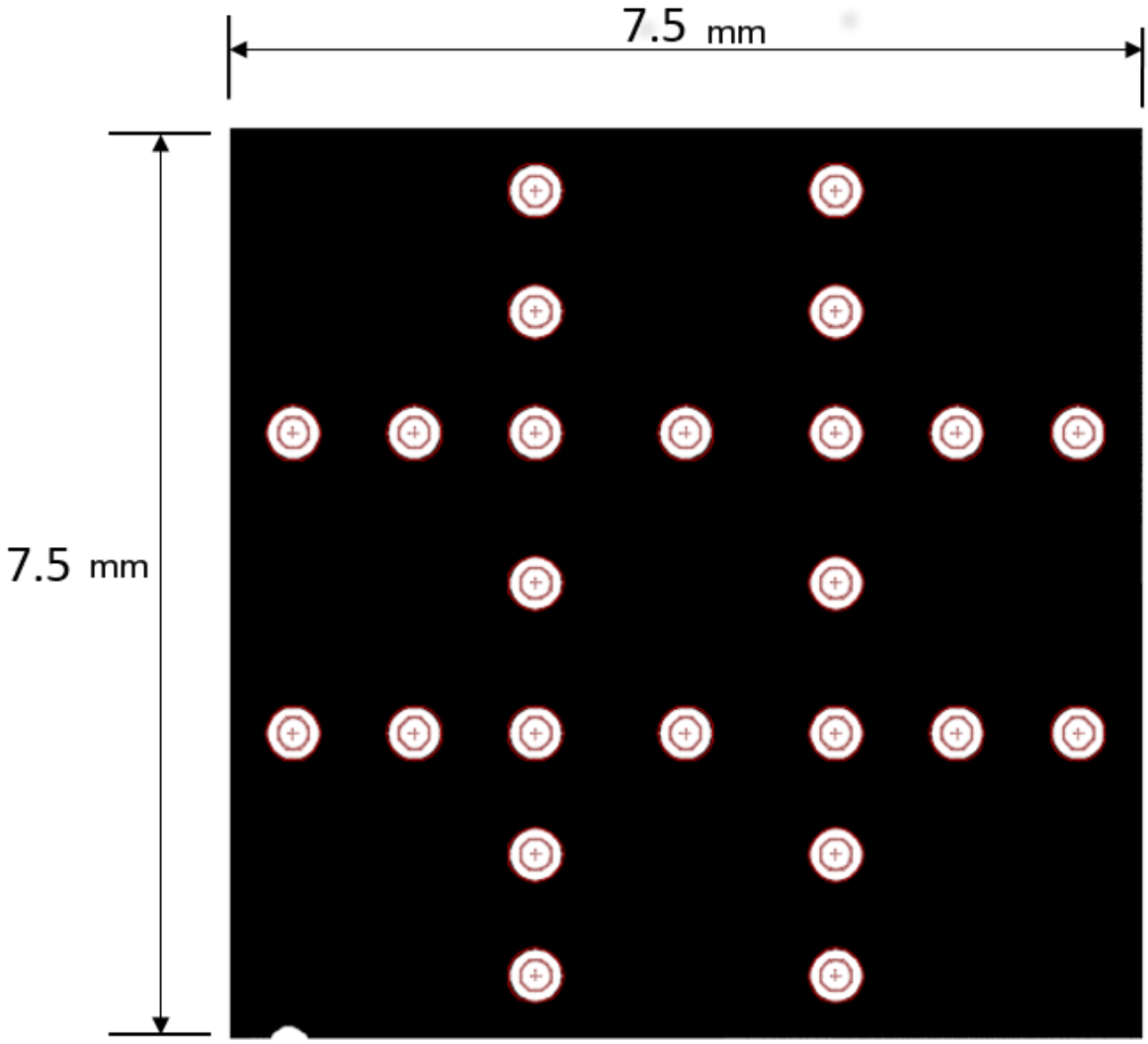


1.4 Thermal Vias

In order to take full advantage of the DRQFN thermal performance, thermal vias are needed to provide a thermal path from the die to the inner/bottom layers of the PCB. Thermal vias should be 0.254 mm in diameter and spaced at 1 mm pitch. The recommended via plating is 1 oz copper in order to maximize the thermal conduction path through the PCB.

It is recommended that the thermal via be through-hole vias. The thermal via layout in the following illustration has 24 through-hole vias arranged in two rows/columns.

Figure 1-4. Thermal Vias Placed on Center Exposed Pad



More vias can be added if design rules allow. Care must be taken so that the stencil opening does not overlap with the through-hole vias. If tenting is required, then it's recommended for this to be on the top side of the PCB.

2. Surface Mount Guidelines

A reliable surface mount of the DRQFN depends on an optimal stencil design and paste printing. Care must be taken to form reliable solder joints on the outer leads and inner lands, as well as to minimize voids on the large exposed pad.

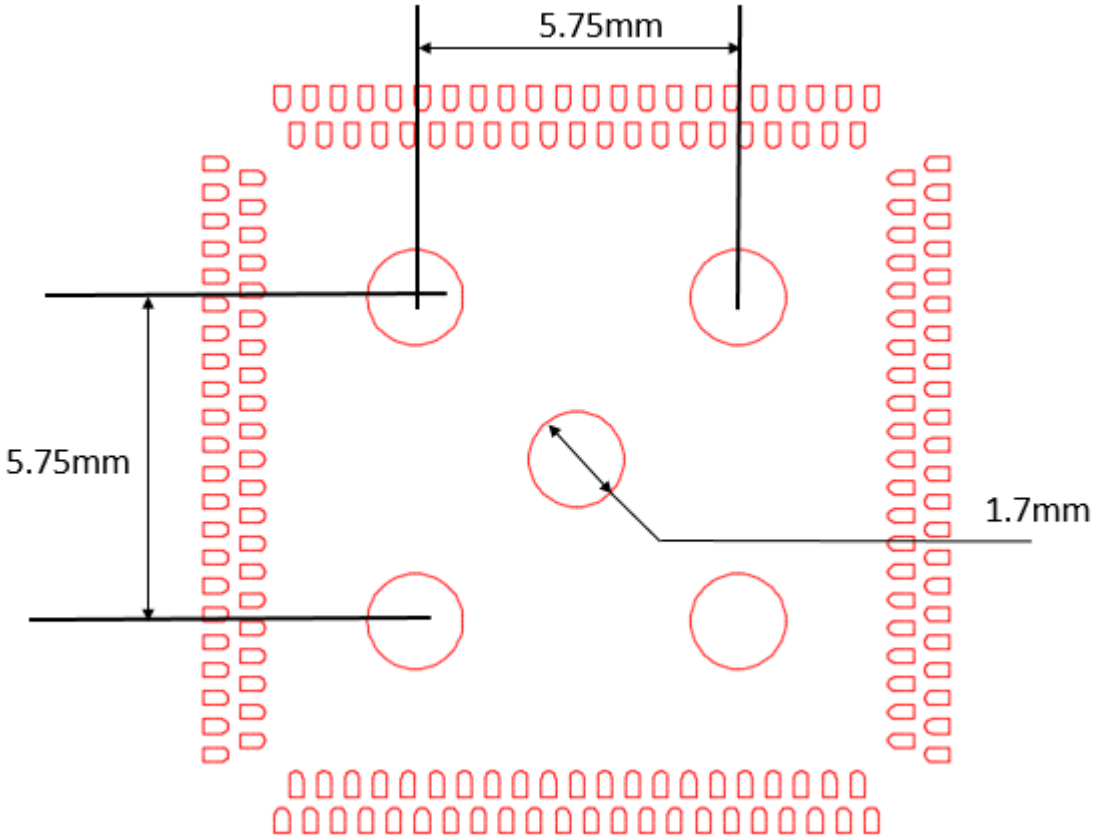
2.1 Stencil Design

The stencil apertures for the inner and outer lands have a 1:1 ratio to the PCB lands. The apertures have rounded corners to minimize clogging. The center paddle aperture has five round openings, which are 1.7 mm in diameter. The solder paste coverage on the center paddle is low (15–25%), which reduces the floating effects of the perimeter lands.

The stencil should be laser-cut and electro-polished to facilitate paste release. The stencil aperture tolerance should be tightly controlled due to the small pitch. There should be a positive taper with a bottom stencil opening that is larger than the top. The recommended stencil thickness is 125 µm (5 mils) to ensure a sufficient standoff height (>50 µm) for good solder joint reliability.

Lead-free solder paste (Sn/Ag/Cu—"no clean," type 3 or type 4) is recommended. Careful process development is recommended because surface mount processes vary across companies.

Figure 2-1. Stencil Design

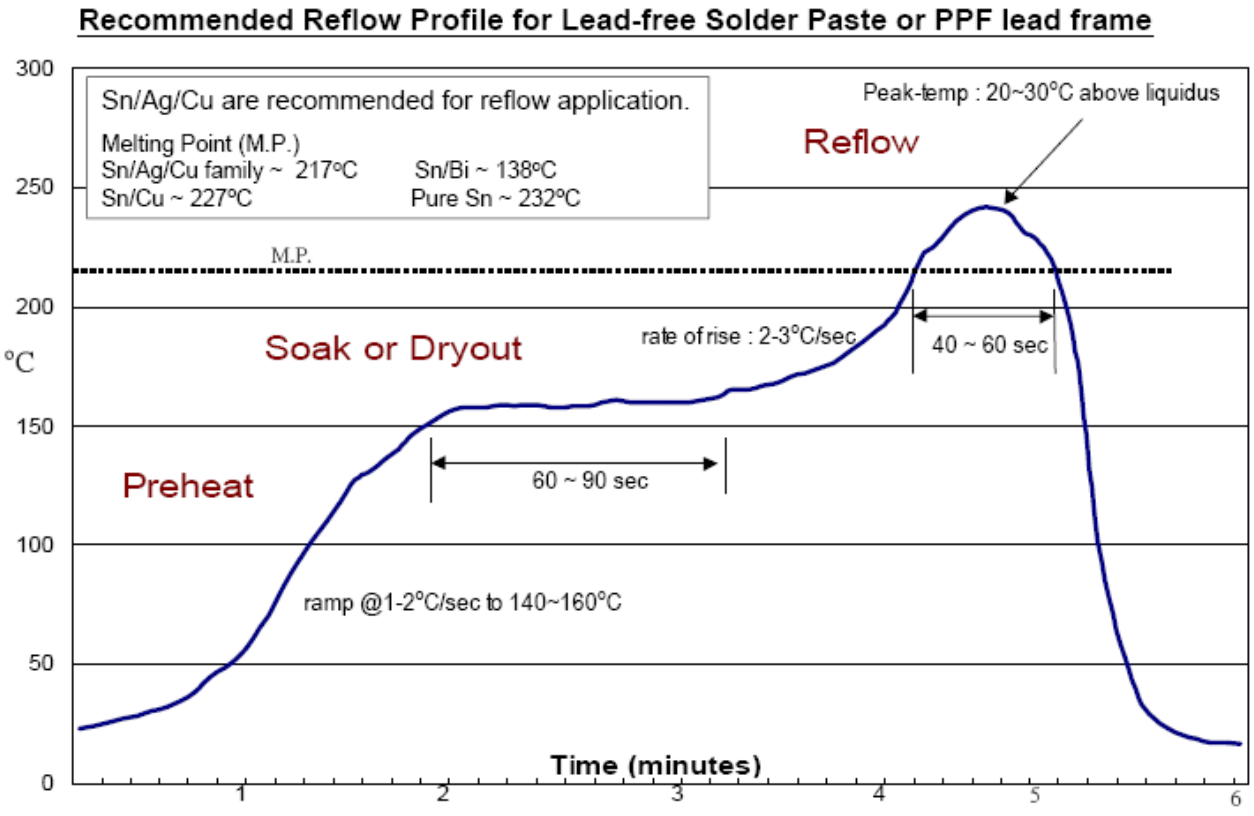


2.2 Reflow Profile

Reflow profile and peak temperatures have a strong influence on the void formation after SMT. The solder paste supplier's recommended reflow profile should be followed because it is specific to the flux formulation contained with the solder paste. Use a forced convection reflow oven with temperature uniformity of less than ±5 °C.

The following illustration shows a typical reflow profile using Sn/Ag/Cu solder paste.

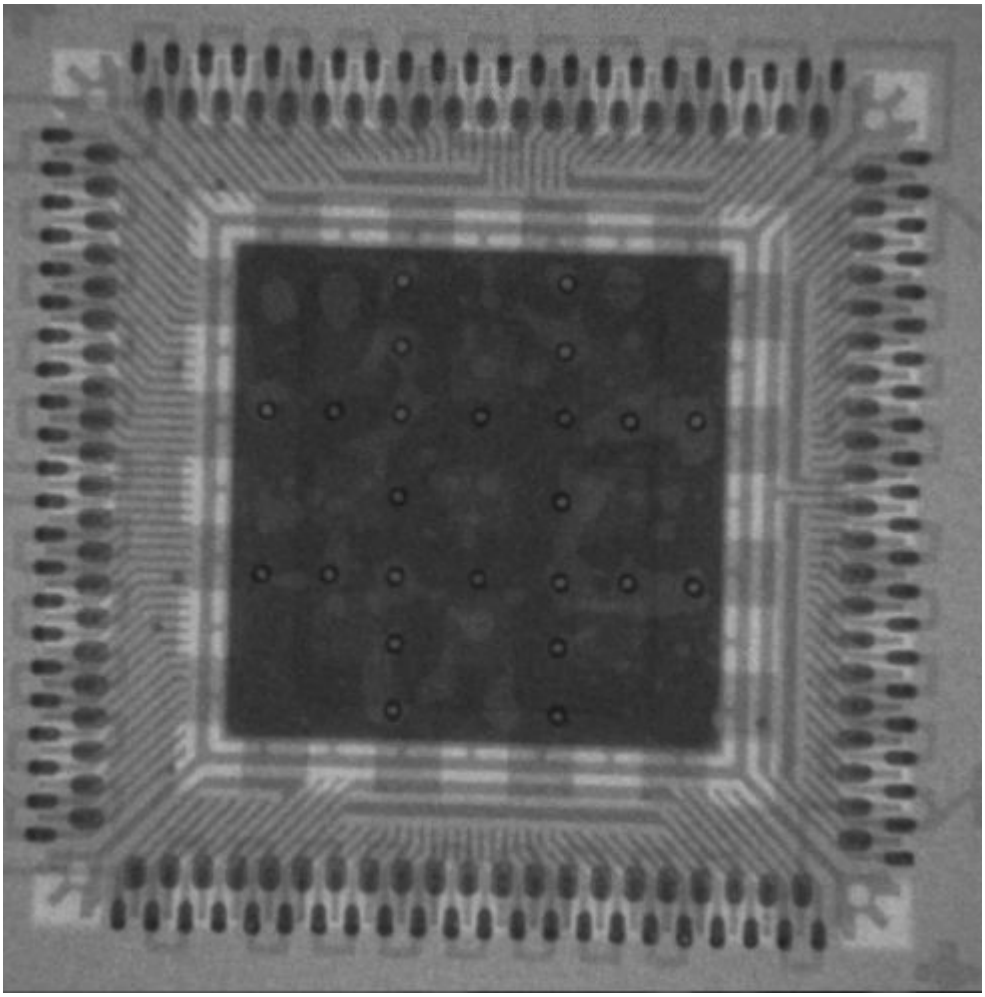
Figure 2-2. Typical Reflow Profile Using Sn/Ag/Cu Solder Paste



2.3 Post Reflow Inspection

Post reflow inspection consists of x-ray sampling and side view visual inspection. Transmission x-rays show the voids under the exposed paddle and any evidence of lead shorts or package misalignment. The following illustration shows an acceptable x-ray image of the DRQFN.

Figure 2-3. Transmission X-Ray

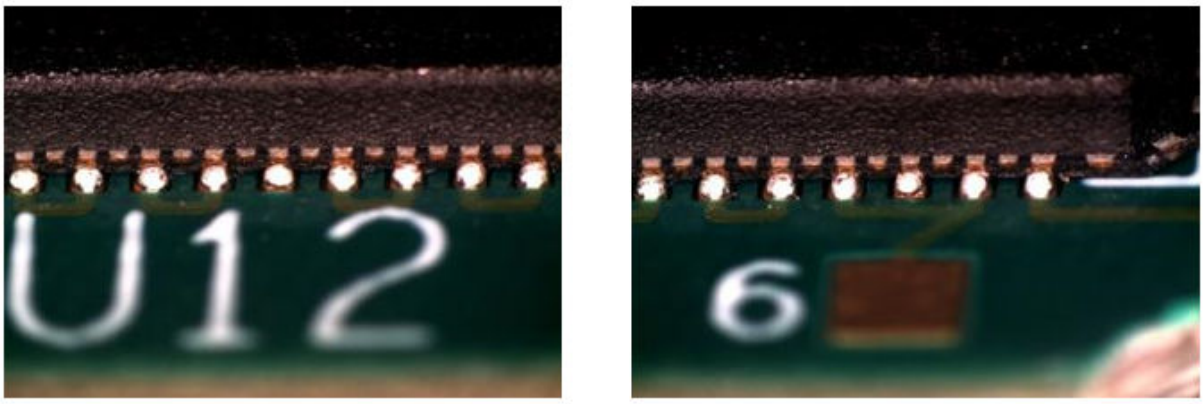


The inner and outer lands have minimal voids. The inner lands and exposed paddle can only be inspected by x-ray.The outer lands can be inspected by x-ray and visual inspection.

The voids spread around the paddle area are unavoidable due to the large exposed pad area, but they do not result in any thermal or electrical performance degradation. Any singular large void should be avoided because it indicates insufficient solder and/or SMT issues (pick and place force, outgassing, clogged stencil).

The following illustration shows a side view visual inspection of the outside solder joints with a solder fillet.

Figure 2-4. Outside Solder Joint (side view)



2.4 Rework Procedure

Any retouching of solder joint is limited to the outside lands. For defects at the inner lands and the exposed paddle, the whole package needs to be removed and reworked, as outlined in the following steps. Prior to any rework, the PCB should be baked for at least 4 hours at 125 °C to remove any moisture.

2.4.1 Package Removal

Remove the package from the PCB by reflowing the solder joints. The reflow profile can be the same one that was used to attach the package, but the time above the liquidus can be reduced as long as the reflow is complete. In the removal process, it's recommended that the board be heated from the bottom side using convective heaters and that hot air be used on the top side. Special nozzles should be used to direct the heat to the removal package. Heating of adjacent components on the PCB should be minimized. Excessive airflow should also be minimized because it will cause the package to skew.

Once the solder joints have reflowed, the package can be removed.

2.4.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. A combination of a blade-style conductive tool and desoldering braid can be used to remove the residual solder. Blade width should match maximum package footprint width and the blade temperature should be low enough to not cause any PCB damage. Once the residual solder is removed, the PCB lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and the solder paste manufacturer's recommendations should be followed.

2.4.3 Solder Paste Application

A miniature stencil specific to the package footprint is used for the solder paste printing. The stencil aperture should be aligned with the lands under 50x–100x magnification. The stencil is lowered onto the PCB and the paste is deposited with a small squeegee blade. Alternatively, the mini stencil can print paste directly on the package lands.

2.4.4 Package Placement

Package placement on the PCB is performed using a split-beam optical system to align the package. The alignment should be done at 50x–100x magnification. The alignment machine should allow fine adjustment in the x, y, and rotational axes.

2.4.5 Package Reflow

The reflow profile used for the original attachment should be used for the reworked package.

3. Revision History

Revision	Date	Description
Rev A	December 2020	The following is the summary of changes in this revision of the document: • The document was migrated to MCHP template. • The document number has been changed to DS00003773A from VPPD-04308. • The application note number has been changed to AN3773 from AN1193.

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