AN1920

Microchip LAN9252 EEPROM Configuration and Programming

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1.0 INTRODUCTION

The Microchip LAN9252 is a 2/3-port EtherCAT® Slave Controller (ESC) with dual integrated Ethernet PHYs. The LAN9252 is typically implemented in Industrial Automation solutions and includes the following main features:

- Integrated high-performance 100Mbps Ethernet transceivers
- 3 FMMUs, 4 SyncManagers, Distributed clock support, 4K bytes of DPRAM
- 8/16-bit host bus interface allowing connection to most 8/16/32-bit embedded controllers
- SPI / SQI slave interface
- Support for 5 different main configurations:
  - Digital I/O (DIGIO)
  - HBI
  - SPI with GPIO
  - SPI with MII - 3-port (MII upstream) mode
  - SPI with MII - 3-port (MII downstream) mode
- 3rd port for flexible network configurations
- Comprehensive power management features
- Low pin count and small package size

The purpose of this document is to provide details on the various LAN9252 EEPROM configuration and programming options when using the EVB-LAN9252-HBIPLUS and EVB-LAN9252-DIGIO evaluation boards.

1.1 Software Requirements

- Latest version of Beckhoff EtherCAT® Slave Stack Tool and required ESI file
- XML Notepad
- LAN9252 ESC configuration data config.xls

1.2 References

- Microchip LAN9252 Data Sheet
- Microchip EVB-LAN9252-HBIPLUS Evaluation Board User's Guide
- Microchip EVB-LAN9252-DIGIO Evaluation Board User's Guide
- Beckhoff ET1100 Data Sheet

1.3 Terms and Abbreviations

TABLE 1-1: TERMS AND ABBREVIATIONS

Term	Definition
DA	Destination Address
ESC	EtherCAT® Slave Controller
EDPD	Energy Detect Power Down
EVB	Engineering Validation Board
HBI	Host Bus Interface
IDE	Integrated Development Environment
SPI	Serial Protocol Interface
SSC	Slave Stack Code

2.0 EEPROM CONFIGURATION

A summary of the LAN9252 ESC registers in EEPROM is shown in Table 2-1. The following list details the sample configurations that can be programed into EEPROM using the ESI files provided along with the LAN9252 EtherCAT® SDK. Refer to the corresponding register definitions in LAN9252 Data Sheet for details on each bit function.

Sample configuration for simple ESC (DIGIO mode):

- DIGIO - 8 Inputs, 8 Outputs
- DIGIO - 16 Bidirectional

Sample configuration for complex ESC (HBI and SPI mode):

- HBI
  - HBI - Indexed 16-Bit Mode
  - HBI - Indexed 8-Bit Mode
  - HBI - Multiplexed 16-Bit Dual Phase Mode
  - HBI - Multiplexed 8-Bit Dual Phase Mode
  - HBI - Multiplexed 16-Bit Single Phase Mode
  - HBI - Multiplexed 8-Bit Single Phase Mode
- SPI
  - SPI - 2-Port Mode

TABLE 2-1: ESC EEPROM CONFIGURABLE REGISTERS

Register	Bits	EEPROM Word / [Bits]
BYTE 0 PDI Control Register (0x0140)	**[7:0]** Process Data Interface	0 / [7:0]
BYTE 1 ESC Configuration Register (0x0141)	**[7]** Unused	0 / [15]
	[6] Enhanced Link Port 2	0 / [14]
	[5] Enhanced Link Port 1	0 / [13]
	[4] Enhanced Link Port 0	0 / [12]
	[3] Distributed clocks Latch In Unit **Note:** Bit 3 is not set by EEPROM	-
	[2] Distributed clocks SYNC Out Unit **Note:** Bit 2 is not set by EEPROM	-
	[1] Enhanced Link Detection All Ports	0 / [9]
	[0] Device Emulation	0 / [8]
BYTE 2 PDI Configuration Register (0x0150) *Digital I/O Mode*	**[7:6]** Output Data Sample Collection	1 / [7:6]
	[5:4] Input Data Sample Selection	1 / [5:4]
	[3] Watchdog Behavior	1 / [3]
	[2] Unidirectional / Bidirectional Mode	1 / [2]
	[1] OUTVALID Mode	1 / [1]
	[0] OUTVALID Polarity	1 / [0]

TABLE 2-1: ESC EEPROM CONFIGURABLE REGISTERS (CONTINUED)

Register	Bits	EEPROM Word / [Bits]
PDI Configuration Register (0x0150) *HBI Mode*	**[7]** HBI ALE Qualification	1 / [7]
	[6] HBI Read/Write Mode	1 / [6]
	[5] HBI Chip Select Polarity	1 / [5]
	[4] HBI Read, Read/Write Polarity	1 / [4]
	[3] HBI Write, Enable Polarity	1 / [3]
	[2] HBI ALE Polarity	1 / [2]
	[1:0] Reserved	1 / [1:0]
BYTE 3 Sync/Latch PDI Configuration Register (0x0151)	**[7]** SYNC1 Map	1 / [15]
	[6] SYNC1/LATCH1 Configuration	1 / [14]
	[5:4] SYNC1 Output Driver / Polarity	1 / [13:12]
	[3] SYNC0 Map	1 / [11]
	[2] SYNC0 / LATCH0 Configuration	1 / [10]
	[1:0] SYNC0 Output Driver / Polarity	1 / [9:8]
BYTE 4 & 5 Pulse Length of SyncSignals Register (0x0983 : 0x0982)	**[15:0]** Pulse Length of SyncSignals	2 / [15:0]
BYTE 6 & 7 Extended PDI Configuration Register (0x0153 : 0x0152) *Digital I/O Mode*	**[15:8]** Reserved	3 / [15:8]
	[7:0] I/O 15-0 Direction	3 / [7:0]
Extended PDI Configuration Register (0x0153 : 0x0152) *SPI Mode*	**[15:8]** I/O 15-0 Buffer Type	3 / [15:8]
	[7:0] I/O 15-0 Direction	3 / [7:0]
BYTE 8 & 9 Configures Station Alias Register (0x0013 : 0x0012)	**[15:0]** Configures Station Alias Address	4 / [15:0]
BYTE 10 & 11 MII Management Control/Status Register (0x0511 : 0x0510)	**[2]** MII Link Detection	5 / [15]
ASIC Configuration Register (0x0143 : 0x0142)	**[15]** MII Link Detection	
	[14:8] RESERVED	5 / [14:8]
	[7] MII Write Gigabit Register 9 Enable	5 / [7]
	[6:0] RESERVED	5 / [6:0]
BYTE 12 & 13 Reserved Register (0x0145 : 0x0144)	**[15:0]** RESERVED	6 / [15:0]

Note: Refer to the LAN9252 Data Sheet for detailed descriptions of the registers listed in Table 2-1.

3.0 EEPROM CONFIGURATION FOR DIGIO

First, 16 bytes of EEPROM is the configuration straps for LAN9252. Each bit present in the configuration area is directly mapped with EtherCAT core registers.

3.1 Byte 0

EEPROM Offset- 0	EtherCAT Core Register	Details	Note
0[0:7]	0x0140	[7:0] Process Data Interface	

Byte zero of EEPROM (register 0x140) defines the PDI type to be used. It must be 0x04 for DIGIO.

3.2 Byte 1

EEPROM Offset- 1	EtherCAT Core Register	Details	Note
1[7]	0x0141[7]	[7] Unused	
1[6]	0x0141[6]	[6] Enhanced link port 2	
1[5]	0x0141[5]	[5] Enhanced link port 1	
1[4]	0x0141[4]	[4] Enhanced link port 0	
1[[3:2]	0x0141[3:2]	[3] Distributed Clocks Latch in Unit [2] Distributed Clocks SYNC Out Unit	Bits 2 and 3 are NOT set by EEPROM.
1[1]	0x0141[1]	[1] Enhanced link detection on all ports	
1[0]	0x0141[0]	[0] Device emulation	

Byte one of EEPROM defines the device emulation for the slave and enhance link detection for each port

Device emulation- If this bit is set, then LAN9252 handles the AL state machine (no need for a microcontroller). This bit must be set for DIGIO.

Enhance link detection – Both normal and Enhance link detection detects the link establishment. However, if enhance link detection bit set then EtherCAT Core will disconnect a link if at least 32 RX errors (RX_ER) occur in a fixed interval of time (~10 us) and the link partner is informed by restarting the Auto-Negotiation mechanism via the MII Management. So, the link partner can close that particular port. Register 0x0110:0x0111 shows the status of MII_LINK and 0x0518:0x051B shows the link detection status updated via MII management interface.

Enhance link detection can be enabled either to all or individual ports.

3.3 Byte 2

Byte two of EEPROM (register 0x150) configures the PDI. In case of DIGIO, it configures method for input output sampling, watchdog behavior, uni-direction or bi-direction and OUTVALID pin.

EEPROM Offset- 2	EtherCAT Core Register	Details	Note
2[7:6]	0x0150[7:6]	Output Data Sample Selection 00: End a Frame 01: RESERVED 10: DC SYNC0 event 11: DC SYNC1 event **Note:** If OUTVALID Mode = 1, output DATA is updated at Process Data Watchdog trigger event (Output Data Sample Selection bits ignored).	
2[5:4]	0x0150[5:4]	Input Data Sample Selection 00: Start of Frame 01: Rising edge of LATCH_IN 10: DC SYNC0 event 11: DC SYNC1 event	
2[3]	0x0150[3]	Watchdog Behavior 0: Outputs are reset immediately after watchdog expires. 1: Outputs are reset with next output event that follows watchdog expiration.	
2[2]	0x0150[2]	Unidirectional/Bidirectional Mode 0: Unidirectional Mode: input/output direction of pins configured individually. 1: Bidirectional Mode: all I/O pins are bidirectional.	
2[1]	0x0150[1]	If this bit is set, then each DIGIO pin is configured as input and output simultaneously. However, byte 6[7:0] (register 0x01523) must be set to the input direction (0x00). 0: Output event signaling 1: Process Data Watchdog trigger (WD_TRIG) signaling on OUTVALID. Output data is updated if watchdog is triggered. Overrides Output Data Sample Selection bits.	
2[0]	0x0150[0]	OUTVALID Polarity 0: Active high 1: Active low	

3.3.1 OUTPUT DATA SAMPLE SELECTION

1. EOF mode - Digital Outputs are updated at the end of each EtherCAT frame.
2. DC SYNC0 mode - Digital outputs are updated with Distributed Clocks SYNC0 events.
3. DC SYNC1 mode - Digital outputs are updated with Distributed Clocks SYNC1 events.
4. WD_TRIG mode - Digital Outputs are updated at the end of an EtherCAT frame which triggered the Process Data Watchdog (with typical SyncManager configuration: a frame containing write access to at least one of the registers 0x0F00:0x0F01). Digital Outputs are only updated if the EtherCAT frame was correct.

3.3.2 INPUT DATA SAMPLE SELECTION

Digital inputs can be configured by four ways:

1. **Start of Frame** - Digital inputs are sampled at the start of each Ethernet frame, so that EtherCAT read commands to address 0x1000:0x1001 will present digital input values sampled at the start of the same frame. The SOF signal can be used externally to update the input data because the SOF is signaled before input data is sampled.
2. **Rising edge of LATCH_IN** - The sample time can be controlled externally by using the LATCH_IN signal. The input data is sampled by the ESC each time a rising edge of LATCH_IN is recognized.
3. **DC SYNC0 event** - Digital inputs are sampled at Distributed Clocks SYNC0 events.
4. **DC SYNC1 event** - Digital inputs are sampled at Distributed Clocks SYNC1 events.

3.3.3 WATCHDOG BEHAVIOR

This bit controls whether output needs to be reset on a watchdog reset. If it is zero, then the output resets if watchdog expires. If it set to one, outputs are reset with next output event that follows watchdog expiration. Watchdog expires on failure to update the process data. That is, if the application demands the output to remain the same even the link drops, then this bit should be set. In this scenario, the OE_EXT signal can reset the DIGIOs externally.

3.3.4 UNIDIRECTIONAL/BIDIRECTIONAL MODE

If this bit is set, then each DIGIO pin is configured as input and output simultaneously. However, byte 6[7:0] (register 0x01523) must be set to the input direction (0x00).

3.3.5 OUTVALID MODE

Output of DIGIO signals can either be controlled internally or externally.

If this bit is ZERO, then a pulse on OUTVALID signal indicates the status of DIGIO output. If watchdog expires then the output resets internally.

If this bit is set, then Process Data Watchdog trigger (WD_TRIG) signaling on OUTVALID pin. Output data is updated if watchdog is triggered, overrides 0x0150[7:6]. The output can be controlled by OE_EXT signal by the external controller.

3.3.6 OUTVALID POLARITY

This bit defines the polarity of the OUTVALID pin whether it is an active high or low.

3.4 Byte 3

EEPROM Offset- 3	EtherCAT Core Register	Detail	Note
3[7]	0x0151[7]	[7] SYNC1 Map	SYNC1 mapped to AL Event Request register 0x0220[3] 0: Disabled 1: Enabled
3[6]	0x0151[6]	[6] SYNC1/LATCH1 Configuration	To select SYNC1 or LATCH1 functionality 0: LATCH1 Input 1: SYNC1 Output
3[5:4]	0x0151[5:4]	[5:4] SYNC1 Output Driver polarity	It configures the polarity of the SYNC1 signal 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)
3[3]	0x0151[3]	[3] SYNC0 Map	SYNC0 mapped to AL Event Request register 0x0220[2] 0: Disabled 1: Enabled
3[2]	0x0151[2]	[2] SYNC0/LATCH0 Configuration	To select SYNC0 or LATCH0 functionality 0: LATCH0 Input 1: SYNC0 Output

EEPROM Offset- 3	EtherCAT Core Register	Detail	Note
3[1:0]	0x0151[1:0]	[1:0] SYNC0 Output Driver polarity	It configures the polarity of the SYNC0 signal 00: Push-Pull active low 01: Open Drain (active low) 10: Push-Pull active high 11: Open Source (active high)

If DIGIO supports DC, then configure the bits as per the application.

3.5 Byte 4-5

Pulse Length of SyncSignals Register - (0x0982-0x0983)

EEPROM Offset- 4:5	EtherCAT Core Register	Details	Note
4-5[15:0]	0x0982-0x0983[15:0]	[15:0] Pulse length of SyncSignals	Pulse length of SyncSignals (in units of 10ns) A value of 0 is used for Acknowledge Mode.

If DIGIO supports DC, then configure the bits as per the application. Pulse length should be less than the cycle time for periodic updates.

3.6 Byte 6-7

Extended PDI Configuration Register - (0x0152-0x0153)

EEPROM Offset- 5:6	EtherCAT Core Register	Details	Note
6[7:0]	0x0152	[7:0] I/O 15-0 Direction	Digital I/Os are configured in pairs as inputs or outputs: 0: Input 1: Output **Note:** Reserved in bidirectional mode, set to 0.
7[7:0]	0x0153	[7:0] RESERVED	

3.7 Byte 8-9

EEPROM Offset- [7:8]	EtherCAT Core Register	Details	Note
8[7:0]- 9[7:0]	0x0012-0x0013	[15:0] Configured Station Alias Address	This field contains the alias address used for node addressing (FPxx commands). More details about different addressing are available at ETG1000 and ETG1020 specifications.

For DIGIO, this register should be updated as per application requirement.

3.8 BYTE 10

For DIGIO, byte 10 should be set as zero.

3.9 Byte 11

Bit 8th of Byte 11 should be set as 1 for MII_LINK detection.

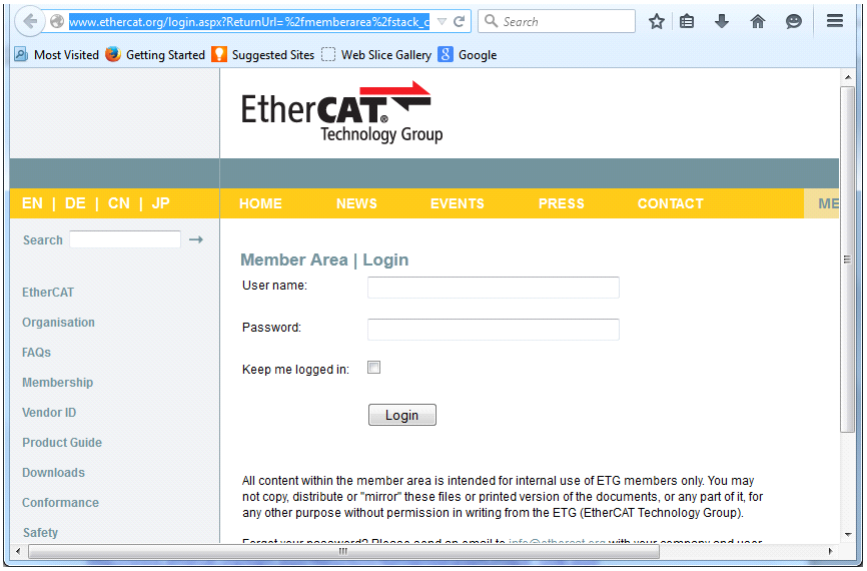
4.0 EEPROM PROGRAMMING

This section details the EEPROM programming procedure using ESI files.

4.1 EtherCAT® Slave Stack Code Tool Installation

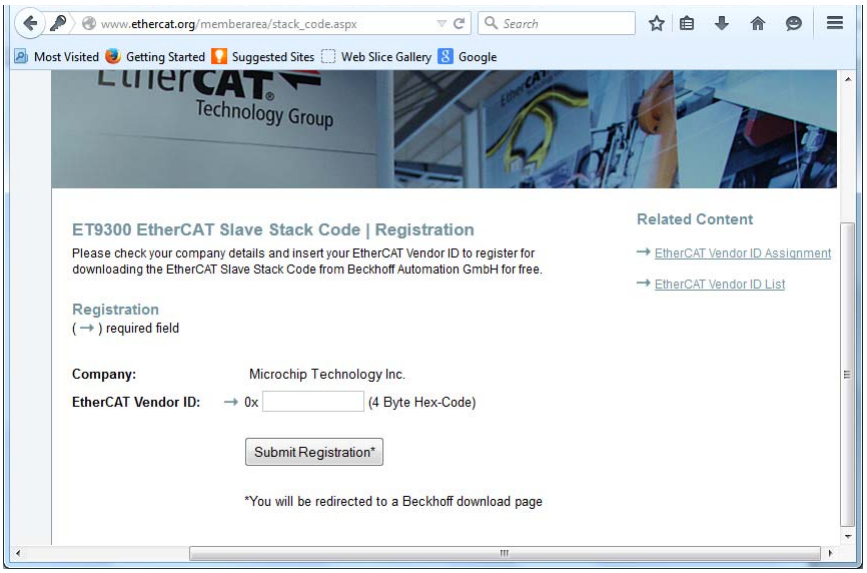
1. The first step to EEPROM programming is to download and install the Beckhoff EtherCAT® Slave Stack Code (SSC) tool. Download the EtherCAT® SSC from the following link:
   http://www.ethercat.org/login.aspx?ReturnUrl=%2fmemberarea%2fstack_code.aspx
2. To continue the download process, enter the ETG user name and password.

FIGURE 4-1: MEMBER AREA LOGIN



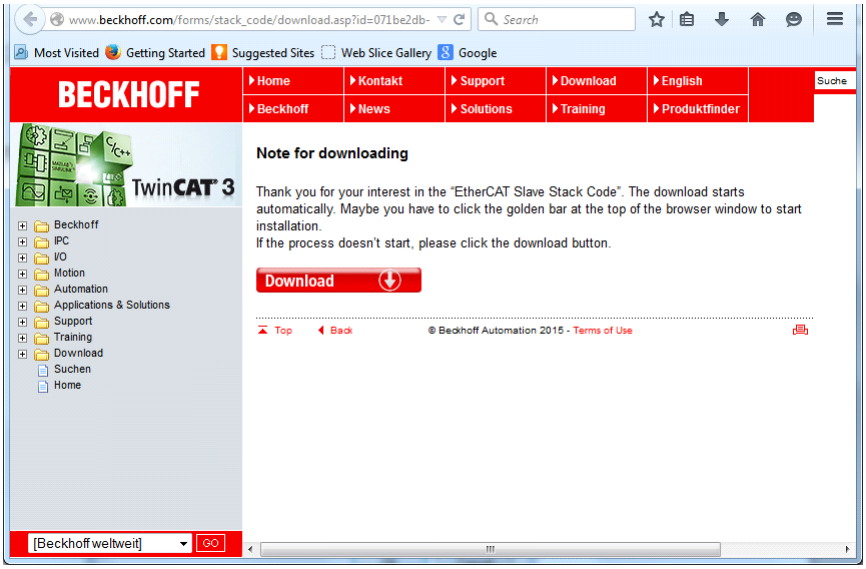
3. Enter the Vendor ID, if prompted, and click the “Submit Registration” button, as shown in Figure 4-2.

FIGURE 4-2: VENDOR ID SUBMISSION



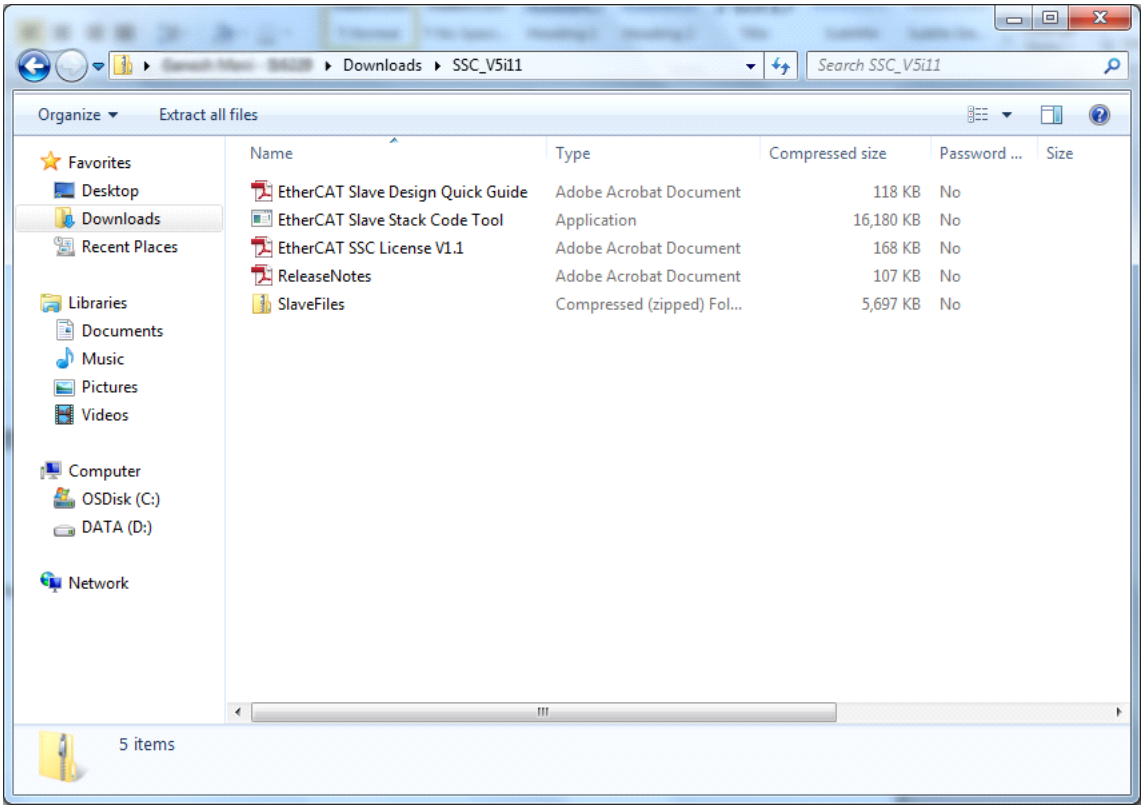
4. Enter the required details, check the “Accept” box and click “Register.”
5. A download link will be sent to the registered email address. Click the emailed download link to download the EtherCAT® Slave Stack Code.

FIGURE 4-3: SLAVE STACK CODE DOWNLOAD



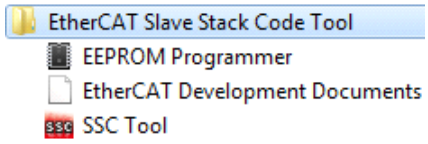
6. Extract the downloaded .zip file “SSC_V5i11”, which will contain the directory structure shown in Figure 4-4.

FIGURE 4-4: SLAVE STACK CODE DIRECTORY STRUCTURE



7. Install the EtherCAT® Slave Stack Code Tool. Once installation is complete, ensure the tools shown in Figure 4-5 are seen in the Start Menu.

FIGURE 4-5: SLAVE STACK CODE TOOLS

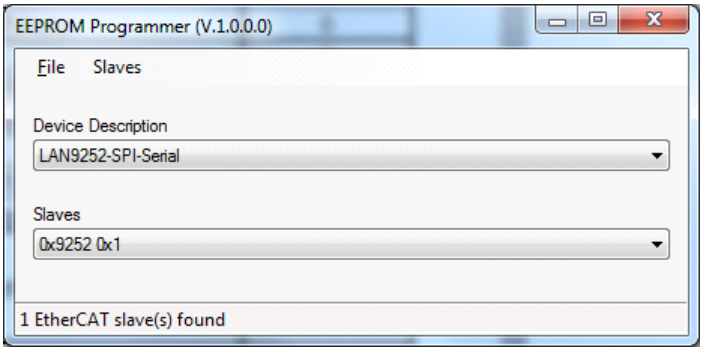


Note: Ensure the LAN9252 evaluation board is configured for the ESC configuration which is going to be programmed.

4.2 Simple ESC EEPROM Programming (PDI Configured in DIGIO Mode)

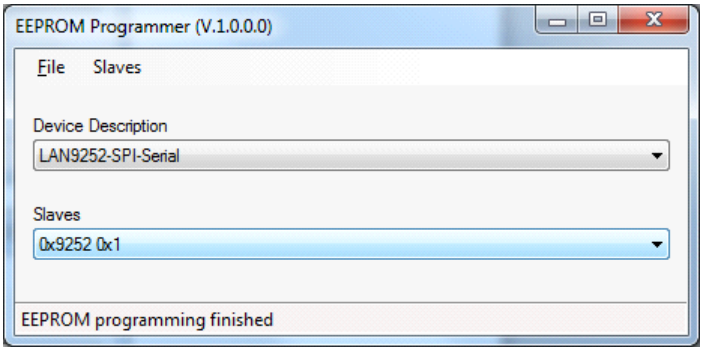
1. To program the EEPROM, launch the previously installed EEPROM Programmer utility from the Start Menu.
2. Load the required ESI file (all ESI files are provided along with the SDK).
3. Connect the LAN9252 evaluation board to the system's Ethernet port using an Ethernet cable.
4. Scan for slave devices. If the EtherCAT® slave device is detected, the window will appear as shown in Figure 4-6.

FIGURE 4-6: EEPROM PROGRAMMER SLAVE DEVICE SCAN



5. Choose the required configuration in the "Device Description" field.
6. Select the "Program" option under the "Slave" drop-down menu. When programming is complete, the window will appear as shown in Figure 4-7.

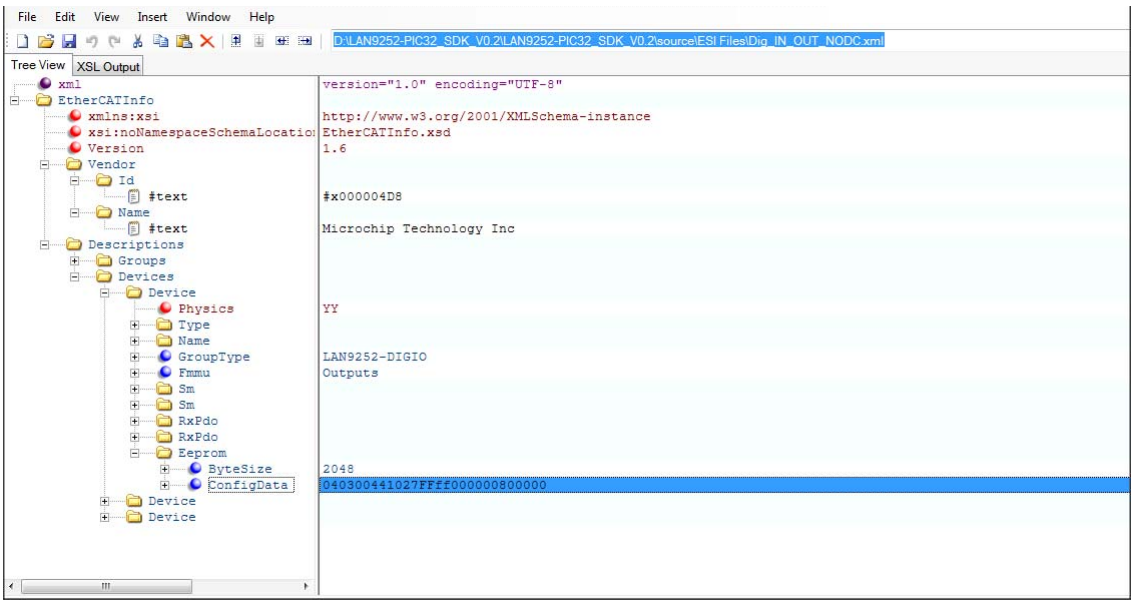
FIGURE 4-7: EEPROM PROGRAMMER COMPLETE



If the user desires to reconfigure the ESC configuration data with additional options, the ESI file can be edited using an XML editor such as XML Notepad, as shown in Figure 4-8. The user may edit the following fields:

- EtherCAT® Slave Controller Configuration Area
- Vendor ID
- Product Code
- Revision Number
- Serial Number

FIGURE 4-8: ESI FILE EDITING IN XML NOTEPAD



Note:	For easy reconfiguration of ESC data, the ESC configuration config.xls can be used, which is supplied with the EtherCAT® SDK.

4.3 Complex ESC EEPROM Programming (PDI Configured in HBI/SPI Mode)

For complex ESC programming where the PDI is configured in HBI or SPI mode, the EEPROM content can be programmed using the ESI file as detailed in Section 4.2, "Simple ESC EEPROM Programming (PDI Configured in DIGIO Mode)". However, if reconfiguration is required, then the following additional steps must first be executed:

1. Launch the Beckhoff SSC Tool and open the project file generated during the SSC to SDK integration process. Once opened, the Slave Information and ESC Configuration Data can be edited using the tool as shown in Figure 4-9 and Figure 4-10.
2. After reconfiguration, create new ESI files by using the “Create New Slave Files” option under the “Projects” drop-down menu. Doing so will create a new folder names “Src” in the desired location. This folder will contain the updated ESI file.
3. Use the generated ESI file to program the EEPROM using the EEPROM Programmer utility as previously detailed in Section 4.2, "Simple ESC EEPROM Programming (PDI Configured in DIGIO Mode)".

FIGURE 4-9: SSC TOOL SLAVE INFORMATION

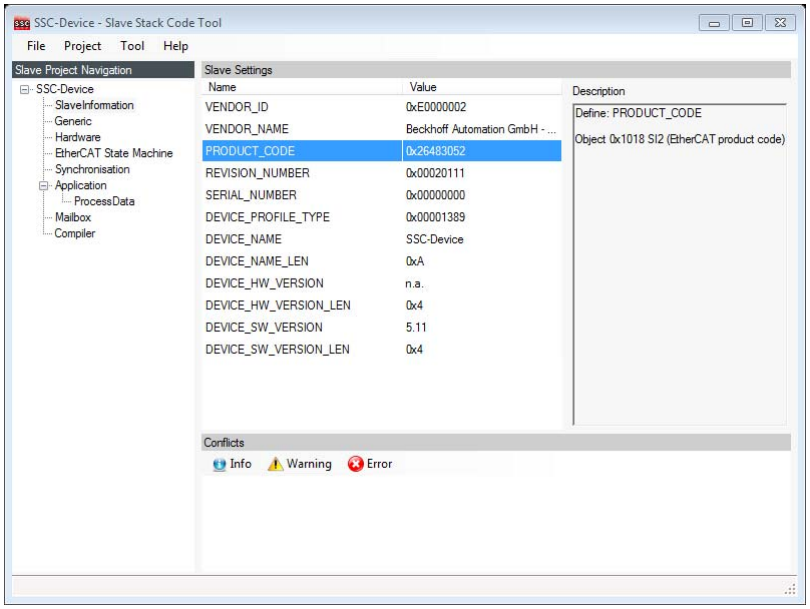
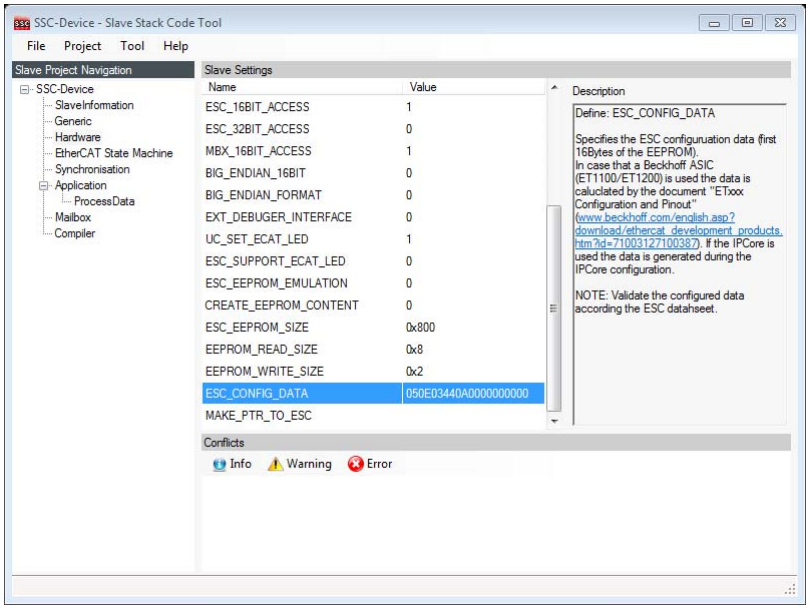


FIGURE 4-10: SSC TOOL HARDWARE DATA



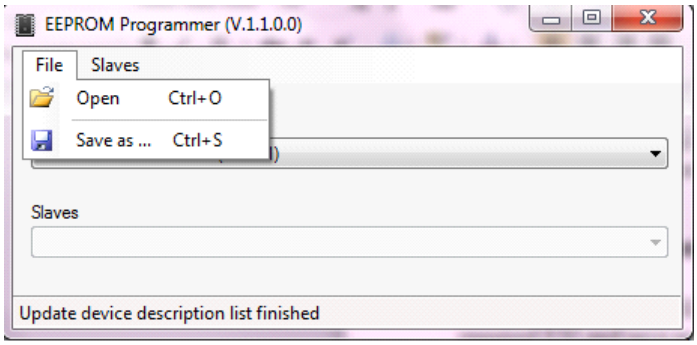
4.4 EEPROM Mass Programming

In cases where gang programming of EEPROM is required without using the EEPROM Programmer tool, a .bin file can be generated from the ESI files using the EEPROM Programmer tool “Save As...” option, as detailed below:

1. Load the required ESI file into the EEPROM Programmer tool.
2. Select “Save As...” from the “File” drop-down menu, as shown in Figure 4-11.
3. Save the file as a ”.bin” file.

Once the .bin file is created, it can be used with USB-I2C adapters, such as Aardvark, to program the EEPROMs directly.

FIGURE 4-11: EEPROM PROGRAMMER “SAVE AS” OPTION



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001920B (03-26-19)	Section 3.3, "Byte 2"	Unidirectional/Bidirectional Mode modified.
	Table 2-1, "ESC EEPROM Configurable Registers"	Table updated: BYTE 3 - “[6]SYNC/LATCH1 Configuration” changed to “[6]SYNC1/LATCH1 Configuration”
	Section 1.0, "Introduction"	“EVB-LAN9252-HBI” changed to “EVB-LAN9252-HBIPLUS”. “SPI with MII - 4-port (MII downstream) mode” changed to “SPI with MII - 3-port (MII downstream) mode”.
	Section 3.0, "EEPROM Configuration for DIGIO"	Section added.
DS00001920A (04-14-15)	Document Release	

Note the following details of the code protection feature on Microchip devices:

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