ZL30182, ZL3024x, ZL30255, ZL3062x, and ZL3072x Series Recommended Power Supply Decoupling and Layout Practices

Introduction

This document details the recommended power supply decoupling and layout practices for the ZL30182, ZL30244, ZL30245, ZL30255, ZL30621, ZL30623, ZL30721, and ZL30723 series of any-to-any clock multipliers, jitter attenuators, and telecom timing integrated circuits (ICs).

Power Supply Decoupling and Layout Practices

The following common design practices are recommended for improving device power supply noise rejection.

- Allocate one low-ESR 0.1 µF to 1 µF decoupling capacitor for each power pin. Example recommended capacitor types are ceramic X5R and X7R. Each capacitor should be located as close as possible to its respective device power pin. Each capacitor should be connected directly to the power pin and should not share vias to power or ground planes with other decoupling capacitors. Adjacent power pins 26 and 27 can share a single decoupling capacitor to reduce component count. Also, pins 58 and 59 can share a single decoupling capacitor.
- Allocate one low-ESR 10 µF bulk capacitor for each device power domain. The power domains consist of the device's 1.8 V and 3.3V power supplies and any optional power islands used with the device's analog supplies. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used. These capacitors filter low frequency noise (up to several hundred kHz) that originates from switching power supplies. If a ferrite bead is used to connect a power island to a main board power plane, the associated bulk capacitor should be located close to the ferrite bead. Bulk decoupling capacitors can be shared with nearby devices powered by common power domains to reduce component count.
- Allocate an additional low-ESR 100 µF capacitor to each power island containing a crystal driver power pin (VDDXO33_A and VDDXO33_B), when using external crystal resonators. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used. This capacitor should be located close to the ferrite bead which ties the power island to its respective power plane.
- Connect each of the device's two exposed ground pads (E-PADs) directly to the board's ground plane through a 3x3 array of vias spaced evenly across the pad.
- Power islands can be optionally used on the device's analog supplies to provide improved power rail noise rejection. A power island is a local copper area, separated from the main power plane by a series passive component such as a ferrite bead or low ohm resistor. When a ferrite bead is used, it should have a resistance of several hundred Ohms at 100 MHz. Additionally, it should have a current rating at least double the maximum current required by the associated device power pins to avoid core saturation and degraded performance. Finally, the combination of the ferrite bead inductance and supply decoupling capacitance should be chosen to avoid creating a resonant frequency which could cause gain peaking of a board noise source such as a switching power supply. For both the ferrite bead and low ohm resistor options, the voltage drop across this component must be taken into account in the board's power supply design to ensure the device's power rail specifications are met.

- Each of the ZL30182/24x/255/62x/72x output clocks has an independent power pin for signal format flexibility: VDDO1_x for OC1_x, VDDO2_x for OC2_x, and VDDO3_x for OC3_x. When implementing the above guidelines, any output clock requiring a 3.3 V or 1.8 V supply can share a power island with the corresponding device core analog supply voltage. If an output clock requires a supply voltage other than 1.8 V or 3.3 V, an additional power island and associated filtering circuitry are required for that output clock. This power island can be shared with other output clocks requiring the same supply voltage.

The ZL30182, ZL30244, ZL30245, ZL30255, ZL30623, and ZL30723 devices have two identical channels, A and B, each of which should be decoupled the same way. The ZL30621 and ZL30721 have two similar blocks, A and B, each of which should be decoupled the same way. Figure 1 shows the application of these guidelines for channels A and B. Note that the scheme shown in the Figure applies to a design which has all output clock signals configured as current-mode logic (CML), which requires a 3.3V VDDO supply.

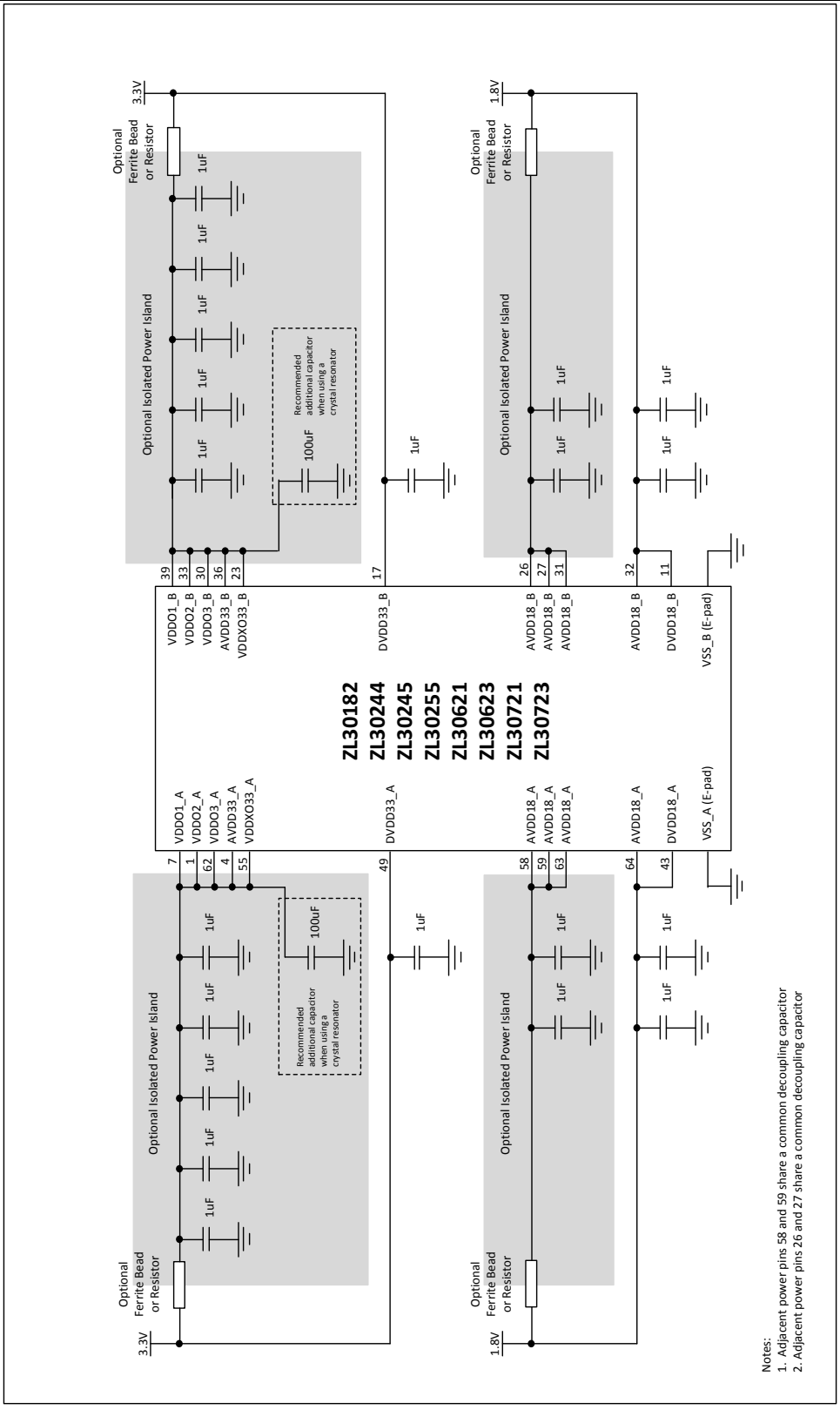

Figure 1 Example ZL30182/24x/255/62x/72x Power Supply Decoupling Scheme For Channel/Block A and B

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