EtherCAT P®, UART, and Motor Control Application Example

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Preface

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Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EtherCAT P® technology. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web SiteThe Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use EtherCAT P that includes a UART interface and motor control circuitry to operate a motor using the EtherCAT® protocol in an industrial or commercial environment.

- **Chapter 1. "Overview"** – Shows a brief description of EtherCAT P and the other features used in the application example.
- **Chapter 2. "System Requirements"** – Describes the list of requirements used for the development of EtherCAT P based application.
- **Chapter 3. "Schematics Design"** – Description of the EtherCAT P schematics.
- **Chapter 4. "PCB Layout"** – Describes the PCB layout of the EtherCAT P.
- **Chapter 5. "Software"** – Describes the software and firmware required for operation of the EtherCAT P.
- **Chapter 6. "Hardware Testing"** – Describes the basic flow for testing the EtherCAT P.
- **Appendix A. "Schematics"** – This appendix shows the schematics of the EtherCAT P board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS50002825A (11-12-18)	Initial document release	

Table of Contents

NOTES:

Chapter 1. Overview

1.1 INTRODUCTION

This application example is intended for an EtherCAT P®-based application. The EtherCAT P standard enables devices to receive power and data using the same EtherCAT P cables. This can simplify the system design with multiple industrial devices spread across the entire industrial system. Controlling a motor or communicating with a UART device are two examples of devices that can utilize the EtherCAT P standard.

This document describes the development process to provide a deeper understanding of the design.

The application example provides the following features:

- LAN9252 2-/3-port EtherCAT slave controller (ESC)
- Two EtherCAT ports with EtherCAT P connectors
- A UART port
- dsPIC33EP256MC504, which is a 16-bit microcontroller with DSC engine optimized for motor control applications
- MCP16301H, which is a DC-DC converter with 4V-30V input voltage and up to 600 mA output current
- PWM and GPIO output

1.2 AUDIENCE

Recipients of this material are expected to have an interest in one or more of the following areas: EtherCAT P, EtherCAT Motor Control, EtherCAT Serial Ports, and/or dsPIC motor control.

The recipient will either be working with the board and materials described in this document or be looking to implement the same within their own design. In such cases, we invite customers to discuss with their local Embedded Systems Engineer and use our free LANCheck® design review services. Links to all resources can be found on the Microchip web site.

1.3 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN9252 Data Sheet*
- *dsPIC33EP256MC504 Data Sheet*
- *MCP16301H Data Sheet*
- *dsPIC33 SDK User's Guide*
- LAN9252 schematic, placement, and routing checklist

1.4 TERMS AND ABBREVIATIONS

- BLDC – Brushless Direct Current
- ESC – EtherCAT slave controller
- EtherCAT P – Power over EtherCAT
- EVB – Engineering Validation Board
- SDK – Software Development Kit
- SPI – Serial Peripheral Interface
- TVS – Transient Voltage Suppression
- UART – Universal Asynchronous Receiver-Transmitter

Chapter 2. System Requirements

2.1 INTRODUCTION

A typical design project starts with an initial list of project requirements, which is refined as more detail is provided during the review process.

This section outlines the system design requirements for this project.

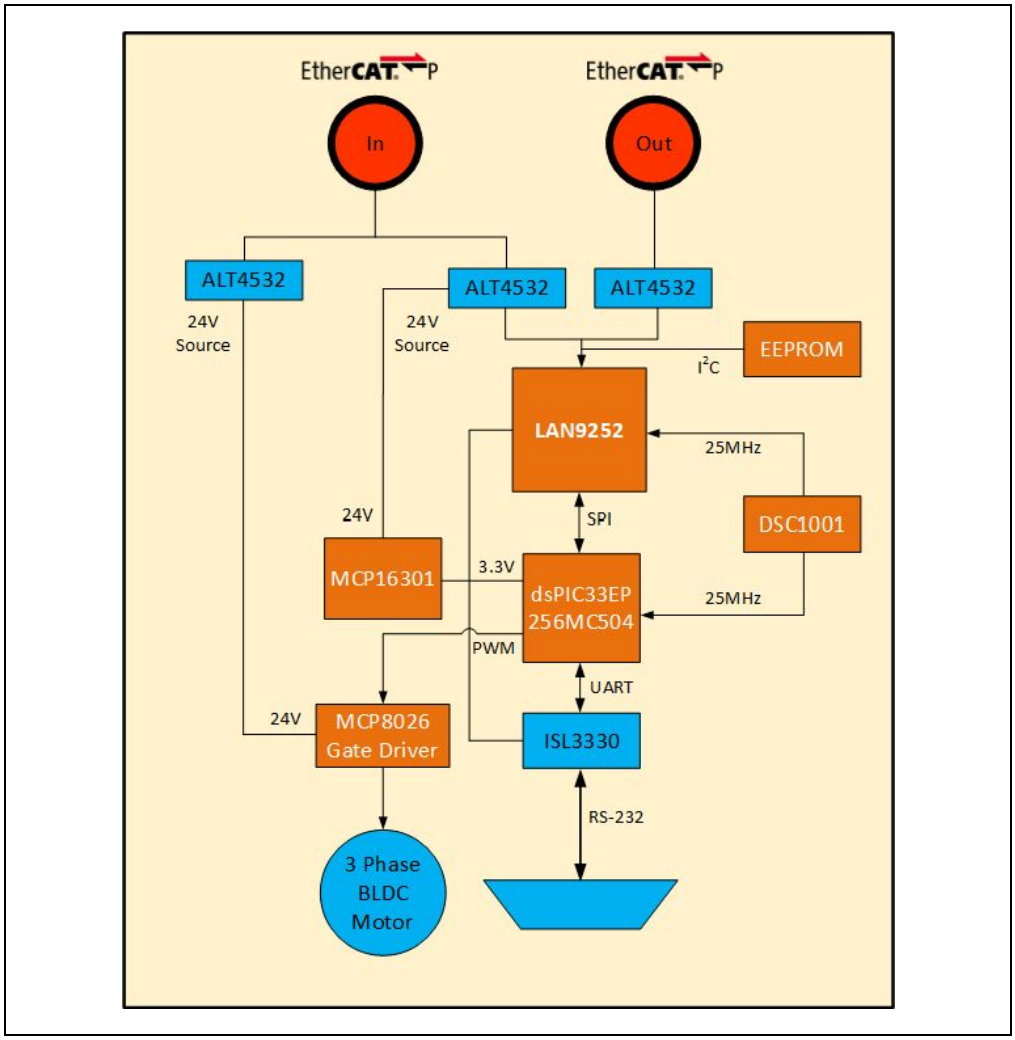
The system should:

- Implement an EtherCAT P application that utilizes two EtherCAT P ports with industry standard connectors
- Include an RS-232 converter
- Include a motor control supporting circuit
- Have a controller that interfaces EtherCAT data, motor control, and RS-232 controller
- Operate from the power extracted through the EtherCAT P connectors
- Have separate LEDs for indication for port 1, port 2, and run/error
- Have general purpose I/Os and a PWM output

2.2 SYSTEM BLOCK DIAGRAM

Figure 2-1 shows the system block diagram.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM



At the top of the block diagram are the industry EtherCAT P connectors, which allow EtherCAT data and the 24V supply voltage to the entire system. Output signals from the EtherCAT P connectors are passed through the capacitors and low pass filters to separate into data and power signals. The data is connected to the transmit and receive channels of the LAN9252 ESC. The pins (TX+, TX-, RX+, and RX-) require protection that is provided by the TVS diodes between two lines and Schottky diodes between the line and the ground.

The 24V is divided into two electrically isolated supply systems: Us and Up. The Us supplies 24V/3A power to the system and sensors; whereas, the Up supplies 24V/3A power to the periphery and actuators. A digital signal processor (DSP) microcontroller (MCU), dsPIC33EP256MC504, is connected to LAN9252 that runs the EtherCAT slave stack. The MCU controls a 3-phase DC motor and transmits EtherCAT data over UART to a PC. The demonstration software allows TwinCAT to switch on or off motor and to control its speed.

The MCP16301H is a DC-DC buck regulator module for converting 24V supply to 3.3V at 600mA.

Chapter 3. Schematics Design

3.1 ETHERCAT P® SCHEMATICS

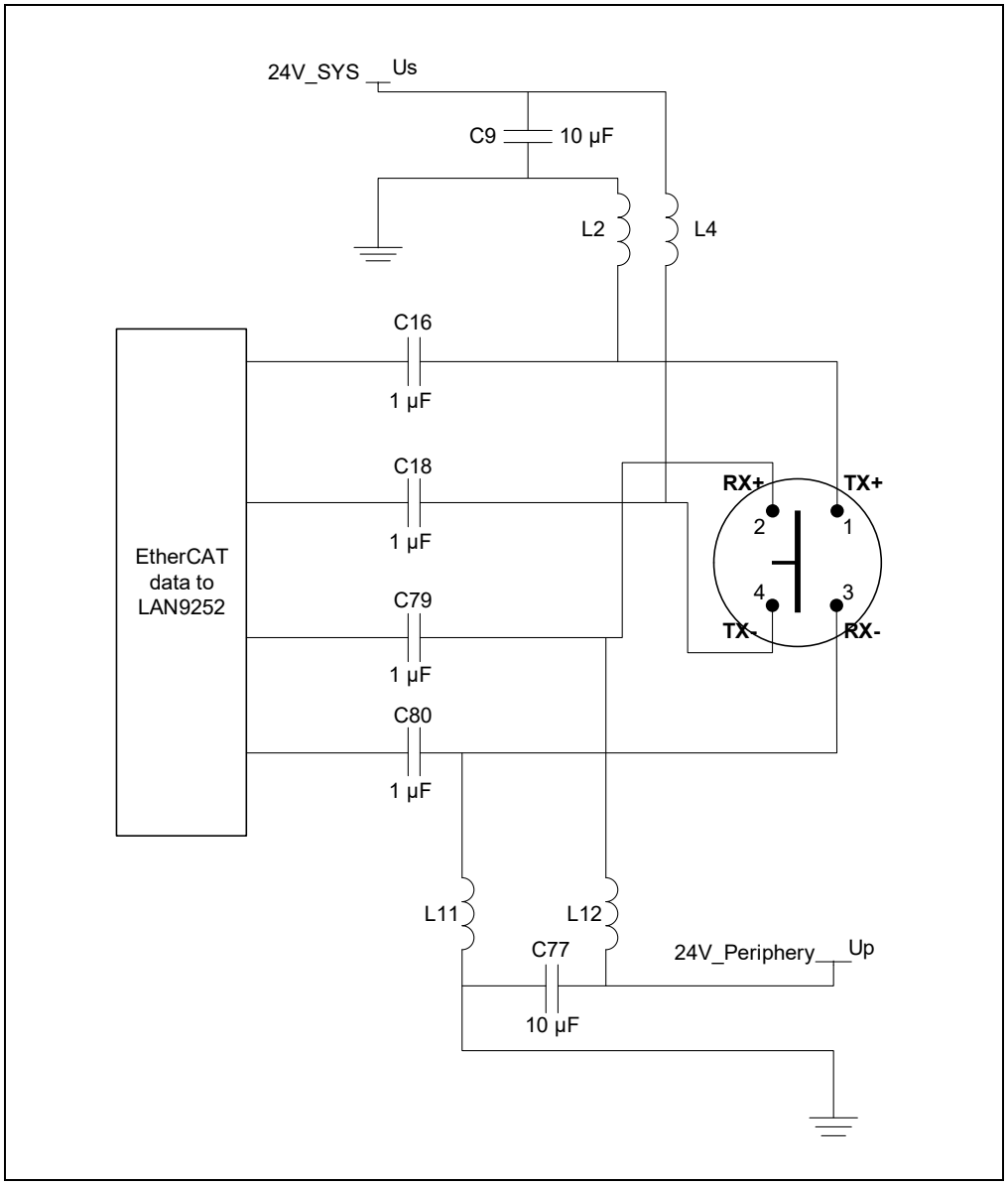
3.1.1 LAN9252

Component selection starts by looking at the list of the requirements to identify components that could be used for the application. At the center of the design is a LAN9252 ESC.

The LAN9252 is used for this design because it is an EtherCAT slave transceiver with dual integrated PHYs. It supports 4-process data interfaces: SPI, SQI, HBI, and a 16-bit digital I/O. This design uses the SPI bus because it provides a low pin count synchronous slave interface that facilitates communication between LAN9252 ESC and dsPIC MCU.

Based on the EtherCAT P standard requirements, the signals received over the EtherCAT P interface should be split into data and power lines. The data is transmitted to the ESC and two separate power signals of 24V/3A each is supplied to the internal circuitry, external sensors (Us), and local actors (Up). Figure 3-1 shows the block diagram of the arrangement. As shown in **Appendix A. “Schematics”**, L2, L4, C9, L11, L12, and C77 form second order LC filters. These filters separate the 24V DC supply voltage. Capacitors C16, C18, C79, and C80 blocks the DC voltage.

FIGURE 3-1: ETHERCAT P® POWER INPUT BLOCK DIAGRAM



EtherCAT P systems must be designed to protect sensitive communication circuitry from transient events, such as Cable Discharge Events (CDE), or Electrostatic Discharge (ESD) events. CDEs are caused when the high voltage signals make contact through the Ethernet cable. The TVS and Schottky diodes, D14 through D19, provides protection against the transient events.

3.1.2 MCP16301

The MCP16301/H devices are high-input voltage step-down regulators, which are capable of supplying 600 mA to a regulated output voltage from 2.0V to 15V. Internally, the trimmed 500 kHz oscillator provides a fixed frequency, while the peak current mode control architecture varies the duty cycle for output voltage regulation. An internal floating driver is used to turn the high-side integrated N-Channel MOSFET on and off. The power for this driver is derived from an external boost capacitor whose energy is supplied from a fixed voltage ranging from 3.0V to 5.5V, which is typically the input or output voltage of the converter.

The MCP16301 integrates an N-Channel MOSFET. A high-side supply is needed to drive the gate of the N-Channel MOSFET above the input voltage to turn it on. This example uses the 3.3V output voltage to charge the boost capacitor (C4) while the inductor current flows, clamping the SW node to a diode drop below ground. Prior to startup, there is no inductor current, so an internal precharged circuit charges the boost cap up to a minimum threshold. Once C4 is charged, NMOS can be turned on, ramping current into the inductor. The D1 diode is used to provide a charging path for the C4 capacitor, while current is flowing through the inductor.

The R1 and R3 sense resistors set the output at 3.3V according to Equation 3-1.

EQUATION 3-1:

$$RTOP = RBOT \times (((VOUT)/(VFB)) - 1)$$

Where, VFB = 0.8V is the reference voltage of the FB pin.

The external divider resistors have no effect on system gain, so a wide range of values can be used. A 10 kΩ resistor is recommended as a good trade-off for quiescent current and noise immunity.

Internally, approximately half of the inductor current downslope is summed with the internal current sense signal. For the proper amount of slope compensation, it is recommended to keep the inductor downslope current constant by varying the inductance with VOUT. For the 3.3V output, a 15 µH inductor is recommended.

The input capacitor must filter the high-input ripple current because of pulsing or chopping the input voltage. A low Equivalent Series Resistance (ESR), preferably a ceramic capacitor, is recommended. The necessary capacitance is dependent on the maximum load current and source impedance. Minimum capacitance at light load is 2.2 µF.

The output capacitor helps in providing a stable output voltage during sudden load transients and reduces the output voltage ripple. The minimum value of the output capacitance is limited to 20 µF, due to the integrated compensation of the MCP16301.

The freewheeling diode creates a path for inductor current flow after the internal switch is turned off. The efficiency of the converter is a function of the forward drop voltage value and speed of the freewheeling Schottky diode.

For detailed information, see the *MCP16301 Data Sheet (DS25004)*.

3.1.3 dsPIC33EP256MC504

The dsPIC33EP256MC504 MCU runs the EtherCAT slave stack. It receives data and command from the EtherCAT master and controls the external motor by outputting three sets of PWM signals for the 3-phase BLDC motor. According to the system requirements, the MCU also implements bridging between EtherCAT and RS232 interfaces.

3.1.4 MCP8026

The MCP8026 is a 3-phase brushless DC (BLDC) motor gate driver with integrated power module. Along with the dsPIC33EP256MC504 MCU, it provides the necessary drive signals to drive a 3-phase BLDC motor. The MCP8026 contains the high-side and low-side drivers for external N-channel MOSFETs. The dsPIC MCU supplies the PWM inputs to the MCP8026.

The major internal blocks of this device include a voltage bias generator and a motor control unit.

3.1.4.1 BIAS GENERATOR

MCP8026 contains two internal low drop outs (LDOs), 5V and 12V output voltage, and an internal buck switch mode power supply (SMPS).

The 5V rail is used for bias of the internal current sense amplifier and the gate control. A minimum of 4.7 µF ceramic output capacitance is required for the 5V LDO.

The 12V rail is used for bias of the 3-phase power MOSFET bridge. It can supply up to 30 mA of load current. A 10 µF ceramic output capacitance is required for the 12V LDO.

The internal SMPS is capable of supplying 750 mW of power to an external load at 460 kHz switching frequency with an input voltage of 6V. An external inductor is used at the LX pin for the SMPS block.

The maximum inductor value for the operation in discontinuous conduction mode can be determined by using Equation 3-2.

EQUATION 3-2:

$$LMAX \leq (Vo \times ((1 - V0)/(Vin)) \times T)/(2 \times locrit)$$

Using the LMAX inductor value ensures discontinuous conduction mode operation for output load currents below the critical current level, Iocrit.

An internally unregulated charged pump is utilized to boost the input to the 12V LDO during low input conditions. A typical charge pump flying capacitor (C29 and C30 as shown in Figure A-3) is a 0.1-1.0 µF ceramic capacitor.

The device has an internal temperature sensor. If the temperature rises above the threshold, all functions are turned off and the device signals the MCU using the DE2 pin. The MCU should take the appropriate action.

3.1.4.2 MOTOR CONTROL

Each motor phase is driven with external NMOS/PMOS MOSFET pairs. A low-side and a high-side gate driver control these MOSFET pairs. The gate drivers are controlled directly by the digital input pins PWM[1:3]H/L. A logic high turns the associated gate driver on, and a logic low turns the associated gate driver off. The PWM[1:3]H/L digital inputs are equipped with internal pull-down resistors. The low-side gate drivers are biased by the 12V LDO output. The high-side gate drivers are a floating drive biased by a bootstrap capacitor circuit. The bootstrap capacitor is charged by 12V LDO whenever the accompanying low-side MOSFET is turned on.

For detailed information, see the *MCP8026 Data Sheet (DS20005905)*. It shows the detailed component calculations.

Chapter 4. PCB Layout

4.1 INTRODUCTION

Input to the PCB layout process includes component signal connectivity (netlist), mechanical requirements, and electrical constraints. As part of the electrical constraints, signals that need special attention include high frequency signals, high power rails, and analog signals.

All the VDD pins should directly be routed into a solid +3.3V power plane, and the pin-to-plane trace should be short and wide. All the decoupling capacitors should be placed near the VDD pins and should have short and direct connections to each power plane (+3.3V and digital ground plane). The VDDCR pins must be routed with a heavy, wide trace with multiple vias to the three decoupling capacitors and the single bulk capacitor associated with it. All three pins and the capacitors should be routed directly into a solid, +1.2V power plane. The digital and analog ground pins should be tied together and should be connected directly into a solid, contiguous, internal ground plane.

To reduce the noise and improve the EMC/EMI test results, a separate power and a ground layer should be used; hence, six layers are used.

TABLE 4-1: ETHERCAT P APPLICATION EXAMPLE STACK-UP

Layer	Type	Description
1	Signal	Signal layer
2	Ground	Ground layer
3	Signal	Signal layer
4	Signal	Signal layer
5	Power	Power layer
6	Signal	Signal layer

The layer information and other physical requirements, such as trace width and spacing, via sizes, and component spacing, are added as constraints into the PCB layout tool used.

The board's layout is shown in Figure 4-1 through Figure 4-6.

FIGURE 4-1: TOP LAYER

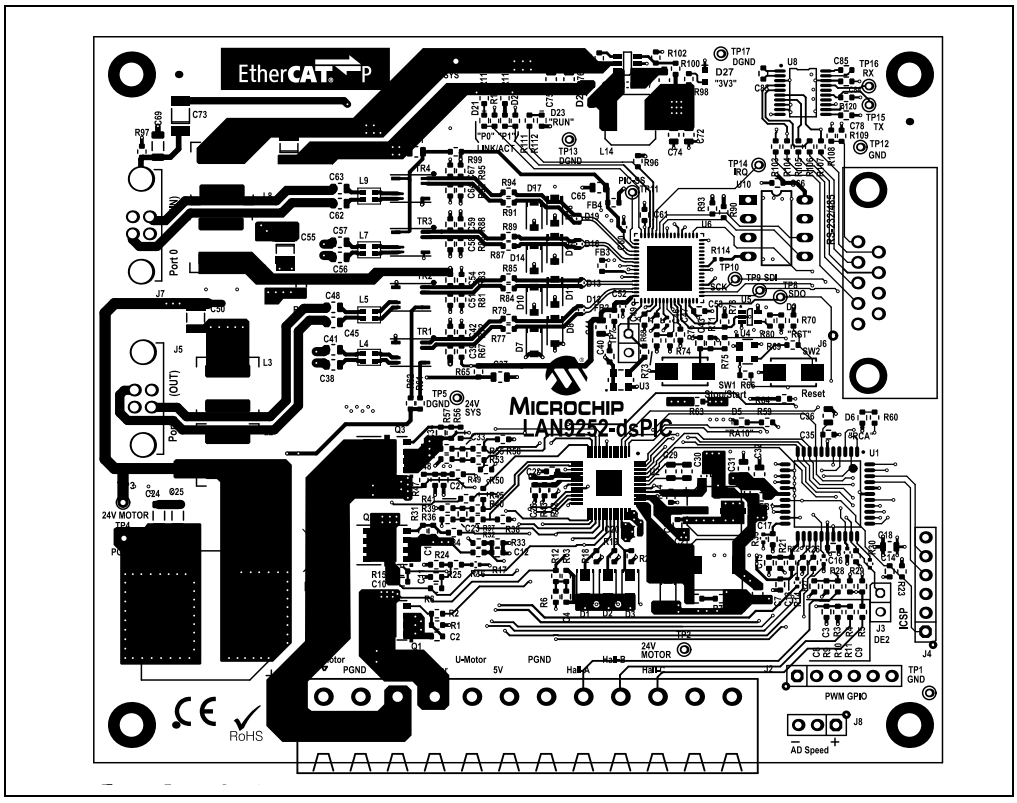


FIGURE 4-2: GROUND LAYER

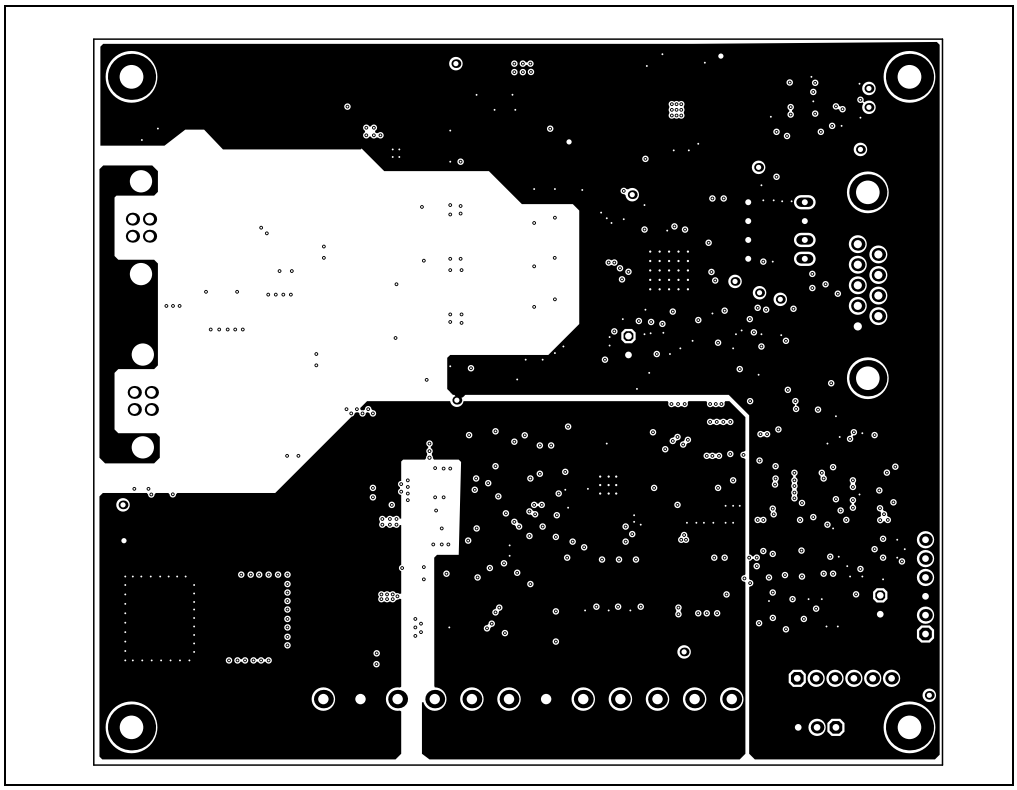


FIGURE 4-3: SIGNAL LAYER

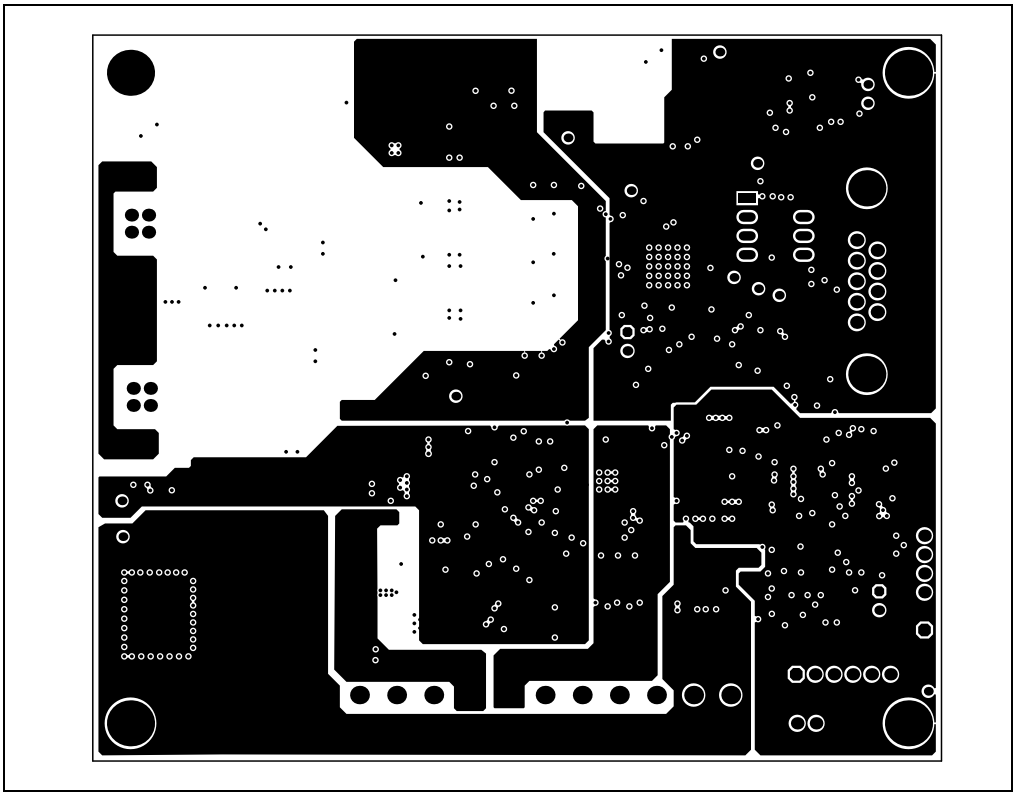


FIGURE 4-4: SIGNAL LAYER

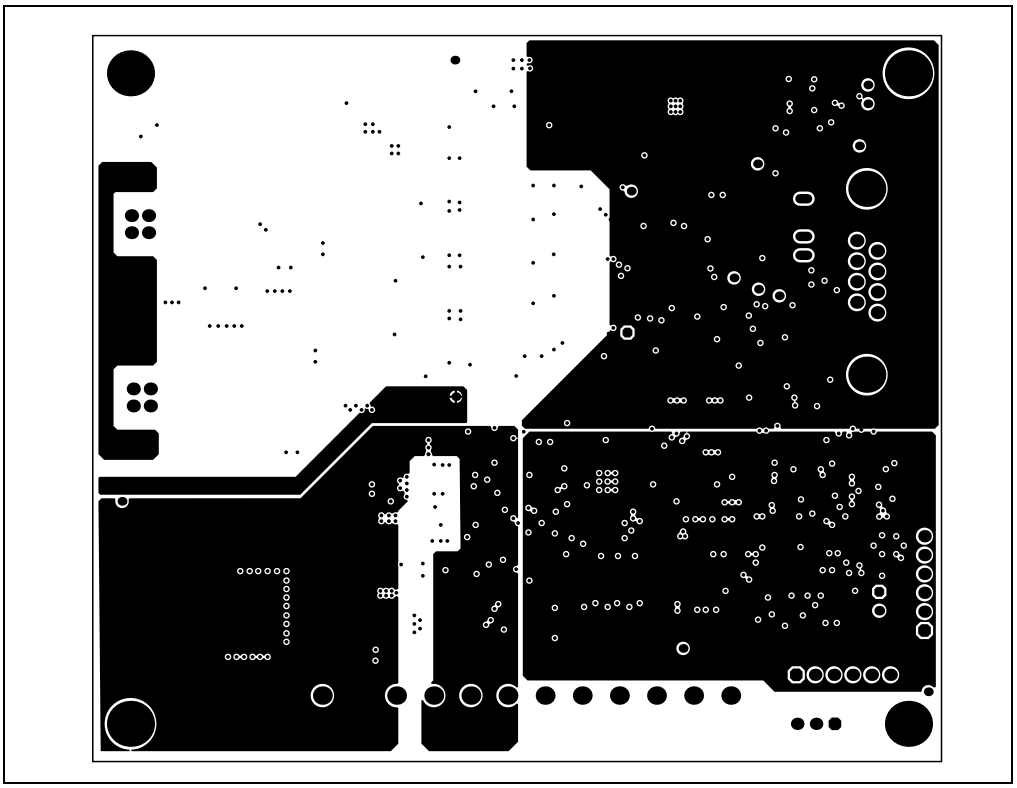


FIGURE 4-5: POWER LAYER

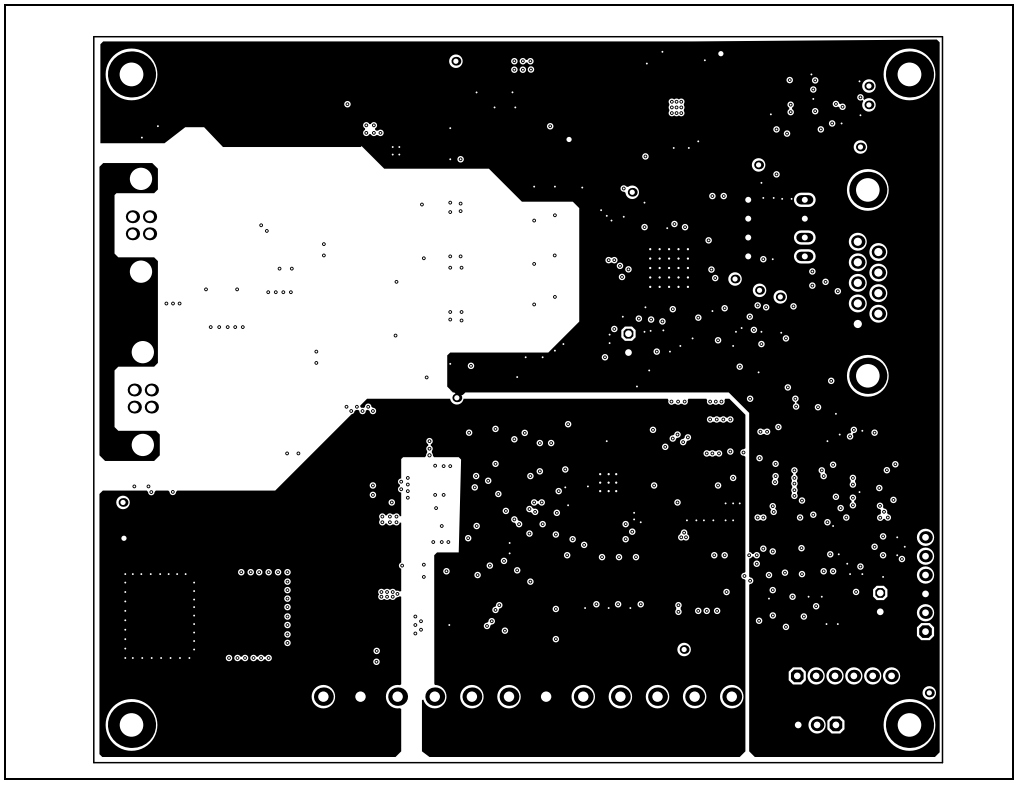
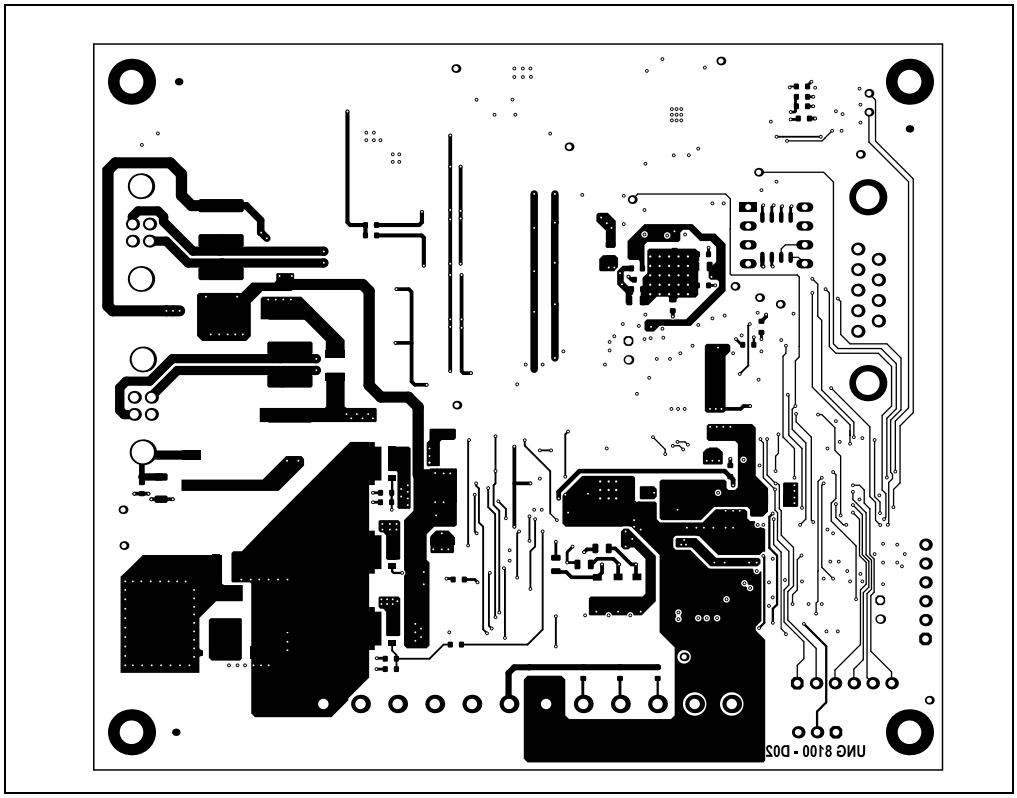


FIGURE 4-6: SIGNAL LAYER

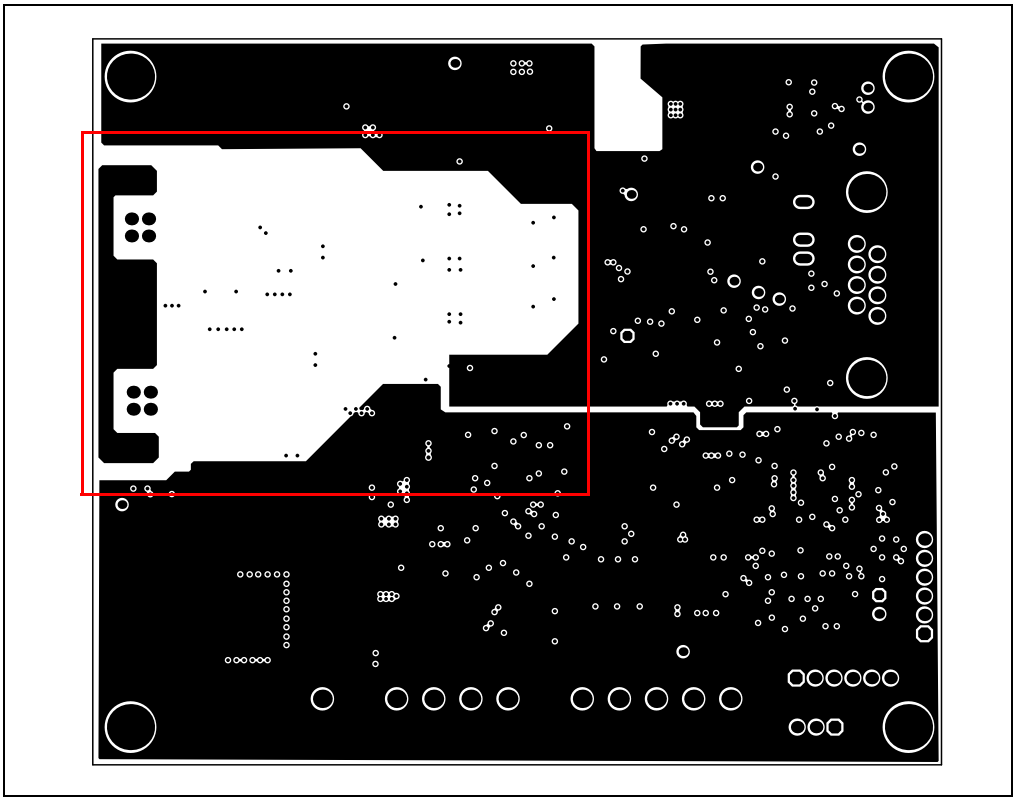


4.1.1 Baseline Wander

EtherCAT is a baseband transmission system where the MLT-3 signals are centered around 0 Hz. In the EtherCAT PHY, the data is passed through the scrambler that allows the signals to be centered around 0 Hz and eliminates the DC offset. The scrambler does this by spreading the signal power more uniformly over the entire channel bandwidth. When a stream of data pattern known as “killer packets” (long periods of +1 or -1) is sent through the EtherCAT cable and the Ethernet transformer, it causes the MLT-3 signals to accumulate a significant DC offset since the transformer is high pass in nature. This causes the signals to drop from baseline or to wander away from the baseline. On the receive side, this signal results in bit error. The LAN9252 ESC corrects the baseline wander (BLW) and can receive ANSI 3 263-1995 FDDI-TD PMD defined killer packet. However, the board layout also plays an important role to correct BLW. A user can follow these recommendations to correct BLW.

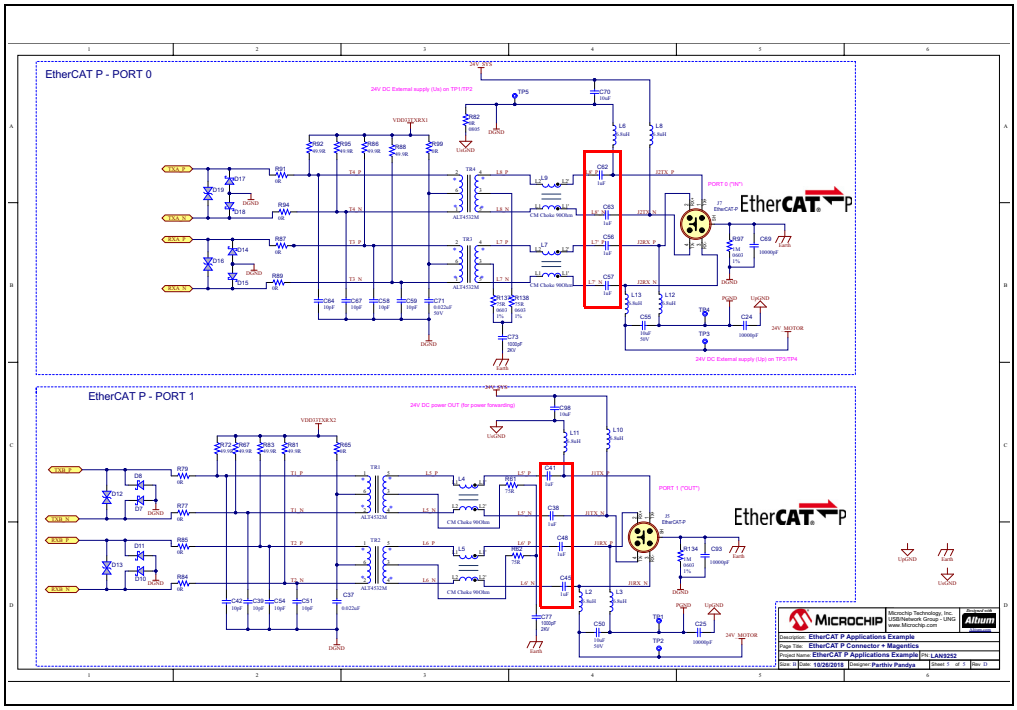
- Avoid referencing Ethernet signals to ground. To do that, in the ground layer (2nd layer), no ground and power plane should be extended under the TX and RX differential pair and magnetics. Figure 4-7 shows the void area in the red square.

FIGURE 4-7: VOID AREA UNDERNEATH ETHERNET SIGNALS



- Increase series capacitor values from 1 µF to 10 µF to improve BLW. Figure 4-8 shows the series capacitors, C56, C57, C62, C63 and C38, C41, C48, C45 in the red square.

FIGURE 4-8: SERIES CAPACITORS



- Use a transformer with minimum 350 uH OCL. Drop in the Ethernet signals is directly related to Ethernet magnetics' open circuit inductance (OCL). An Ethernet transformer with the lower inductance value may result in failure of BLW.
- Minimize the distance between LAN9252 and the EtherCAT P connectors.
- Do not route differential pairs under parts. Do not cross TX/RX lines with other PCB traces unless the differential pair (TX+/- or RX+/-) should be routed away from all other signals and close together.
- Keep both traces of each differential pair as identical to each other as possible.
- Route each differential pair on the same PCB layer.

The example board passes the BLW test by employing the above recommendations.

Chapter 5. Software

5.1 ETHERCAT P® SOFTWARE REQUIREMENTS

Several software components are required, including dsPIC33 SDK, EEPROM programming, and a system application.

5.1.1 dsPIC33 SDK

The dsPIC33 SDK is an EtherCAT software stack for the LAN9252 device written for the dsPIC33 device. The SDK implements the EtherCAT slave functions that can communicate with the EtherCAT master.

The SDK is available from www.microchip.com web site. It includes a quick start guide that explains the steps to:

1. Install TwinCAT (EtherCAT master) drivers on a PC that acts as an EtherCAT master
2. Generate the slave source files using the SSC® tool
3. Integrate dsPIC33EP256MC504 MCU configuration files in the slave source files generated in step 2
4. Compile the MPLAB X® IDE based project and program it on a demo board
5. Scan the EtherCAT slave device from TwinCAT
6. Program EEPROM with ESI
7. Run the example

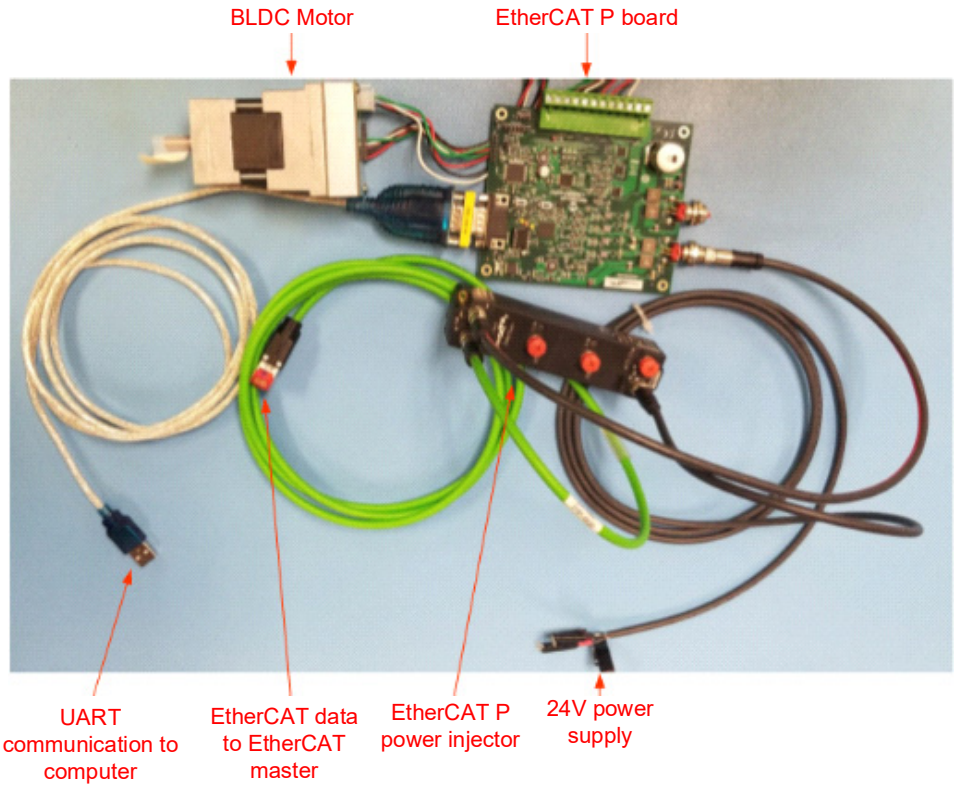
There are several source files required to develop the EtherCAT slave project. To speed up the process, the EtherCAT.org web site provides the SSC tool, which uses a graphical user interface or GUI-based approach to select the required parameters to generate the source files.

5.1.2 EEPROM Programming

Once the SDK is programmed on the dsPIC MCU, the system requires that the on-board EEPROM be programmed with EtherCAT Slave Information (ESI). When the system starts, the EtherCAT master, TwinCAT in this case, reads the LAN9252 ESC profile using the LAN9252's internal register.

5.1.3 Example

FIGURE 5-1: ETHERCAT P SETUP



The system illustrates a motor control application using EtherCAT communication. The application example board is an EtherCAT slave device, which receives data from the EtherCAT master (that is, TwinCAT) and controls the 3-phase BLDC motor. The motor can be switched on and off and can change the speed. For UART communication, the data can be transmitted between TwinCAT and the HyperTerminal PC application.

Chapter 6. Hardware Testing

6.1 INTRODUCTION

During hardware testing, the various system functional blocks should be verified, starting with the power supply.

6.1.1 Power Supply

The MCP16301H input voltage should be tested for the correct 24V supply voltage. Confirm that the output voltage is 3.3V using a digital voltmeter. Also, confirm 3.3V supply voltage to all the digital ICs such as, dsPIC33EP256MC504, MCP8026, LAN9252, and so on. The power supply verification should include verifying the voltage, ripple, and operation under various load conditions, including the maximum rated load.

6.1.2 dsPIC33EP256MC504

A simple software routine should be done on the MCU to test the following parts:

- On-board debug LED. This LED can be used to test if the MCU is running. A small program can be run on the MCU, which causes the debug LED to blink at a particular frequency. This test validates that the MCU is programmed successfully and working properly.
- UART. Successful transmission and reception of data from a PC to the ESC confirms that the UART connections are correct.
- Motor control. Correct connections and component selection for the motor control circuit must be ensured.

Once correct operation of individual parts is verified, the software SDK should be programmed on the board and tested for the complete functionality.

NOTES:

Appendix A. Schematics

This appendix shows the schematics of the EtherCAT P board.

FIGURE A-1: ETHERCAT P® APPLICATION EXAMPLE BLOCK DIAGRAM

EtherCAT P Application Example Board

Revision History

Revision	Date	Revision Summary	Author

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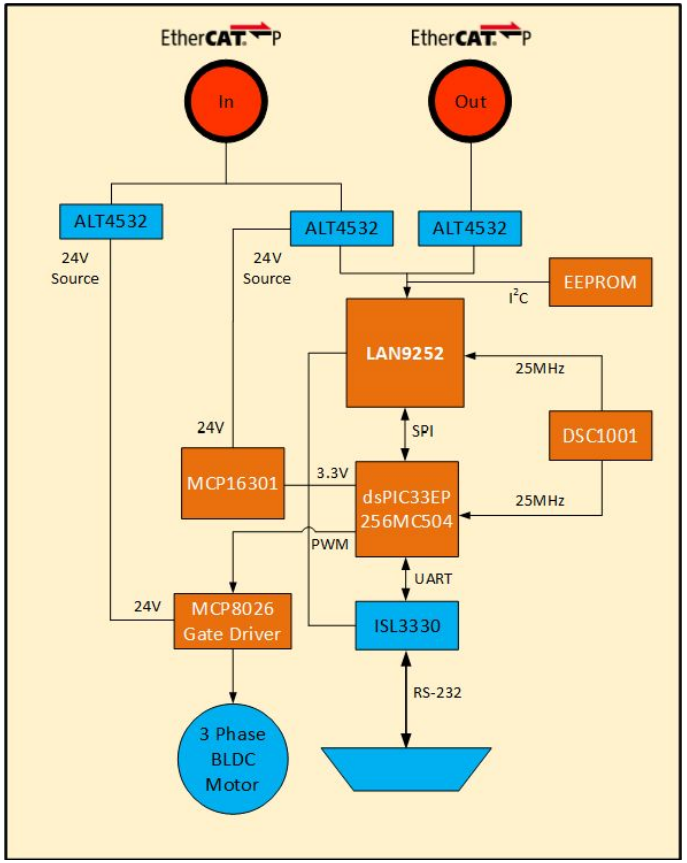
Block Diagram



MICROCHIP	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com		Designed with Altium
Description: EtherCAT P Applications Example			
Page Title: Block Diagram			
Project Name: EtherCAT P Applications Example		PN: LAN9252	
Size: B	Date: 10/26/2018	Designer: Parthiv Pandya	Sheet 1 of 5 Rev D

FIGURE A-2: LAN9252 STRAP AND EEPROM CONNECTIONS

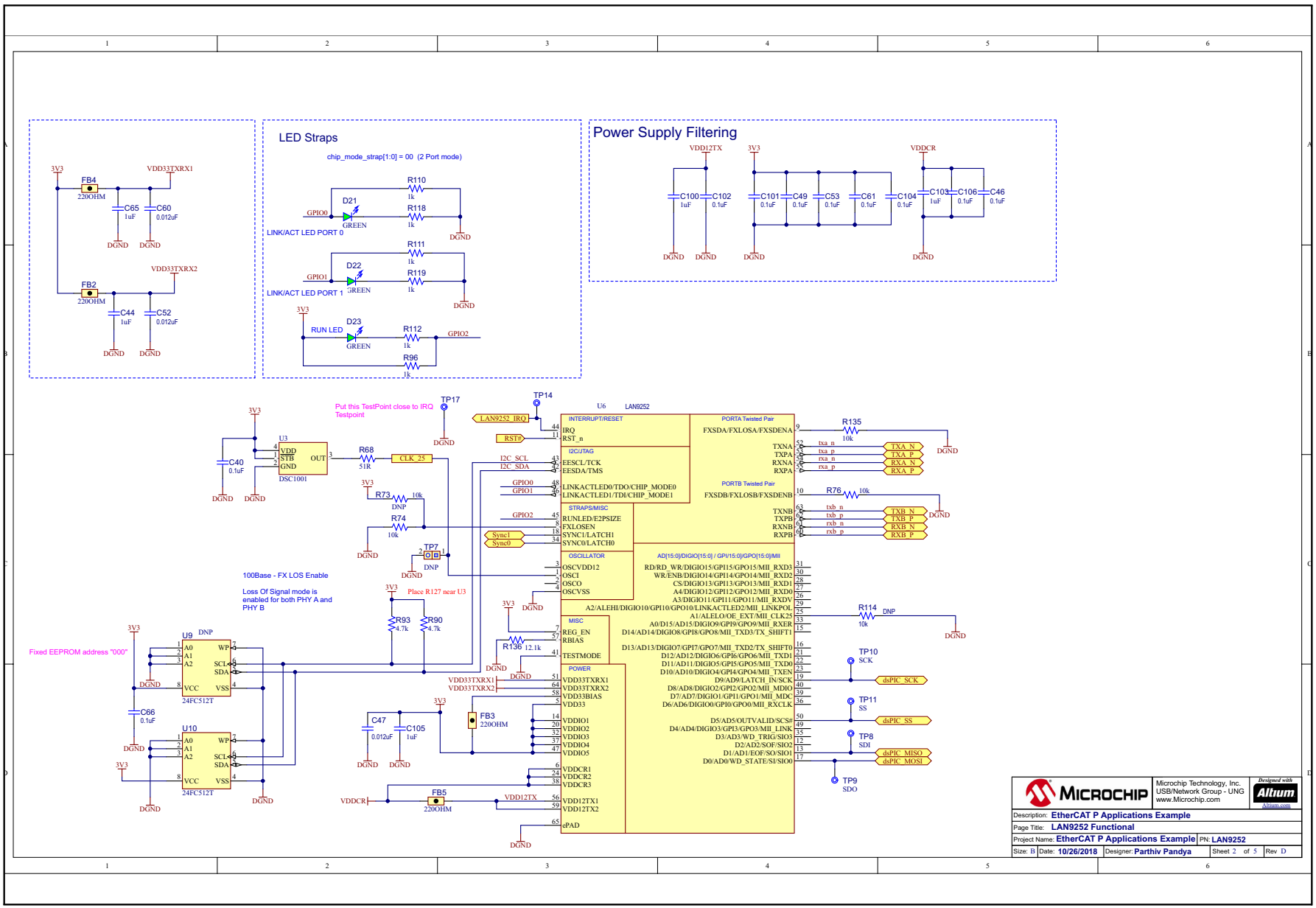


FIGURE A-3: DSPIC33EP FUNCTIONAL AND MOTOR CONTROL

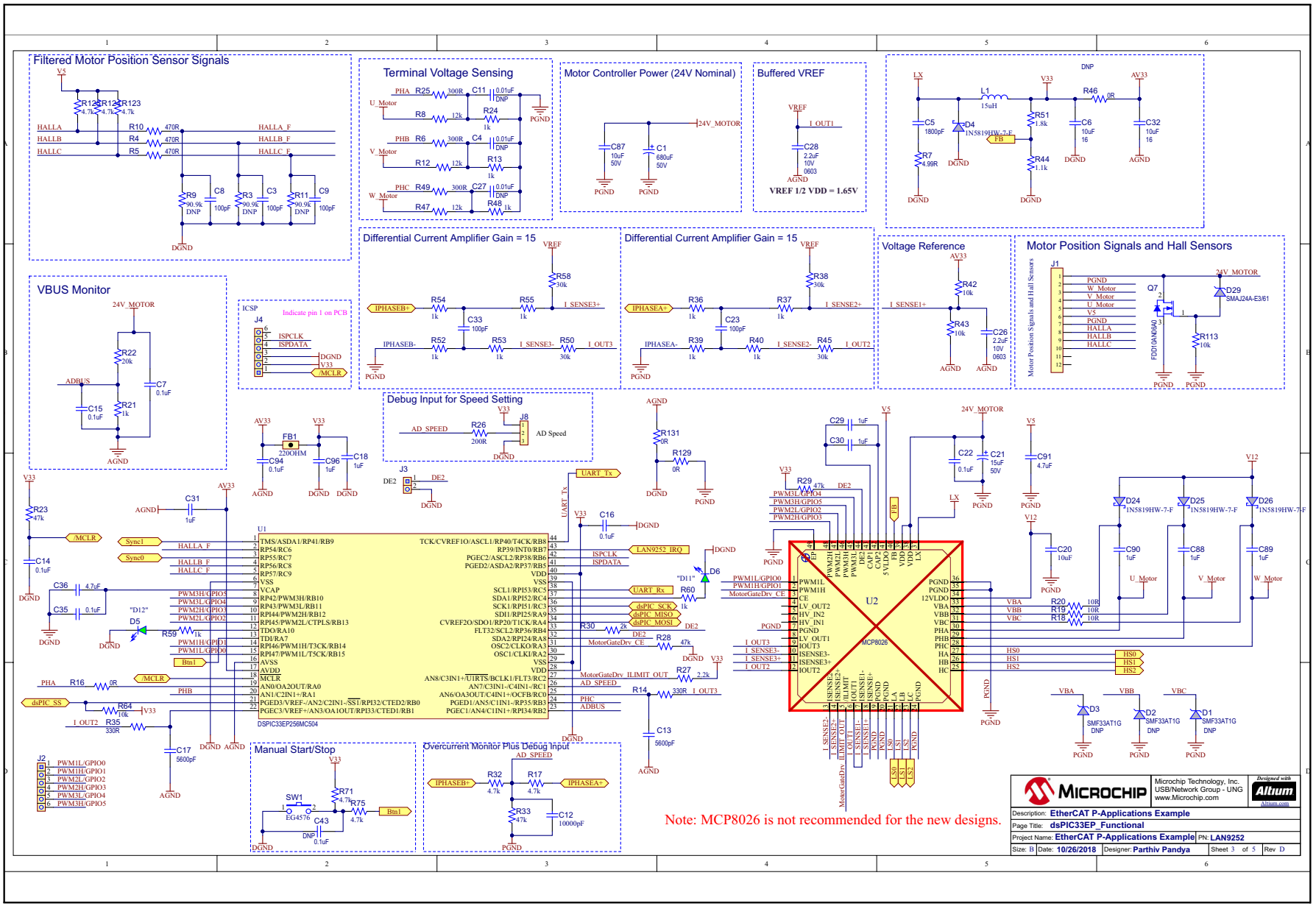


FIGURE A-4: MOSFETS, UART, AND 3.3V REGULATOR

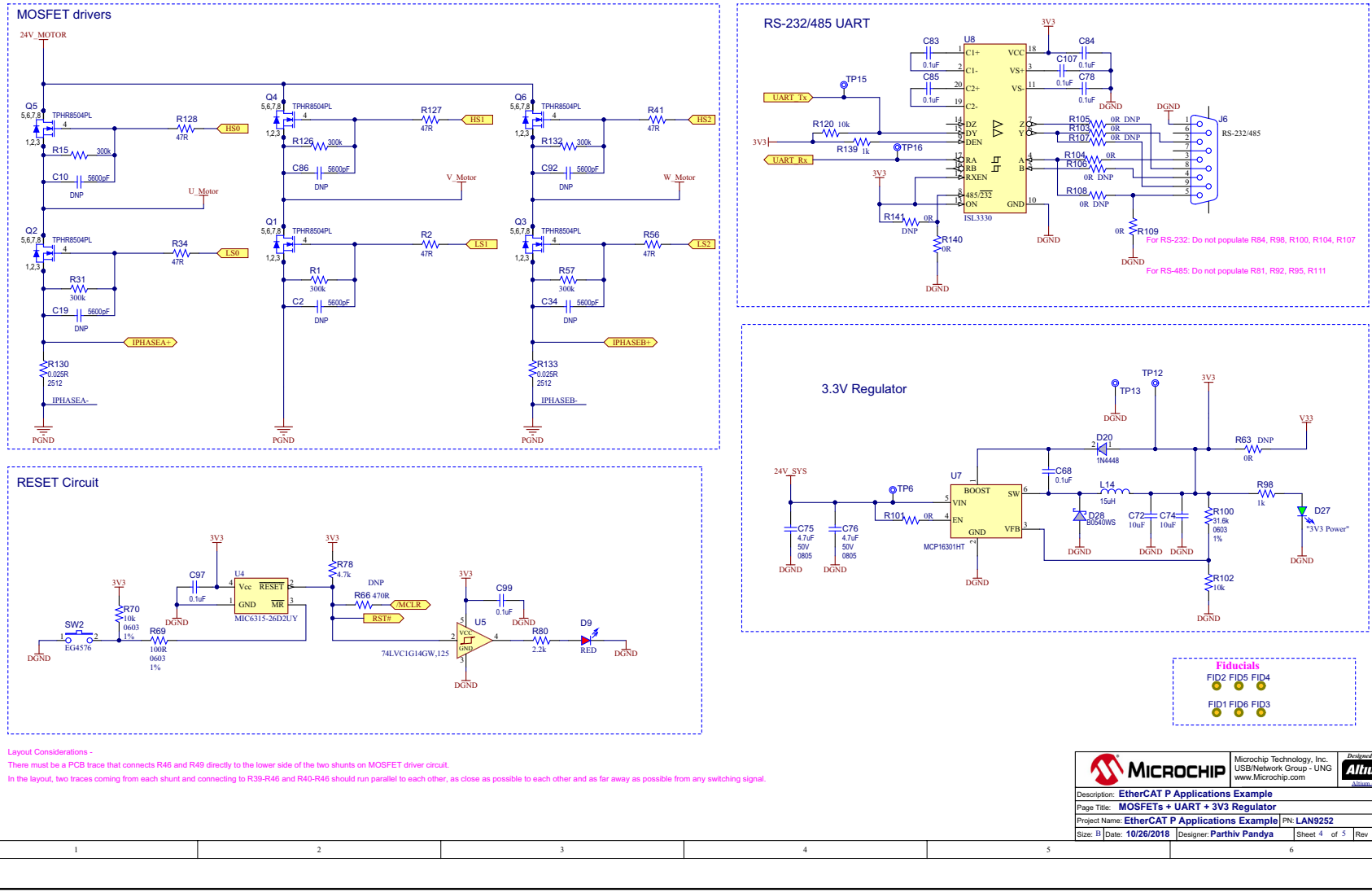
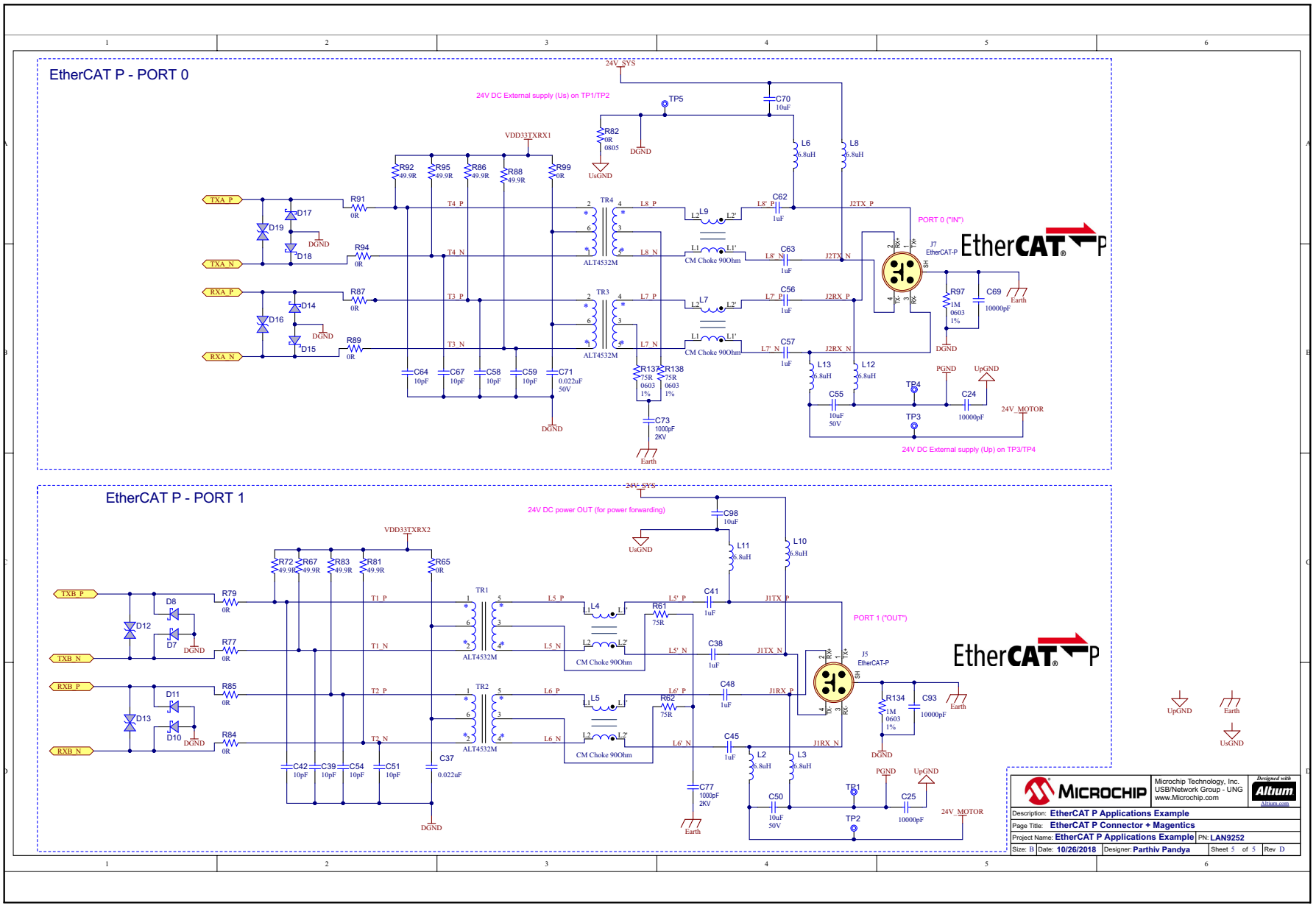


FIGURE A-5: ETHERCAT P® CONNECTORS AND MAGNETICS



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