

# **UCS2112**

# **UCS2112 Silicon Errata**

The UCS2112 parts that you have received conform functionality to the current UCS2112 Data Sheet (DS20005424 $\mathbf{C}$ ), except for the anomalies described in this document.

The silicon issue discussed below is being addressed in the current UCS2113 silicon.

# 1. Module: ALERT#1 and ALERT#2 Output Pins

Both ALERT#1 and ALERT#2 pins are asserted for 100 ns when the UCS2112 enters Sleep state (by connecting both PWR\_EN1 and PWR\_EN2 pins to ground, or by setting the PWR\_EN1S and PWR\_EN2S bits in the configuration registers to '0' and setting PIN\_IGN bit to '1') and when it is coming out of Sleep state.

# Work around 1

Use the UCS2113, which is a pin-for-pin compatible replacement for the UCS2112.

# Work around 2

Filter the 100 ns pulse by adding capacitors to ground on the ALERT#1 and ALERT#2 pins, or by adjusting the input debouncing parameters of the circuit that connects to these lines.

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APPENDIX A: DOCUMENT

**REVISION HISTORY** 

**Rev. A Document (04/2018)** 

• Initial Release of this Document.

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