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## Hardware Design Checklist

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### 1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip PCI12000. These checklist items should be followed when utilizing the PCI12000 in a new design. A summary of these items is provided in [Section 12.0, "Hardware Checklist Summary"](#). Detailed information on these subjects can be found in the corresponding sections:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power and Bypass Capacitance"](#)
- [Section 4.0, "PCIe Signals"](#)
- [Section 5.0, "UART"](#)
- [Section 6.0, "I<sup>2</sup>C/SPI Controllers"](#)
- [Section 7.0, "GPIOs"](#)
- [Section 8.0, "Clock Circuit"](#)
- [Section 9.0, "Power and Startup"](#)
- [Section 10.0, "Configuration"](#)
- [Section 11.0, "Miscellaneous"](#)

### 2.0 GENERAL CONSIDERATIONS

#### 2.1 Required References

The PCI12000 implementor should have the following documents on hand:

- *PCI12000 Data Sheet*
- *AN4255 PCI12000/PCI11xxx Register Map*
- *AN5213 Configuration and Programming Options for the PCI1XXXX*
- *AN4885 Interfacing PCI1xxx with RS-232, RS-422, and RS-485 Through UART*

#### 2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

#### 2.3 Ground

- The ground flag, **GND**, must be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

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## 3.0 POWER AND BYPASS CAPACITANCE

### 3.1 1.1V Supplies

- The analog supplies (**VDD11**) are located on pins 17, 37, 51, and 67 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F shared bulk capacitance placed nearby the device IC.
- The PCIe upstream port 1.1V supplies for Lanes 0-1 (**VDD11PA**) are located on pins 3, 7, 8, 10, and 14 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins that are adjacent and directly shorted together.) All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.
- The PCIe upstream port 1.1V supplies for Lanes 2-3 (**VDD11PB**) are located on pins 28, 32, and 33 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins which are adjacent and directly shorted together.) All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.
- The PCIe downstream port 1.1V supplies (**VDD11PC**) are located on pins 58, 62, and 63 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins which are adjacent and directly shorted together.) All pins should share one 0.1  $\mu$ F bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.

### 3.2 Variable Voltage

- The variable voltage supplies (**VDDVARIO**) are located on pins 25 and 46 and require a connection to a regulated 1.8V to 3.3V power supply. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.

### 3.3 3.3V Supplies

- The general I/O 3.3V voltage supply (**VDD33**) is located on pin 52 and requires a connection to a regulated 3.3V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible (only 1 capacitor is necessary for pins which are adjacent and directly shorted together). All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.
- The general I/O (1) 3.3V voltage supply (**VDD33A0**) is located on pin 52 and requires a connection to a regulated 3.3V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.

### 3.4 2.5V Supplies

- The PCIe upstream port 2.5V voltage supplies for Lanes 0-1 (**VDD25PA**) are located on pins 4, 9, and 13 and require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1  $\mu$ F and one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.
- The PCIe upstream port 2.5V voltage supplies for Lanes 2-3 (**VDD25PB**) are located on pins 29 and 34 and require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.
- The PCIe downstream port 2.5V voltage supplies (**VDD25PC**) are located on pins 59 and 64 and require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 0.1  $\mu$ F bulk capacitor placed nearby the device IC.

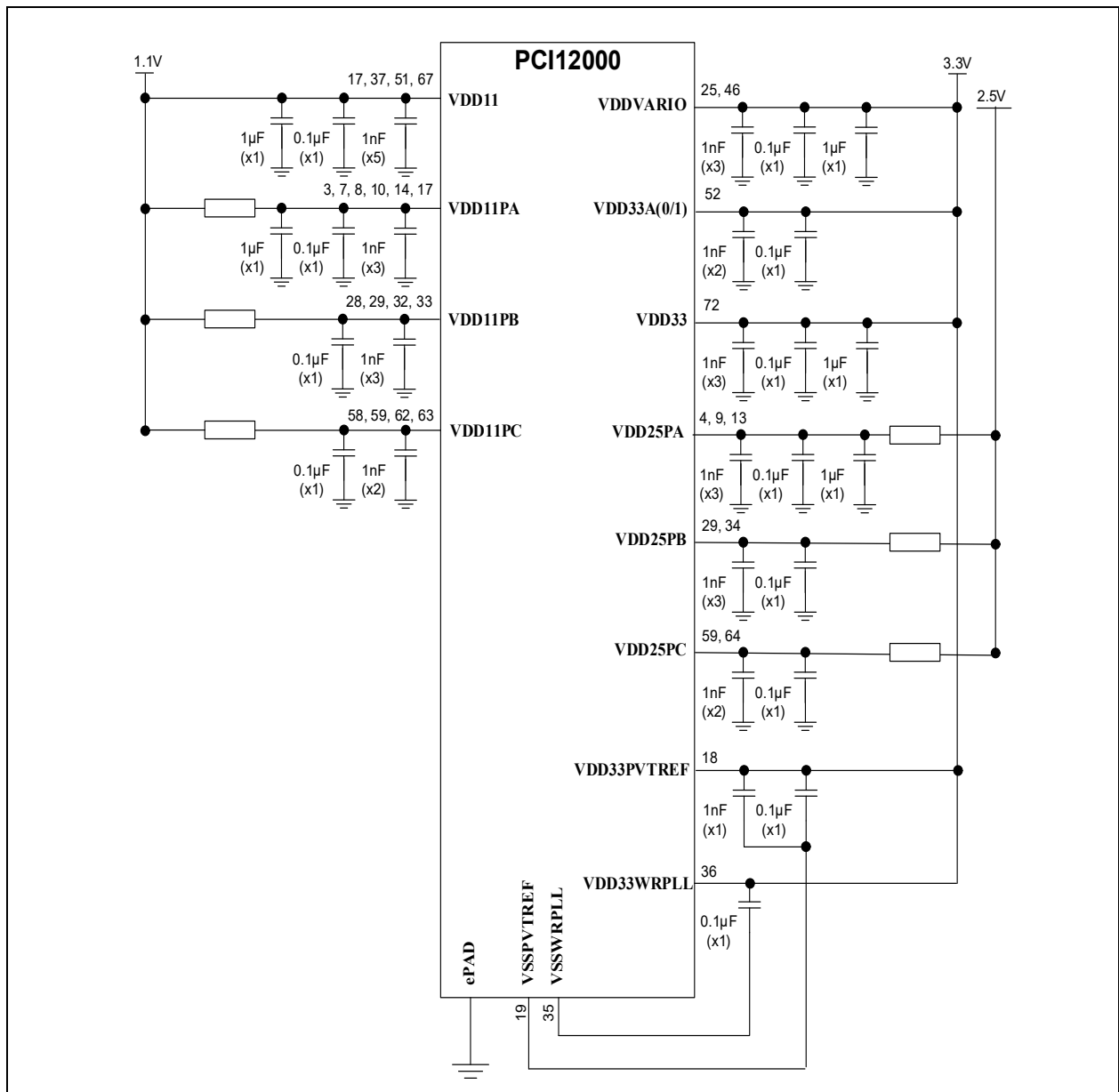
## 3.5 3.3V References

- The 3.3V reference for the internal PVT component (VDD33PVTREF) is located on pin 18 and requires a connection to a regulated 3.3V power plane. This pin should have dedicated 1 nF and 0.1  $\mu$ F capacitors placed as closely to the pin as possible.
- The 3.3V reference for the internal PLL component (VDD33WRPLL) is located on pin 36 and requires a connection to a regulated 3.3V power plane. This pin should have a dedicated 0.1  $\mu$ F capacitor placed as closely to the pin as possible. The opposite end of this capacitor should be directly connected to the VSSWRPLL signal on pin 35 and should not be connected directly to the ground plane.

## 3.6 Power Schematic

The power and ground connections are shown in [Figure 3-1](#).

**FIGURE 3-1: POWER AND GROUND CONNECTIONS**



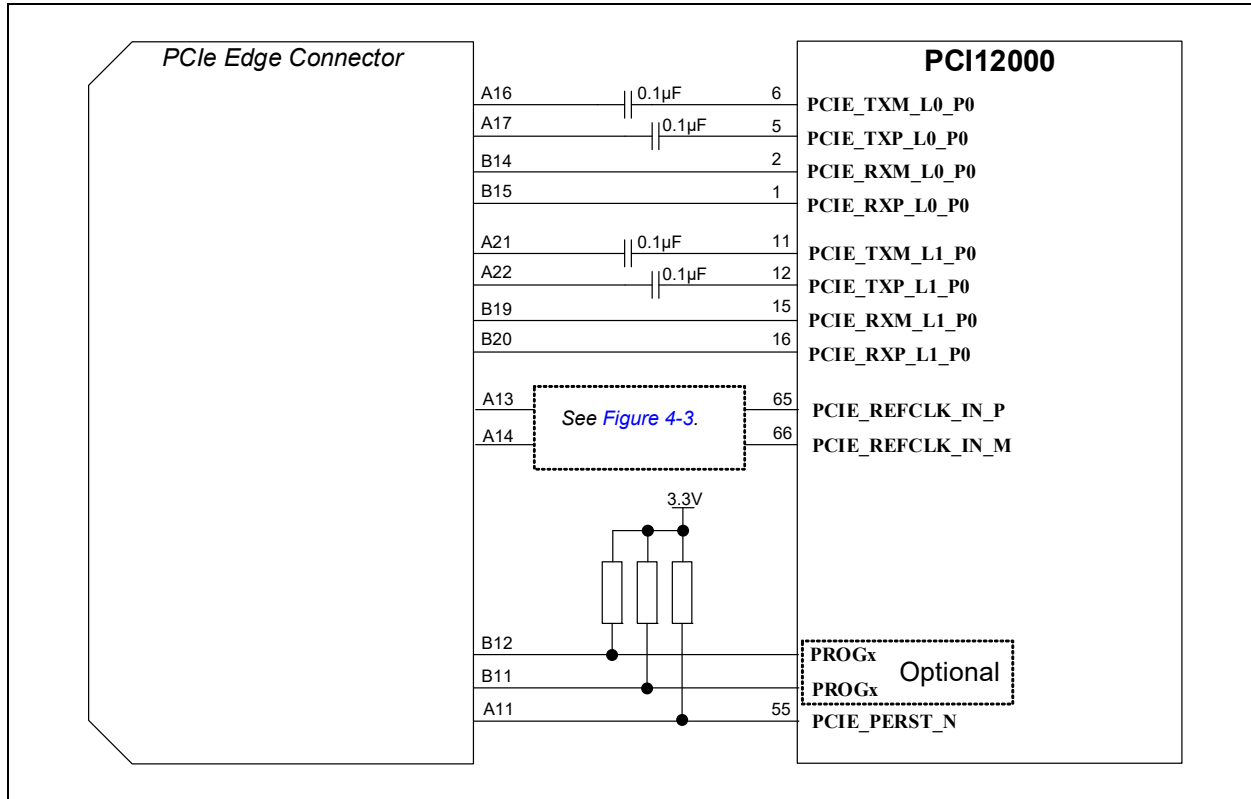
# PCI12000

## 4.0 PCIE SIGNALS

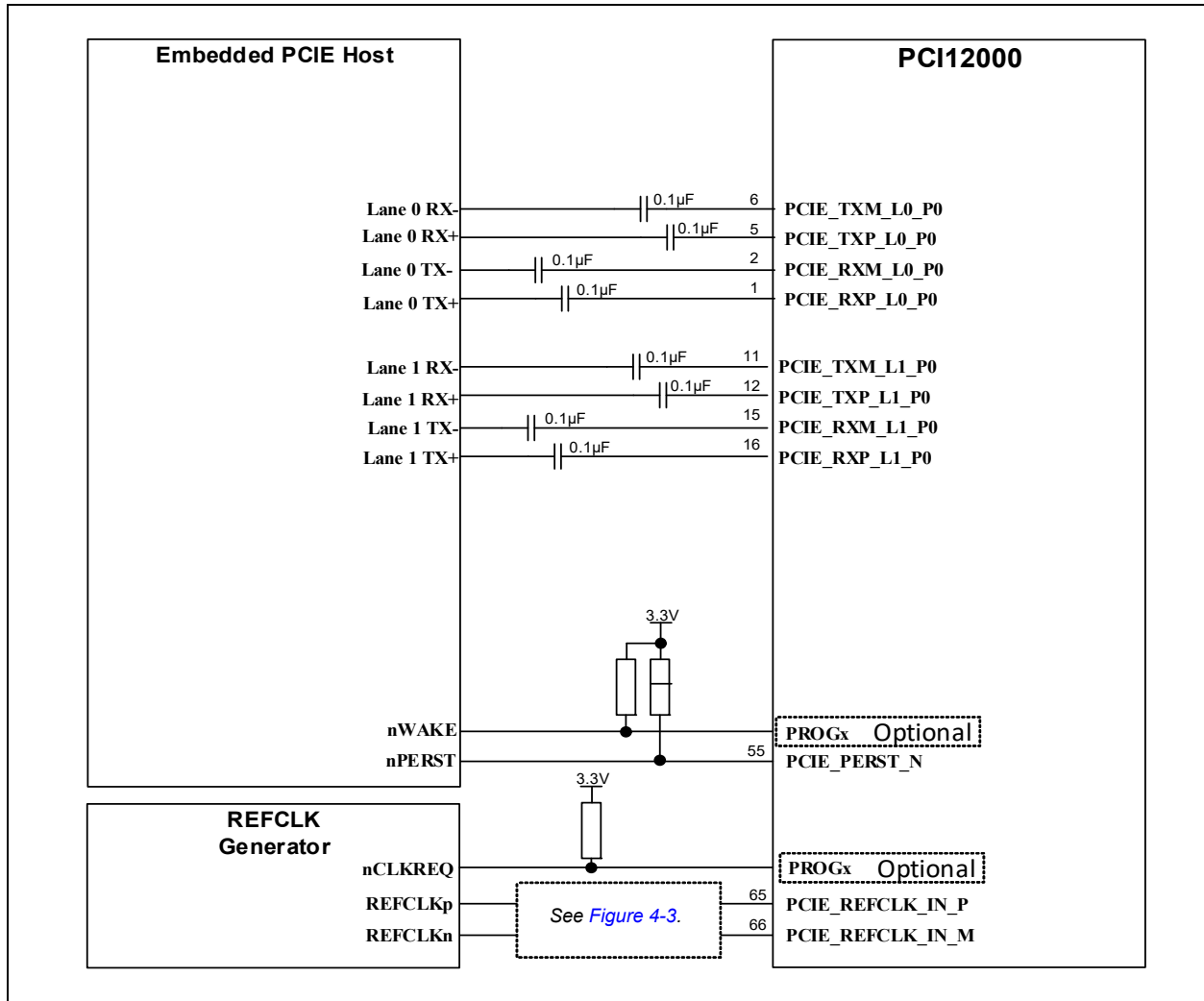
### 4.1 Upstream Port PCIe® Signals

The upstream port PCIe® connections are shown in [Figure 4-1](#) and [Figure 4-2](#).

**FIGURE 4-1: UPSTREAM PORT EDGE CONNECTOR® PCIE CONNECTIONS**



**FIGURE 4-2: UPSTREAM PORT TO EMBEDDED HOST PCIE CONNECTIONS**



## 4.1.1 PCIE PINS

- **PCIE\_TXP\_L0\_P0/PCIE\_TXM\_L0\_P0** (pins 5/6): These pins comprise the PCIe upstream Lane 0 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp0/PERn0** pins of the PCIe edge connector, or the Lane 0 receiver pins of an embedded PCIe host.
- **PCIE\_RXP\_L0\_P0/PCIE\_RXM\_L0\_P0** (pins 1/2): These pins comprise the PCIe upstream Lane 0 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp0/PETn0** pins of the PCIe edge connector, or connected to the Lane 0 transmitter pins of an embedded PCIe host through series 0.1 µF decoupling (DC blocking) capacitors.
- **PCIE\_TXP\_L1\_P0/PCIE\_TXM\_L1\_P0** (pins 12/11): These pins comprise the PCIe upstream Lane 1 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp1/PERn1** pins of the PCIe edge connector, or the Lane 1 receiver pins of an embedded PCIe host.

**Note:** These pins may be left floating or unconnected if implementing a 1 Lane PCIe connection.

- **PCIE\_RXP\_L1\_P0/PCIE\_RXM\_L1\_P0** (pins 16/15): These pins comprise the PCIe upstream Lane 1 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp1/PETn1** pins of the PCIe edge connector, or connected to the Lane 1 transmitter pins of an

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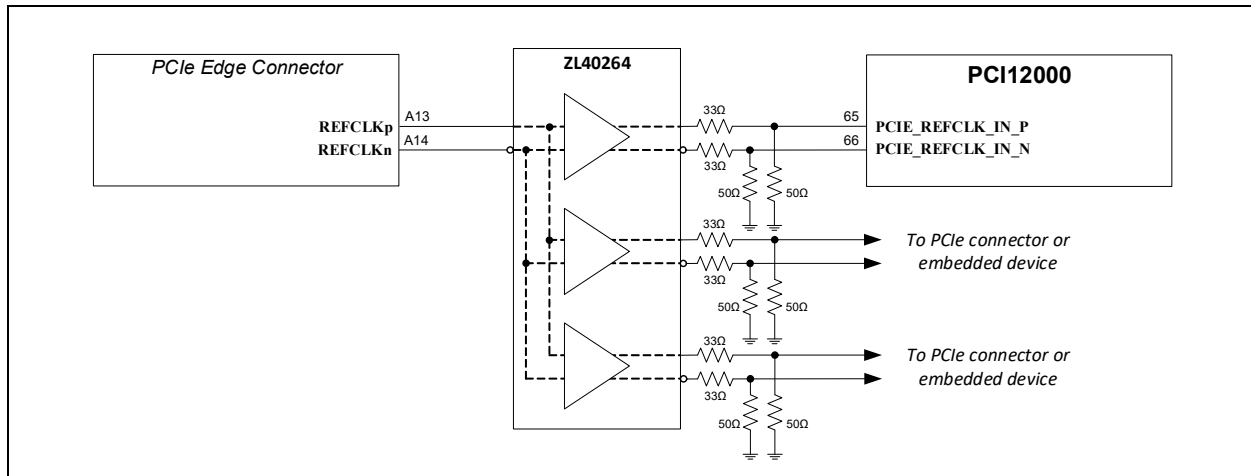
embedded PCIe host through series 0.1  $\mu$ F decoupling (DC blocking) capacitors.

**Note:** These pins may be left floating or unconnected if implementing a 1 Lane PCIe connection.

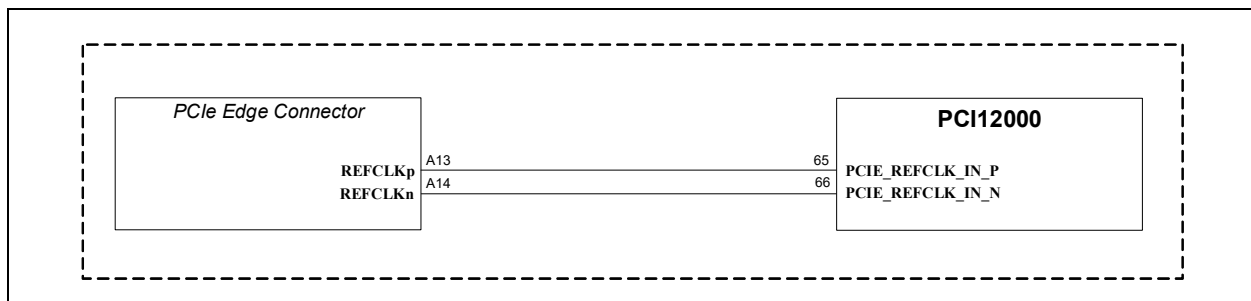
## 4.1.2 REFCLK

- **PCIE\_REFCLK\_IN\_P/PCIE\_REFCLK\_IN\_M** (pins 65/66): These pins comprise the 100 MHz PCIe Differential Reference Clock which is supplied by the PCIe Root Complex port. A PCIe REFCLK buffer device is used to buffer and supply the 100 MHz to the PCI12000 upstream port and PCIe downstream ports, as shown in [Figure 4-3](#). If downstream PCI12000 ports are unused, the PCIe REFCLK pins of the PCIe Edge Connector can connect directly to the PCI12000 without the use of a buffer, as indicated in [Figure 4-4](#).
- The PCI12000 REFCLK pins are LVDS (Low-Voltage Differential Signaling) differential inputs, but PCIe REFCLK sources are normally differential HCSL (High-Speed Current Steering Logic). LVDS and HCSL have different nominal common-mode voltage and nominal voltage swing specifications. The LVDS standard requires a receiver to accept any common mode of 0V to 2.4V. The HCSL TX common mode is within the range of acceptable common-mode voltages for LVDS, and the REFCLK receiver of PCI12000 is capable of recovering a clock which is transmitted with HCSL voltage swing. [Figure 4-3](#) illustrates an implementation using a Microchip ZL40264 clock buffer, which implements HCSL outputs. [Figure 4-4](#) shows an example of REFCLK being sourced directly from an edge connector, which is always expected to be an HCSL clock source.

**FIGURE 4-3: REFCLK CONNECTIONS WITH REFCLK BUFFER**



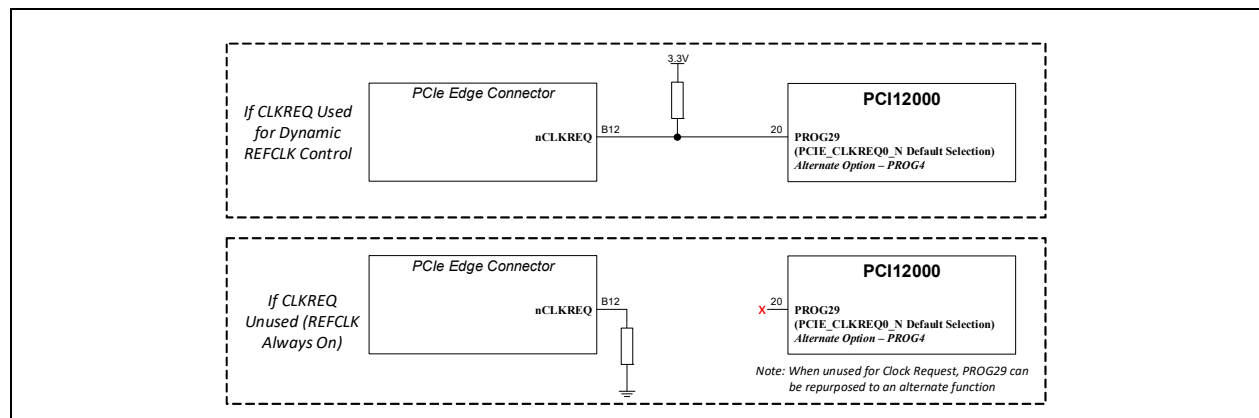
**FIGURE 4-4: REFCLK CONNECTIONS WITH NO BUFFER AND NO DOWNSTREAM PCIE PORTS**



## 4.1.3 CLOCK REQUEST

- The **PCIE\_CLKREQ0\_N** pin function (which is assigned to PROG29 in PCI12000 by default) is an optional pin function used to allow for dynamic REFCLK request. This functionality is necessary to support L1 substates (L1.1 and L1.2). If L1 substates are unsupported, this pin function can be left unused in the end application while pulling the **nCLKREQ** pin on the edge connector to **GND** to force the **REFCLK** output to always remain enabled. The Clock Request options are displayed graphically in [Figure 4-5](#).

**FIGURE 4-5: UPSTREAM PORT CLOCK REQUEST OPTIONS**



If utilizing the dynamic Clock Request functionality:

- A programmable pin function must be selected and programmed into the PCI12000 device via the preferred method (EEPROM or OTP memory).
- The selected pin on the PCI12000 device must connect to the PCIe edge connector **nCLKREQ** (pin B12 of a standard PCIe Edge connector).
- An external pull-up resistor to 3.3V should be included.

If not utilizing the dynamic Clock Request functionality:

- The pin on PCI12000 may be left floating (if leaving the default selection of PROG29 unchanged) or left unassigned.
- The **nCLKREQ** pin on the PCIe Edge connector should be pulled low to ensure that the REFCLK is always output.

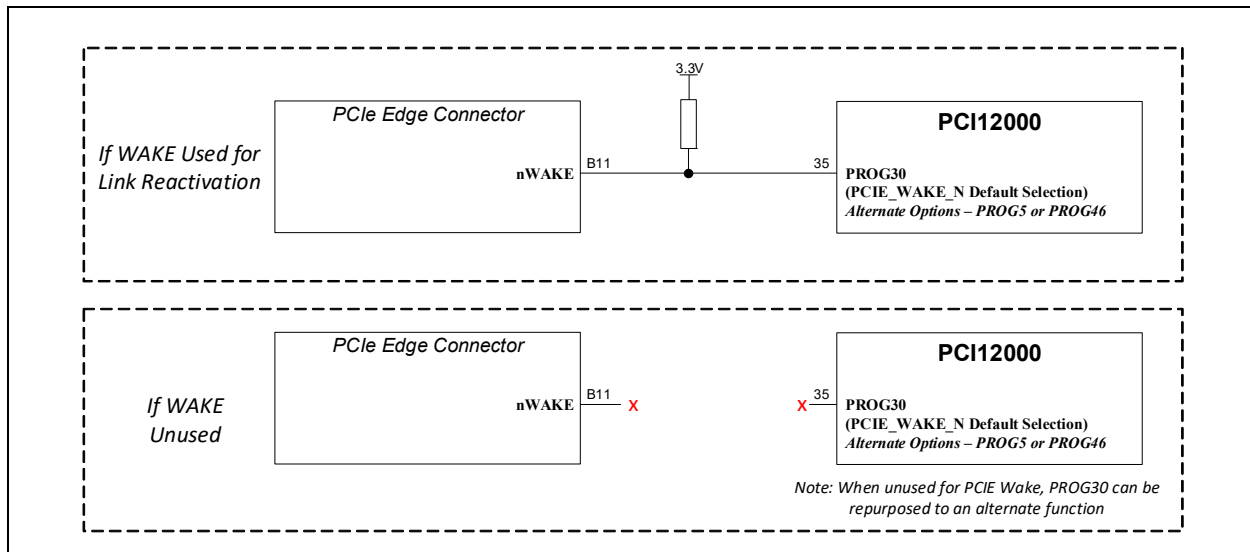
## 4.1.4 WAKE

- The **PCIE\_WAKE\_N** pin function (which is assigned to PROG30 in PCI12000 by default) is an optional pin function used to allow for link reactivation from the D3cold Low-power state. Support of the **PCIE\_WAKE\_N** is optional.

The Clock Request options are displayed graphically in [Figure 4-6](#).

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FIGURE 4-6: UPSTREAM PORT WAKE OPTIONS



If utilizing the Wakeup functionality:

- A programmable pin function must be selected and programmed into the PCI12000 device via the preferred method (EEPROM or OTP memory), or left with the default selection of PROG30.
- The selected pin on the PCI12000 device must connect to the PCIe edge connector **nWAKE** (pin B11 of a standard PCIe Edge connector).
- An external pull-up resistor to 3.3V should be included.

If not utilizing the Wakeup functionality:

- The pin on PCI12000 may be left floating (if leaving the default selection of PROG30 unchanged) or left unassigned.
- The **nCLKREQ** pin on the PCIe Edge connector should be pulled low to ensure that the **REFCLK** is always output.

## 4.1.5 PERST

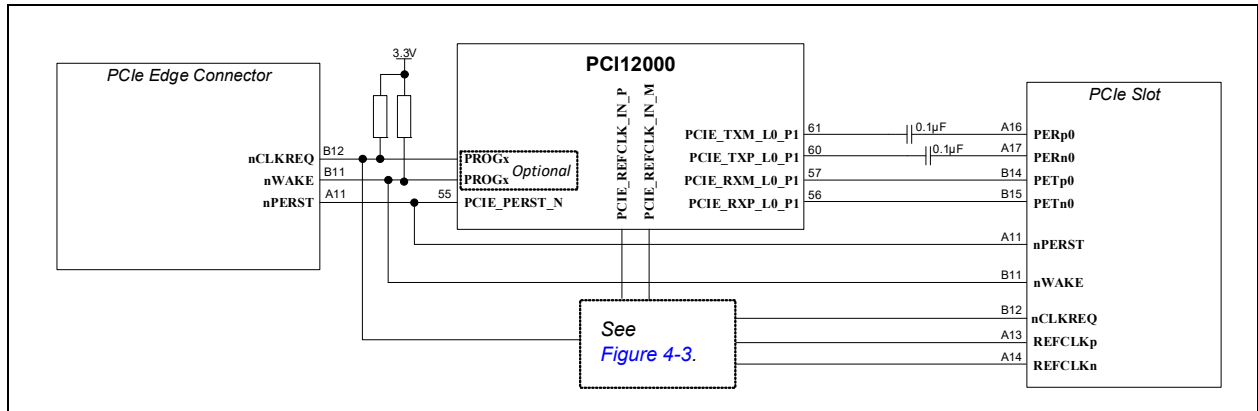
- **PCIE\_PERST\_N** (pin 55): PERST should always be connected directly to the edge connector or directly to the PERST control output of the embedded host. An external pull-up resistor may be required for certain systems, such as when PCI12000 is directly connected to an embedded host. For standard PCIe edge card use-cases, it is assumed that the PCIe host board implements the PERST pull-up resistor.

## 4.2 Downstream Port PCIe Signals

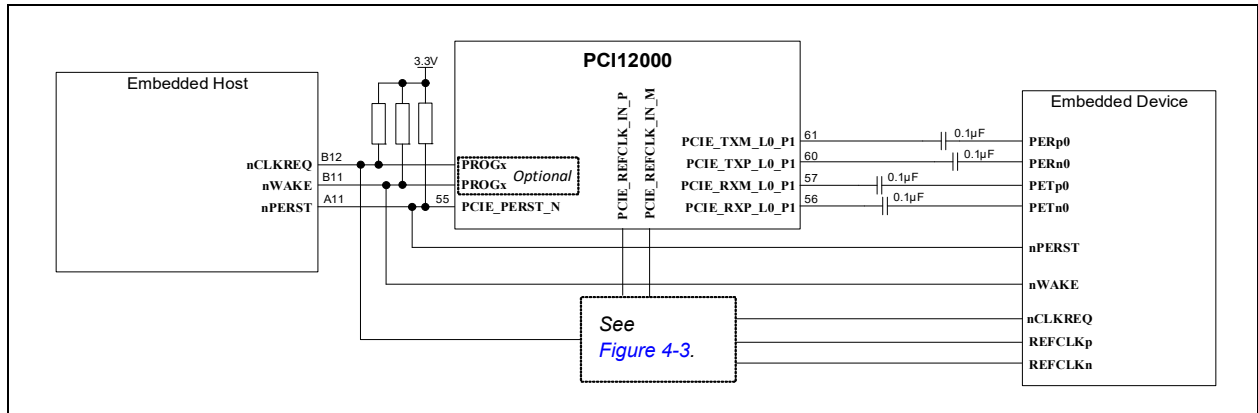
The PCI12000 has two, one-lane downstream PCIe ports. This downstream ports can be connected in a number of ways:

- To a standard PCIe slot, as shown in [Figure 4-7](#).
- To an embedded PCIe device, as shown in [Figure 4-8](#).
- To an alternate PCIe connector (i.e.: Mini PCIe, M.2, SD Express card, etc.). Consult relevant standards documents and reference designs for more details on how to implement these connections. Contact Microchip support for additional resources.

**FIGURE 4-7: STANDARD DOWNSTREAM PCIE PORT SLOT IMPLEMENTATION**



**FIGURE 4-8: EMBEDDED DOWNSTREAM PCIE PORT IMPLEMENTATION**



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## 5.0 UART

There are four UART interfaces available on the PCI12000. Each interface includes full flow control signals which may be optionally used, as well as an optional wake signal to allow for UART devices to wake the PCI12000.

Each interface can connect to one of the following:

- Direct to an embedded device
- An RS-232 Transceiver
- An RS-485 Transceiver
- An RS-422 Transceiver

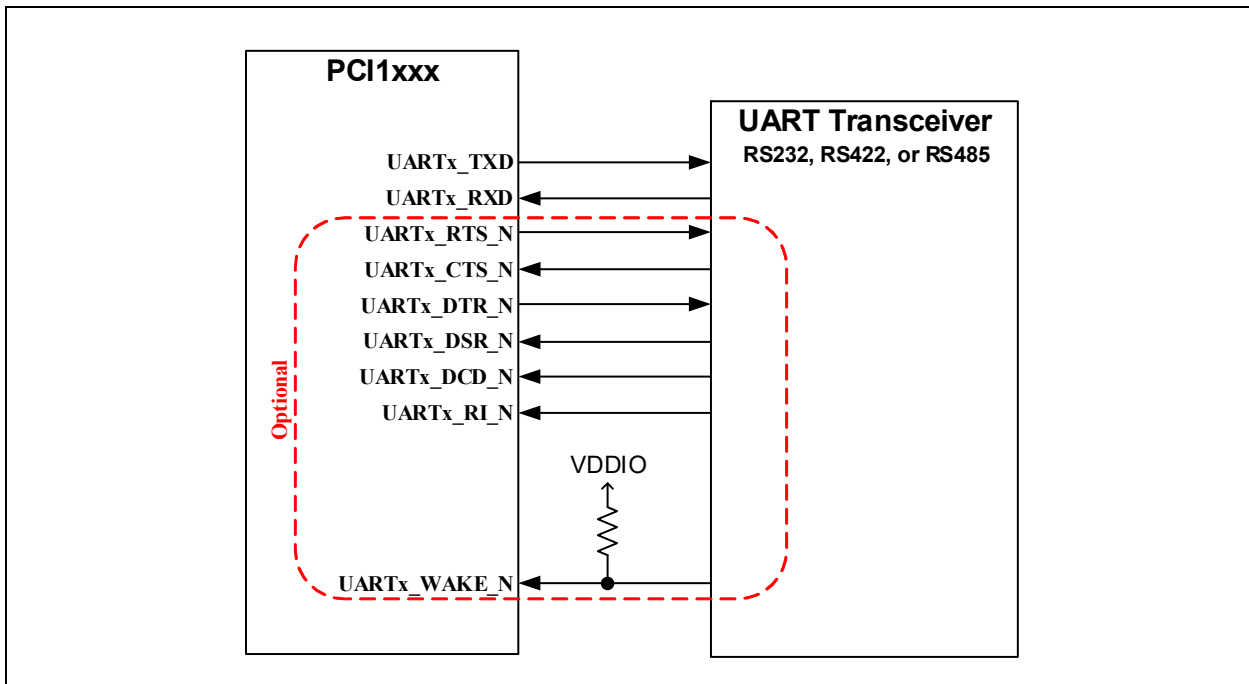
In general, UART signals connect to the transceiver according to [Figure 5-1](#). Each transceiver may have additional requirements and connections.

Transceivers make use of the UARTx\_TXD (transmit), UARTx\_RXD (receive), UARTx\_RTS\_N (ready to send), and UARTx\_CTS\_N (clear to send) signals.

Consult the data sheet for the selected transceiver for additional guidance.

In general, a UART can be part of a data terminal equipment (DTE) or a data circuit-terminating equipment (DCE). A DTE is assumed to be the controlling piece of hardware (such as a computer), and the DCE is assumed to be the receiving piece of hardware (such as a modem or terminal). For additional information on this, refer to Section 3.0 of the *AN4885 Interfacing PCI1xxx with RS-232, RS-422, and RS-485 Through UART*.

**FIGURE 5-1: PCI12000 UART CONNECTIONS**



**TABLE 5-1: UART0 INTERFACE PINS**

Option	UART0_TXD		UART0_RXD		UART0_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	29	20	30	21	31	22
Option 2	69	47	70	48	64	38
Option 3	70	48	71	49	72	50
Option 4	71	49	72	50	75	68
Option	UART0_CTS_N		UART0_DTR_N		UART0_DSR_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	32	23	31	22	29	20
Option 2	65	39	64	38	32	23
Option 3	71	49	75	68	65	39
Option 4	76	69	—	—	76	69
Option	UART0_DCD_N		UART0_RI_N		UART0_WAKE_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	30	21	31	22	31	22
Option 2	—	—	—	—	68	42
Option 3	—	—	—	—	69	47
Option 4	—	—	—	—	75	68
Option 5	—	—	—	—	78	71

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**TABLE 5-2: UART1 INTERFACE PINS**

Option	UART1_TXD		UART1_RXD		UART1_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	31	22	32	23	33	24
Option 2	69	47	70	48	72	50
Option 3	77	70	78	71	—	—
Option	UART1_CTS_N		UART1_DTR_N		UART1_DSR_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	30	21	33	24	72	50
Option 2	71	49	71	49	—	—
Option	UART1_DCD_N		UART1_RI_N		UART1_WAKE_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	—	—	—	—	29	20
Option 2	—	—	—	—	32	23
Option 3	—	—	—	—	68	42
Option 4	—	—	—	—	69	47
Option 5	—	—	—	—	70	48

**TABLE 5-3: UART2 INTERFACE PINS**

Option	UART2_TXD		UART2_RXD		UART2_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	64	38	65	39	31	22
Option	UART2_CTS_N		UART2_DTR_N		UART2_DSR_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	32	23	31	22	32	23
Option	UART2_DCD_N		UART2_RI_N		UART2_WAKE_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	33	24	—	—	64	38
Option 2	—	—	—	—	71	49
Option 3	—	—	—	—	—	—

**TABLE 5-4: UART3 INTERFACE PINS**

Option	UART3_TXD		UART3_RXD		UART3_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	66	40	67	41	—	—
Option	UART3_DCD_N		UART3_RI_N		UART3_WAKE_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	—	—	—	—	65	39

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## 6.0 I<sup>2</sup>C/SPI CONTROLLERS

The The PCI12000 has one I<sup>2</sup>C/SMBus and two SPI controller interfaces available for controlling embedded devices from the PCIe host. The PCI12000 is capable of supporting all of the interfaces in parallel.

**Note:** For guidance on I<sup>2</sup>C/SMBus and SPI configuration interfaces, see *AN5213 Configuration and Programming Options for the PCI1XXXX*.

### 6.1 I<sup>2</sup>C/SMBus Controller Interface

- The PCI12000 has an I<sup>2</sup>C/SMBus controller interface that can bridge PCIe commands to I<sup>2</sup>C/SMBus.
- Typically, a pull-up resistor of 1 k $\Omega$  to 10 k $\Omega$  is sufficient, depending on the configured interface speed and total capacitance on I<sup>2</sup>C tree.
- A pull-up voltage of 1.8V to 3.3V is supported.
- Ensure that all I<sup>2</sup>C/SMBus target devices connected to the bus have unique addresses assigned.
- Ensure that the PCI12000 and all I<sup>2</sup>C/SMBus target devices connected to the bus can support the target bus speed. See [Table 6-1](#).

**TABLE 6-1: I<sup>2</sup>C/SMBUS CONTROLLER INTERFACE PINS**

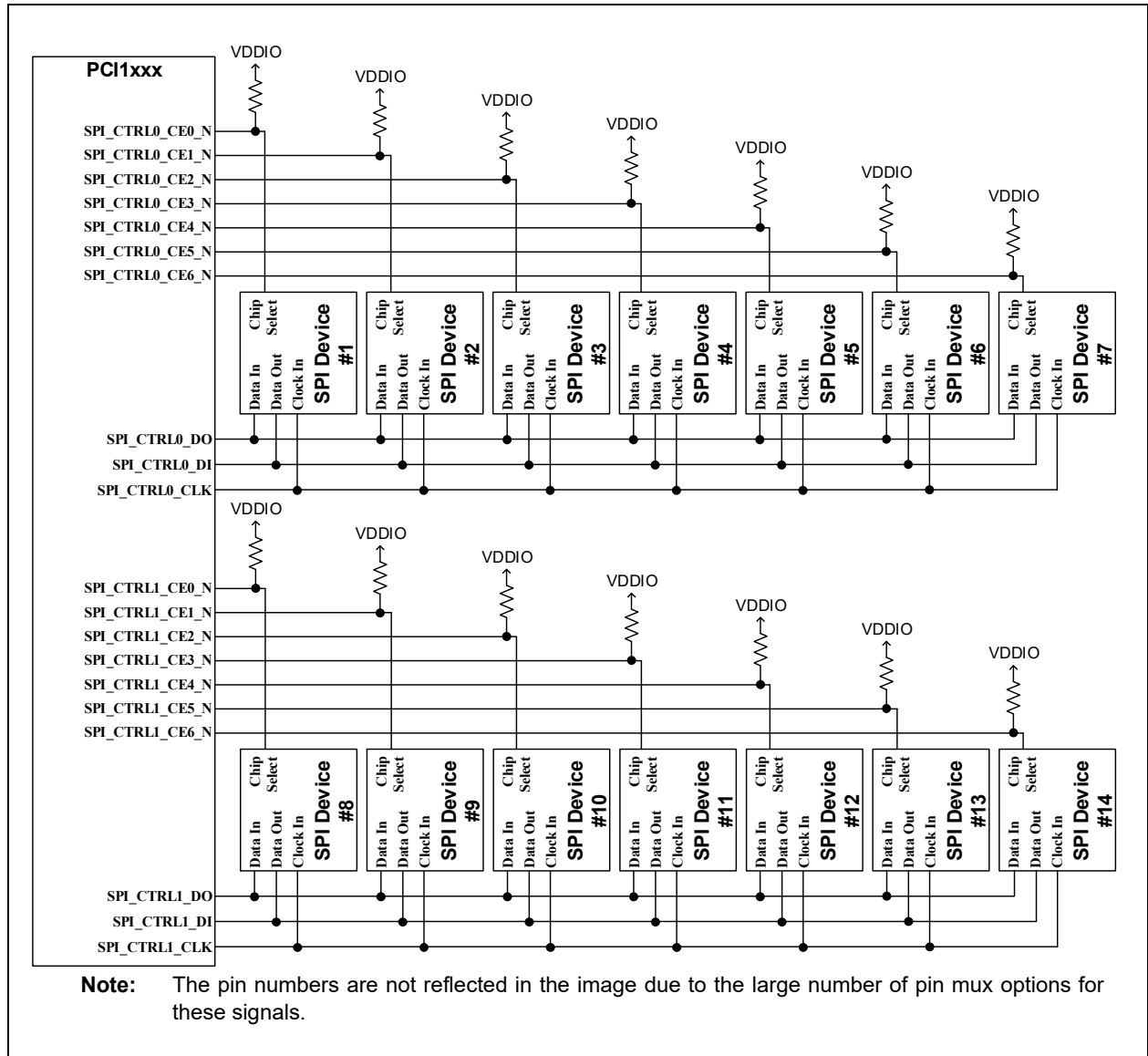
Option	SMBUS_CTLR_SCL		SMBUS_CTLR_SDA		SMBUS_CTLR_ALERT_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG32	23	PROG33	24	PROG66	40
Option 2	PROG64	38	PROG65	39	PROG70	48
Option 3	PROG68	42	PROG69	47	PROG78	71
Option 4	PROG76	69	PROG77	70	—	—

## 6.2 SPI Controller Interface

- The PCI12000 has two SPI controller interfaces that can bridge PCIe commands to I<sup>2</sup>C/SMBus. Each interface has seven separate chip select signals to support up to seven SPI devices per SPI bus.
- An I/O voltage of 1.8V to 3.3V is supported. I/O voltage is set via the **VDDVARIO** supply power pins.
- The PCI12000 SPI controller interface has a configurable signal rate and can support 2 MHz, 10 MHz, 12 MHz, 15 MHz, 20 MHz, 25 MHz, or 30 MHz operation.

An SPI controller implementation is shown in [Figure 6-1](#).

**FIGURE 6-1: PCI12000 SPI CONTROLLER**



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**TABLE 6-2: SPI CONTROLLER 0 INTERFACE PINS**

Option	SPI_CTRL0_DO		SPI_CTRL0_DI		SPI_CTRL0_CLK		SPI_CTRL0_CE0_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG65	39	PROG66	40	PROG64	38	PROG67	41
Option 2	PROG69	47	PROG70	48	PROG71	49	PROG68	42
Option 3	PROG76	69	PROG77	70	PROG75	68	PROG78	71
Option	SPI_CTRL0_CE1_N		SPI_CTRL0_CE2_N		SPI_CTRL0_CE3_N		SPI_CTRL0_CE4_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG31	22	—	—	PROG32	23	PROG32	23
Option 2	PROG69	47	—	—	PROG33	24	PROG64	38
Option 3	PROG72	50	—	—	—	—	PROG68	42
Option	SPI_CTRL0_CE5_N							
	PROG	Pin						
Option 1	PROG33	24						
Option 2	PROG70	48						

**TABLE 6-3: SPI CONTROLLER 1 INTERFACE PINS**

Option	SPI_CTRL1_DO		SPI_CTRL1_DI		SPI_CTRL1_CLK		SPI_CTRL1_CE0_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG30	21	PROG31	22	PROG29	20	PROG32	23
Option 2	PROG65	39	PROG66	40	PROG64	38	PROG67	41
Option 3	PROG76	69	PROG77	70	PROG75	68	PROG78	71
Option	SPI_CTRL1_CE1_N		SPI_CTRL1_CE2_N		SPI_CTRL1_CE3_N		SPI_CTRL1_CE4_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG33	24	PROG68	42	PROG33	24	PROG65	39
Option 2	—	—	—	—	PROG69	47	PROG69	47
Option 3	—	—	—	—	—	—	PROG70	48
Option	SPI_CTRL1_CE5_N		SPI_CTRL1_CE6_N					
	PROG	Pin	PROG	Pin				
Option 1	PROG71	49	PROG64	38				

# PCI12000

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## 7.0 GPIOs

- Every **PROG<sub>x</sub>** pin (PROG29 to PROG78) can be optionally configured as a GPIO for a custom application for the Host controller. For each **PROG<sub>x</sub>** pin, the “func0” pin mux option configures the pin for GPIO use. Other options, “func1” to “func15,” may also configure the pin for GPIO use, depending on the pin. Refer to the *PCI12000 Data Sheet* programmable pin function map for details.
- For each GPIO, it is recommended to configure a default state, which aligns with hardware requirements. Configuration options include:
  - Direction: Input or Output
  - (If Output) Output State: Drive High or Drive Low
  - Pull-up Resistor: Enable or Disable
  - Internal Pull-down Resistor: Enable or Disable
- For unused pins, it is acceptable to leave the pin as a floating input. Users may optionally pull the pin down to ground via external resistor or by enabling the internal pull-down resistor.
- On PCI12000, the following **PROG<sub>x</sub>** pins are not bonded out and, therefore, unusable within an end application:
  - PROG34 to PROG63
  - PROG73 to PROG74

## 8.0 CLOCK CIRCUIT

### 8.1 Crystal and External Clock Connection

A 25.000 MHz ( $\pm 50$  ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *PCI12000 Data Sheet*.

- **XTALI** (pin 43) is the clock circuit input for the PCI12000. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 44) is the clock circuit output for the PCI12000. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, which are based on the total  $C_L$  specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical  $C_1$  and  $C_2$  capacitor values is:

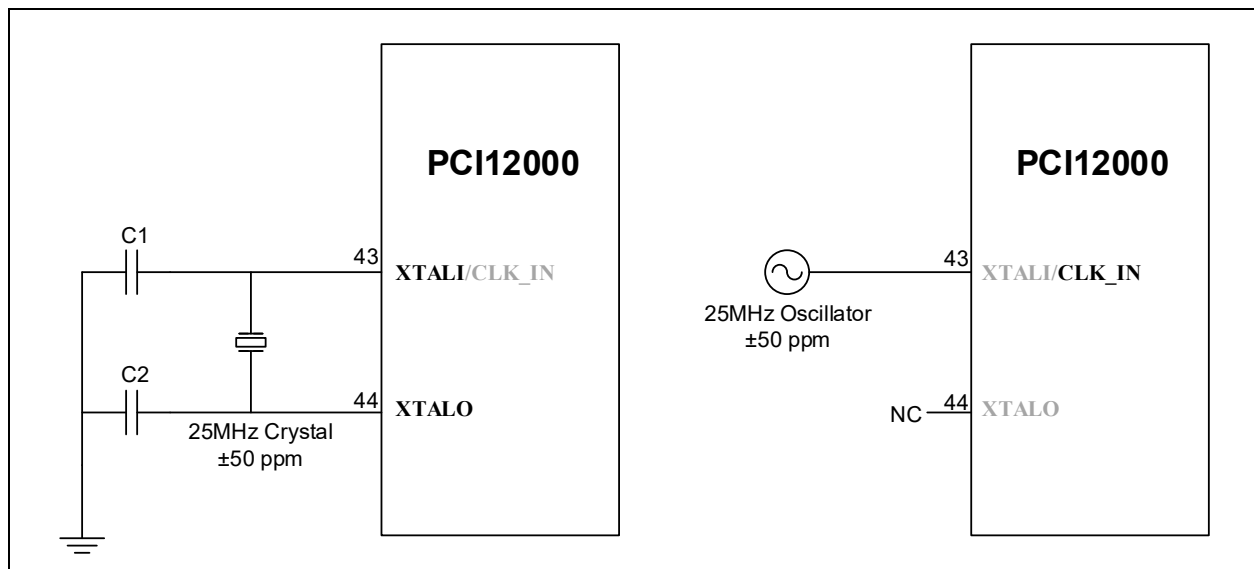
$$C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$$

Where,  $C_L$  is the specification from the crystal data sheet,  $C_{X1} = C_{\text{stray}} + C_1$ ,  $C_{X2} = C_{\text{stray}} + C_2$ .

**Note:**  $C_{\text{stray}}$  is the stray or parasitic capacitance due to PCB layout. It can be assumed to be very small, within the 1 pF to 2 pF range, and verified by physical experiments in the laboratory if PCB simulation tools are not available.

- Alternatively, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the PCI12000. When using a single-ended clock source, **XTALO** (pin 44) should be left floating as a No Connect (NC).

**FIGURE 8-1: CRYSTAL AND OSCILLATOR CONNECTIONS**



# PCI12000

## 9.0 POWER AND STARTUP

### 9.1 Board Power Supplies

#### 9.1.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *PCI12000 Data Sheet*.
- If a monotonic or fast power rail rise cannot be assured, then the **RESET\_N** signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

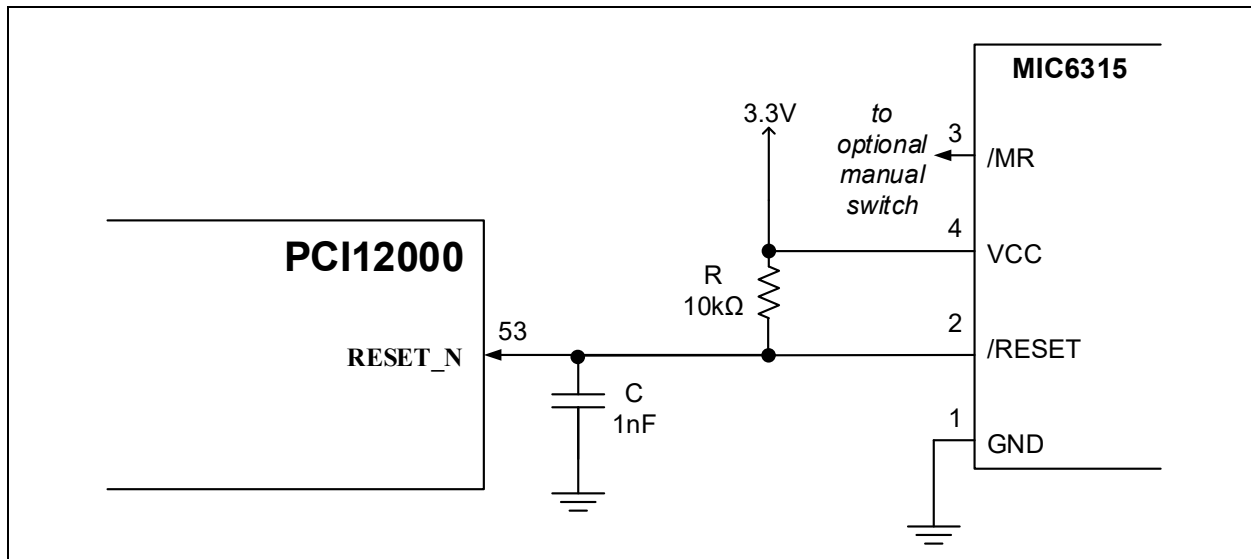
#### 9.1.2 CURRENT CAPABILITY

- The 3.3V and 1.1V power supplies must be able to supply enough power to the PCIE switch. It is recommended that the 3.3V and 1.1V power rails be sized such that they are able to supply maximum power consumption specification as displayed in the *PCI12000 Data Sheet*.

### 9.2 Reset Circuit

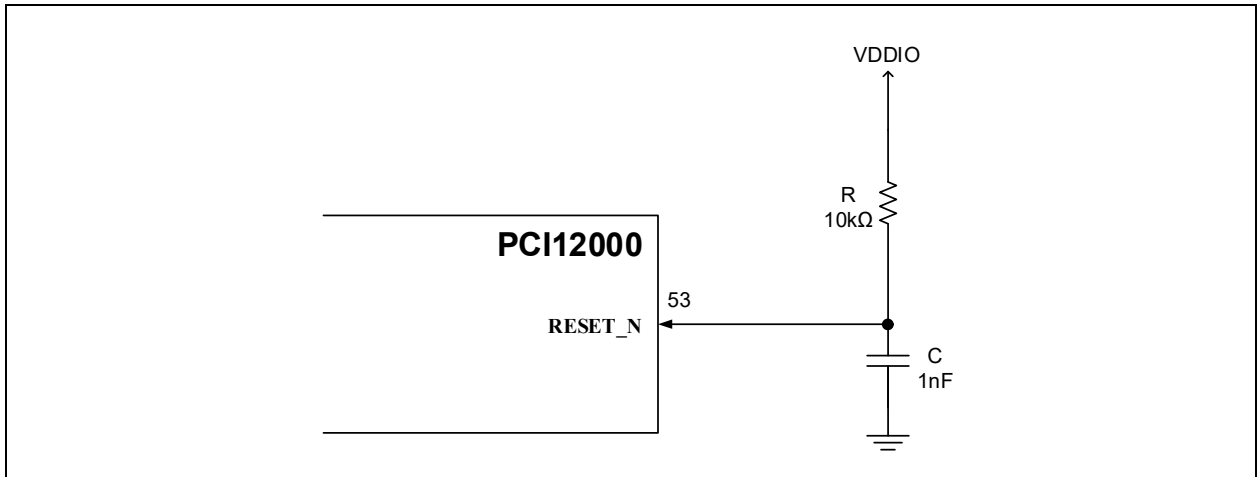
- **RESET\_N** (pin 53) is an active-low Reset input. This signal resets all logic and registers within the PCI12000. A hardware Reset (**RESET\_N** assertion) is not required following power-up. Refer to the latest copy of the *PCI12000 Data Sheet* for Reset timing requirements.
- The best practice for managing **RESET\_N** is to use an external Reset supervisor IC. A Reset supervisor can ensure that the entire system supporting the PCI12000 is properly reset following Fault and Brownout conditions. See [Figure 9-1](#).

**FIGURE 9-1: RESET TRIGGERED BY RESET SUPERVISOR**



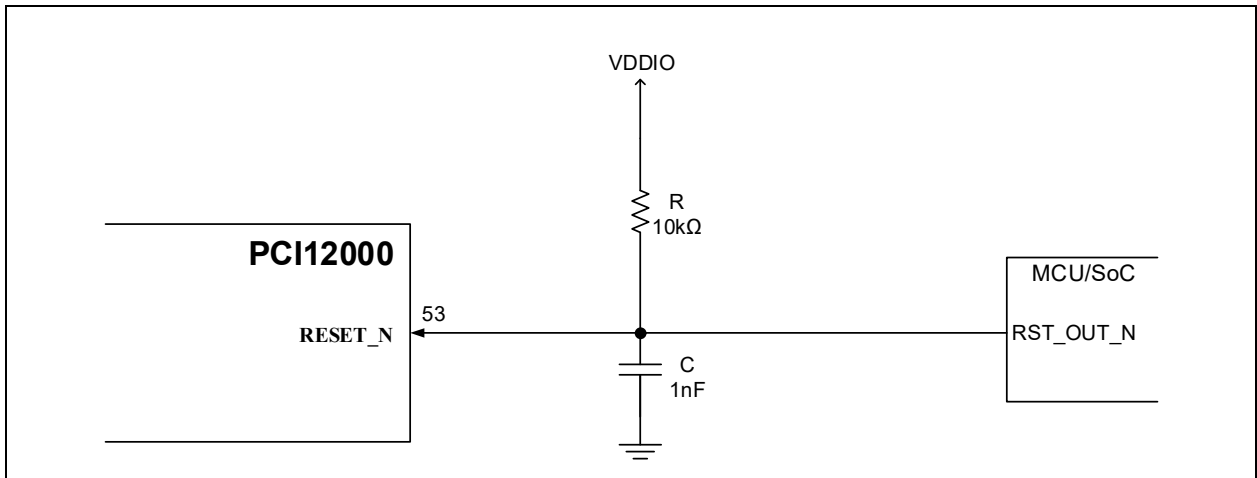
- [Figure 9-2](#) shows a recommended Reset circuit for powering up the PCI12000 when Reset is triggered by the power supply. This implementation is lower cost, but less robust and, therefore, may not be appropriate for many applications as it does not ensure that all system components experience a common Reset event following Fault and power brownout events.

**FIGURE 9-2: RESET TRIGGERED BY POWER SUPPLY**



- [Figure 9-3](#) details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU or equivalent system management controller. The Reset out pin (**RST\_OUT\_N**) from the CPU/MCU provides the warm Reset after power-up.

**FIGURE 9-3: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT**



# PCI12000

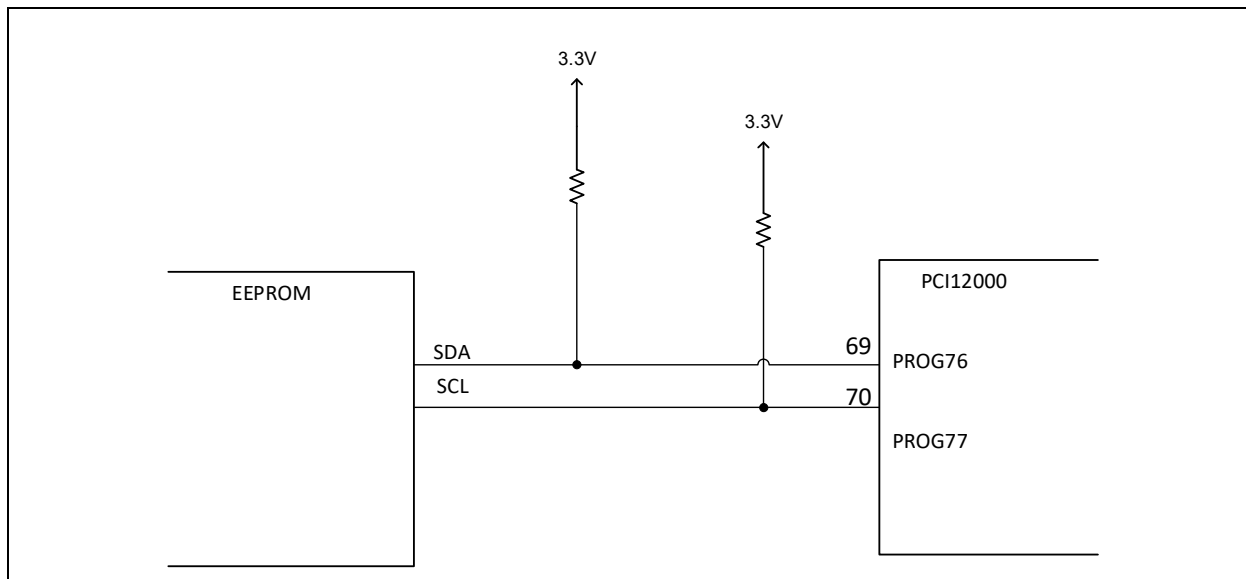
## 10.0 CONFIGURATION

- PCI12000 can be configured from the following sources:
  - EEPROM memory
  - External I<sup>2</sup>C/SMBus controller or SPI controller (PCI12000 cannot be configured via both interfaces.)
- PCI12000 can also be completely or partially configured via internal OTP memory.

### 10.1 EEPROM

- The *PCI12000 Data Sheet* maintains a list of approved compatible EEPROM memory devices. By default, the EEPROM interface expects a 32 Kbit, 1 MHz I<sup>2</sup>C EEPROM. The following strap pins detections are required at startup in order to enter I<sup>2</sup>C/SMBus Configuration mode:
  - EEPROM\_STRAP\_EN = 1
- If configuring via EEPROM, recommended schematic connections are shown in [Figure 10-1](#).

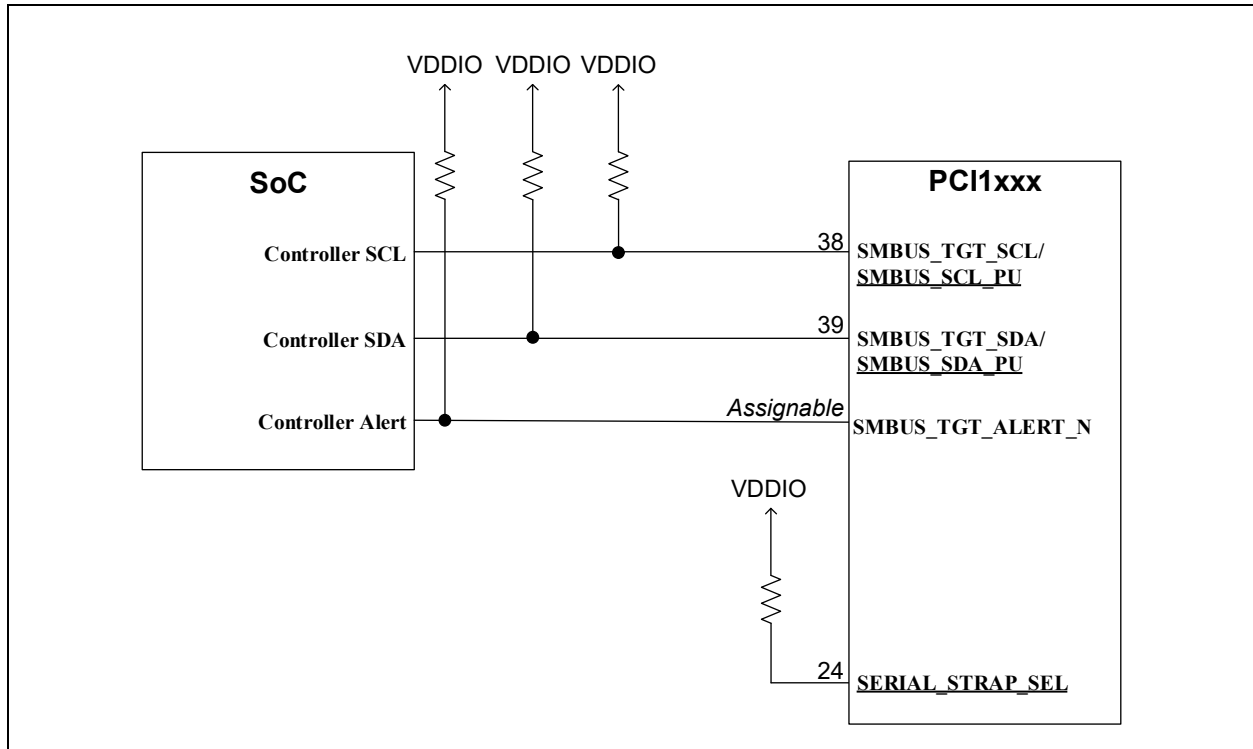
**FIGURE 10-1: EEPROM CONFIGURATION**



### 10.2 I<sup>2</sup>C/SMBus Configuration Interface

- The PCI12000 may be configured via I<sup>2</sup>C/SMBus by an embedded SoC/MCU during both the startup and runtime stages. The proper configuration straps must be detected by the PCI12000 at startup for the I<sup>2</sup>C/SMBus interface to become active. The following strap pins detections are required at startup to enter the I<sup>2</sup>C/SMBus Configuration mode:
    - SERIAL\_STRAP\_EN = 1
    - SMBUS\_SCL\_PU = 1
    - SMBUS\_SDA\_PU = 1
  - The interface command specification and configuration register set is described in full in the *AN4255 PCI12000/PCI11xxx Register Map* application note.
  - Typically, a pull-up resistor of 1 k $\Omega$  to 10 k $\Omega$  is sufficient, depending on the interface speed and total capacitance on I<sup>2</sup>C tree.
  - A pull-up voltage of 1.8V to 3.3V is supported.
  - The target interface supports the Standard mode speed of up to 100 kHz and the Fast mode speed of 400 kHz.
- A typical I<sup>2</sup>C/SMBus target implementation is shown in [Figure 10-2](#).

**FIGURE 10-2: TARGET INTERFACE**



**Note:** If I<sup>2</sup>C/SMBus pull-up resistors are detected by the SMBUS\_SCL\_PU and SMBUS\_SDA\_PU pin straps at startup, the PCI12000 will be indefinitely configured by the attached I<sup>2</sup>C/SMBus controller. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I<sup>2</sup>C/SMBus controller is fully operational and can properly configure the PCI12000 at startup.

The I<sup>2</sup>C/SMBus target clock and data pins, as well as the hardware configuration strap pins SERIAL\_STRAP\_SEL, SMBUS\_SCL\_PU, and SMBUS\_SDA\_PU are all fixed. The I<sup>2</sup>C/SMBus target alert pin is assignment to a number of PROGx pin options. See Table 10-1.

**TABLE 10-1: I<sup>2</sup>C/SMBUS TARGET INTERFACE PINS**

Option	SMBUS_TGT_SCL		SMBUS_TGT_SDA		SMBUS_TGT_ALERT_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG64	38	PROG65	39	PROG32	23
Option 2	—	—	—	—	PROG33	24
Option 3	—	—	—	—	PROG66	40
Option 4	—	—	—	—	PROG67	41
Option 5	—	—	—	—	PROG68	42
Option 6	—	—	—	—	PROG69	47

### 10.3 SPI Peripheral Interface

- The PCI12000 may be configured via SPI interface by an embedded SoC/MCU during both the startup and run-time stages. The proper configuration straps must be detected by the PCI12000 at startup for the I<sup>2</sup>C/SMBus interface to become active.
- The following strap pins detections are required at startup to enter the I<sup>2</sup>C/SMBus Configuration mode:
  - SERIAL\_STRAP\_EN = 1

# PCI12000

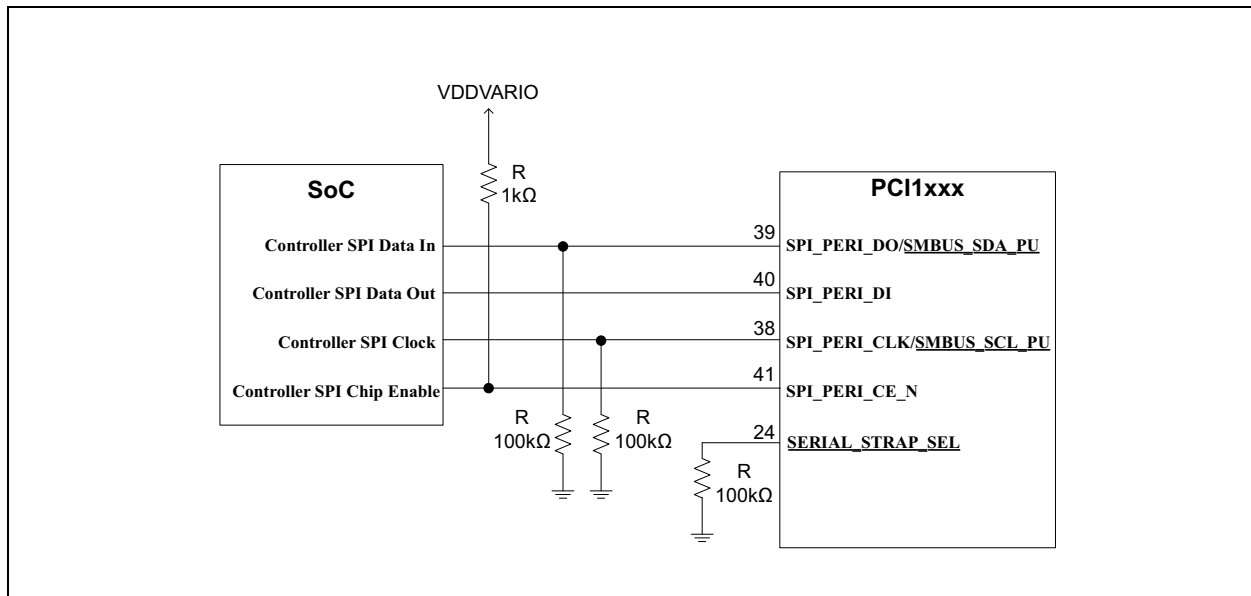
- SMBUS\_SCL\_PU = 0
- SMBUS\_SDA\_PU = 0

**Note:** The SMBUS\_SCL\_PU and SMBUS\_SDA\_PU hardware straps share the same pins as the SPI data out and SPI clock lines. Hence, weak pull-down resistors (i.e.:100 kΩ) are recommended to minimize the effect on SPI communication.

- The interface command specification and configuration register set is described in full in *AN5213 Configuration and Programming Options for the PCI1XXXX*.
- An I/O voltage of 1.8V to 3.3V is supported. I/O voltage is set via the **VDDVARIO** supply power pins.
- The SPI Peripheral interface supports clock rate of up to 30 MHz.

A typical SPI peripheral target implementation is shown in [Figure 10-3](#).

**FIGURE 10-3: SPI PERIPHERAL INTERFACE**



**TABLE 10-2: SPI TARGET INTERFACE PINS**

Option	SPI_PERI_DO		SPI_PERI_DI		SPI_PERI_CLK		SPI_PERI_CE_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG65	39	PROG66	40	PROG64	38	PROG67	41

## 11.0 MISCELLANEOUS

The PCI12000 includes several pins that are in place for manufacturing purposes. These pins are not intended for customer use but must be connected properly for reliable operation of the PCI12000. See [Table 11-1](#) for more details.

**TABLE 11-1: TEST PIN DETAILS**

Pin Name	Required Connections
TESTEN	Default: Pull down to ground with a 100 k $\Omega$ resistor. JTAG enable: Pull up to 3.3V with a 10 k $\Omega$ resistor.

# PCI12000

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NOTES:

## 12.0 HARDWARE CHECKLIST SUMMARY

TABLE 12-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
Section 3.0, "Power and Bypass Capacitance"	Section 3.1, "1.1V Supplies"	Ensure all 1.1V supplies are in the range 1.08V to 1.32V, and they share one 1 $\mu$ F and one 0.1 $\mu$ F bulk capacitor each.		
	Section 3.2, "Variable Voltage"	Ensure VDDVARIO is in the range 1.8V to 3.3V, and they share one 1 $\mu$ F and one 0.1 $\mu$ F bulk capacitor.		
	Section 3.3, "3.3V Supplies"	Ensure VDD33 is in the range 3.0V to 3.6V, and a 0.1 $\mu$ F capacitor is on each pin.		
	Section 3.4, "2.5V Supplies"	Ensure VDD25 is in the range 2.2V to 2.8V, and each pin has a dedicated 1 nF capacitor.		
	Section 3.5, "3.3V References"	Ensure VDD33PVTREF and VDD33WRPLL are within the range of 3.0V to 3.6V with dedicated 1 nF and 0.1 $\mu$ F capacitors on VDD33PVTREF and a dedicated 0.1 $\mu$ F capacitor on VDD33WRPLL.		
Section 4.0, "PCIe Signals"	Section 4.1, "Upstream Port PCIe® Signals"	Verify that the PCIe upstream data pins are correctly routed to the PCIe® connector and the host. Pay special attention to the 0.1 $\mu$ F decoupling capacitor series connecting to the corresponding transmitter and receiver pins.		
	Section 4.2, "Downstream Port PCIe Signals"	Verify that the PCIe downstream data pins of the two ports are correctly routed to the PCIe connector and host as shown in Figure 4-7 and Figure 4-8.		
Section 5.0, "UART"		Verify proper pin configuration. Make sure they are routed correctly to the transceiver. Refer to Figure 5-1.		
Section 6.0, "I <sup>2</sup> C/SPI Controllers"	Section 6.1, "I <sup>2</sup> C/SMBus Controller Interface"	Ensure PROG pins are connected correctly and pulled up to the supported pull-up voltage, 1.8V to 3.3V.		
	Section 6.2, "SPI Controller Interface"	Ensure PROG pins are connected correctly and pulled up to the supported pull-up voltage, 1.8V to 3.3V. Verify that the signal rate is one of the eight supported speeds (Refer to this section for the supported speeds.)		
Section 7.0, "GPIOs"		Verify that any GPIO pins that will be used as GPIOs within the application are connected properly, and never exceed the voltage maximum/minimum values, or overload the current source/sink maximum values as defined in the data sheet.		
Section 8.0, "Clock Circuit"	Section 8.1, "Crystal and External Clock Connection"	Confirm whether the crystal or clock is 25.000 MHz ( $\pm$ 50 ppm).		
		If a single-ended clock is used, ensure it is connected to XTALI while leaving XTALO floating. If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Power and Startup"	Section 9.1, "Board Power Supplies"	Verify that the board power supplies deliver 3V to 3.6V, and 1.08V to 1.32V to the switch power rails, and that the power-on rise time meets the requirement of the switch as defined in the data sheet.		
		If the rise time requirement cannot be met, ensure that the <b>RESET_N</b> line is held low until the power regulators reach a steady state.		
	Section 9.2, "Reset Circuit"	Ensure that the <b>RESET_N</b> signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		
Section 10.0, "Configuration"	Section 10.1, "EEPROM"	Ensure that an approved compatible EEPROM device is used.		
		Verify if the following strap configuration is made at startup to enter Configuration mode: EEPROM_STRAP_EN = 1.		
	Section 10.2, "I <sup>2</sup> C/SMBus Configuration Interface"	Verify if the following strap configuration is made at startup to enter Configuration mode: 1.SERIAL_STRAP_EN = 1 2.SMBUS_SCL_PU = 1 3.SMBUS_SDA_PU = 1		
	Section 10.3, "SPI Peripheral Interface"	Verify if the following strap configuration is made at startup to enter Configuration mode: 1.SERIAL_STRAP_EN = 1 2.SMBUS_SCL_PU = 0 3.SMBUS_SDA_PU = 0		
Section 11.0, "Miscellaneous"		Verify if <b>TESTEN</b> is pulled to <b>GND</b> .		

## APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005168B (01-15-25)	Section 10.1, "EEPROM"	Changed "SERIAL_STRAP_EN" to "EEPROM_STRAP_EN".
	Figure 3-1, Figure 4-6, Figure 4-7, Figure 4-8 and Figure 10-1	Updated pins and drawings.
	Table 5-1 and Table 5-3	Updated pins.
	All	Made minor updates and formatting changes throughout the document.
DS00005168A (12-19-23)	Initial release	

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