VSC8257/VSC8258

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8257 and VSC8258 product families. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8257 or VSC8258 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Thermal Considerations"
- Section 5.0, "Media SerDes Interface"
- Section 6.0, "Host SerDes Interface"
- Section 7.0, "Reference Clocks"
- Section 8.0, "Serial Management Interfaces (SMI)"
- Section 9.0, "Miscellaneous"

Note 1: The VSC8257 and VSC8258 have identical pinouts. The only difference between them is that the VSC8258 supports MACsec, while the VSC8257 does not. In this document VSC825x is used to refer to either device.

2: The VSC825x must be configured after power-up, even for basic bring-up purposes. Use the Microchip supplied API and reference the sample application for examples of API calls.

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC825x implementor should have *one* of the following documents on hand:

- *VSC8257-01 Data Sheet* (www.microchip.com/VSC8257)
- *VSC8258-01 Data Sheet* (www.microchip.com/VSC8258)

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference is used for all ground pins. Use one or more continuous ground planes to ensure a low impedance ground path and a continuous ground reference for all signals. Section 4.0, "Thermal Considerations" explains the importance of grounds for thermal dissipation.

2.4 Pin Types

Table 2-1 lists the pin types used in this document and their definitions.

TABLE 2-1: PIN TYPES AND DESCRIPTIONS

Symbol	Pin Type	Description
A	Analog input/output (I/O)	Analog input for sensing variable voltage levels
I	Input	Input signal
O	Output	Output signal
B	Bidirectional	Bidirectional input or output signal
CML	Current mode logic	—
NC	No Connect	—
LVTTL	Low-voltage transistor-to-transistor logic	—
LVTTLOD	Low-voltage transistor-to-transistor logic with open-drain output	—

3.0 POWER

Table 3-1 shows the power supply pins for VSC825x.

TABLE 3-1: POWER SUPPLY PINS

Name	Pin	Description	Notes
VDDAH	F4	1.0 V power supply for host side analog	Analog, use ferrite bead
VDDAH	G5	1.0 V power supply for host side analog	
VDDAH	H5	1.0 V power supply for host side analog	
VDDAH	J5	1.0 V power supply for host side analog	
VDDAH	K5	1.0 V power supply for host side analog	
VDDAH	L4	1.0 V power supply for host side analog	
VDDAL	F11	1.0 V power supply for line side analog	Analog, use ferrite bead
VDDAL	G10	1.0 V power supply for line side analog	
VDDAL	H10	1.0 V power supply for line side analog	
VDDAL	J10	1.0 V power supply for line side analog	
VDDAL	K10	1.0 V power supply for line side analog	
VDDAL	L11	1.0 V power supply for line side analog	
VDDHSH	G4	1.2 V power supply for host side I/Os	Analog, use ferrite bead
VDDHSH	H4	1.2 V power supply for host side I/Os	
VDDHSH	J4	1.2 V power supply for host side I/Os	
VDDHSH	K4	1.2 V power supply for host side I/Os	
VDDHSL	G11	1.2 V power supply for line side I/Os	Analog, use ferrite bead
VDDHSL	H11	1.2 V power supply for line side I/Os	
VDDHSL	J11	1.2 V power supply for line side I/Os	
VDDHSL	K11	1.2 V power supply for line side I/Os	
VDDL	F8	1.0 V power supply for chip core	Digital, no ferrite bead
VDDL	F10	1.0 V power supply for chip core	
VDDL	L8	1.0 V power supply for chip core	
VDDL	L10	1.0 V power supply for chip core	
VDDLR	G7	1.0 V power supply for chip core	Digital, no ferrite bead
VDDLR	G8	1.0 V power supply for chip core	
VDDLR	H7	1.0 V power supply for chip core	
VDDLR	H8	1.0 V power supply for chip core	
VDDLR	J7	1.0 V power supply for chip core	
VDDLR	J8	1.0 V power supply for chip core	
VDDLR	K7	1.0 V power supply for chip core	
VDDLR	K8	1.0 V power supply for chip core	
VDDMDIO	L5	2.5V power supply for MDIO I/Os	Digital, no ferrite bead
VDDTTL	F7	2.5V power supply for non-MDIO digital I/Os	Digital, no ferrite bead
VDDTTL	L7	2.5V power supply for non-MDIO digital I/Os	

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. See Table 3-2. Note that the 1.0V maximum current values in Table 3-2 include margins, so they total to more than the maximum 1.0V current specification in the data sheet. The data sheet value is correct for overall power.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Power Rail	Voltage	Symbol	Maximum Current
VDDLR	1.0V	IDDLR	4000 mA
VDDL	1.0V	IDDL	1000 mA
VDDAH	1.0V	IDDAH	1500 mA
VDDAL	1.0V	IDDAL	1500 mA
VDDHSH	1.2V	IDDHSH	300 mA
VDDHSL	1.2V	IDDHSL	300 mA
VDDTTL	2.5V	IDDTTL	150 mA

3.2 Power Supply Planes

- The VSC825x requires three power rails: 2.5V, 1.2V, and 1.0V. The filtered analog 1.0V and 1.2V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly-positioned local decoupling. For more information, see Section 3.4, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Analog Power Plane Filtering

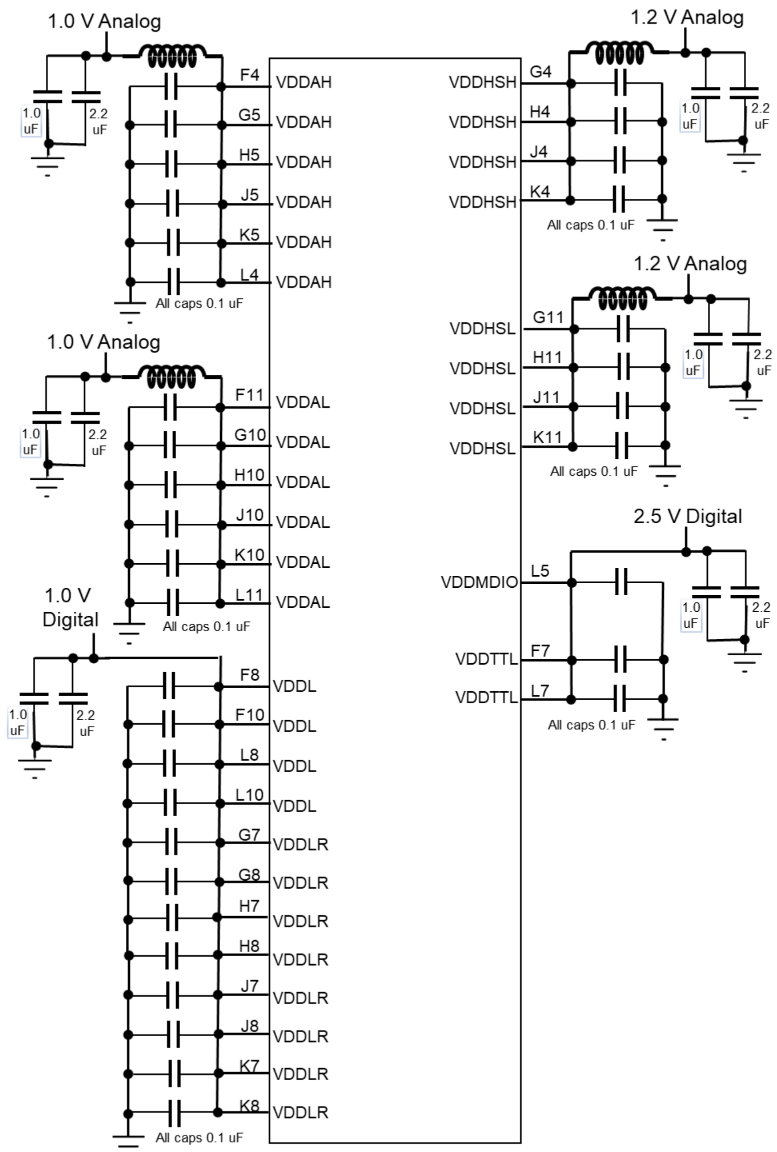
- The analog power supplies are:
  - **VDDAH**
  - **VDDAL**
  - **VDDHSH**
  - **VDDHSL**
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended on digital supplies **VDDL**, **VDDLR**, **VDDTTL**, and **VDDMDIO**.
- The chosen ferrite beads should have impedance of 80Ω to 120Ω at 100 MHz, and the characteristics are specified in Table 3-3.

TABLE 3-3: FERRITE BEAD PARAMETERS

VSC825x Analog Supply	Ferrite Bead Requirements	
	Current	Maximum DC Resistance
VDDAH	1000 mA	40 mΩ
VDDAL	1000 mA	40 mΩ
VDDHSH	150 mA	100 mΩ
VDDHSL	150 mA	100 mΩ

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



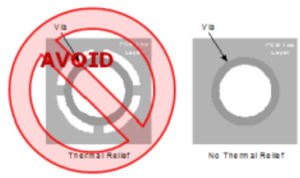
3.4 Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC825x's power pins for every pin.
- If the VSC825x device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 THERMAL CONSIDERATIONS

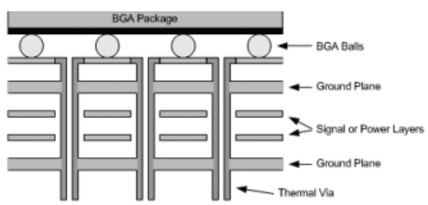
- For proper cooling, ensure efficient thermal dissipation by maximizing the number of via connections to the ground plane. Additional ground planes enhance thermal dissipation and signal integrity performance.
- When connecting the thermal vias to ground planes, it is recommended to avoid thermal relief connection traces as shown on the left side of Figure 4-1 as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have solid connection to the traces and planes on each layer as shown on the right side of Figure 4-1.

FIGURE 4-1: THERMAL VIAS



- PCB thermal vias should connect to the solid ground planes within the board to dissipate heat below the package. A minimum of one-ounce copper cladding is recommended. Figure 4-2 shows a cross-section of the thermal via.

FIGURE 4-2: THERMAL GROUND PLANE CONNECTION



5.0 MEDIA SERDES INTERFACE

5.1 Media SerDes Design Rules

Table 5-1 shows information on the Media SerDes interface. Best performance is achieved when SerDes traces are placed using the following design rules:

- AC coupling capacitors are not needed for SFP+ and SFP applications because SFP+/SFP modules have internal AC coupling capacitors on both TX and RX signals.
- Use AC coupling with 0.1 µF capacitors on RXIN and TXOUT for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing that is equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between SerDes pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If a port is unused, both the **RXIN** and **TXOUT** pins can be left floating (No Connect).

TABLE 5-1: MEDIA SERDES INTERFACE PINS

Pin Name	Pin	Type	Level	Description
RXIN0N	B16	I	CML	Line receive channel 0 input data, complement
RXIN0P	B15	I	CML	Line receive channel 0 input data, true
RXIN1N	F16	I	CML	Line receive channel 1 input data, complement
RXIN1P	F15	I	CML	Line receive channel 1 input data, true
RXIN2N	K16	I	CML	Line receive channel 2 input data, complement
RXIN2P	K15	I	CML	Line receive channel 2 input data, true
RXIN3N	P16	I	CML	Line receive channel 3 input data, complement
RXIN3P	P15	I	CML	Line receive channel 3 input data, true
TXOUT0N	D16	O	CML	Line transmit channel 0 output data, complement
TXOUT0P	D15	O	CML	Line transmit channel 0 output data, true
TXOUT1N	H16	O	CML	Line transmit channel 1 output data, complement
TXOUT1P	H15	O	CML	Line transmit channel 1 output data, true
TXOUT2N	M16	O	CML	Line transmit channel 2 output data, complement
TXOUT2P	M15	O	CML	Line transmit channel 2 output data, true
TXOUT3N	T15	O	CML	Line transmit channel 3 output data, complement
TXOUT3P	T14	O	CML	Line transmit channel 3 output data, true

5.2 Connecting to 10G SFP+ or 1G SFP

Follow the succeeding guidelines for connecting the differential SerDes data pins to the SFP+/SFP (also referred to as SFP):

- Connect the VSC825x **TXOUT** pins directly to the **TD** input pins of the SFP.
- Connect the VSC825x **RXIN** pins directly to the **RD** output pins of the SFP.
- External termination resistors and AC coupling capacitors are not needed on the PCB.

Connection and use of the other SFP signals are at the discretion of the user.

The **RX_LOS** output of the SFP can drive the recommended GPIO input of the VSC825x and/or the host device.

VSC825x **GPIO** pins can be configured as Two-Wire masters for accessing SFP registers via SDA and SCL. However, since this adds an additional layer of software complexity to manage these signals, it is extremely common for the SFP Two-Wire interface to be managed directly from the switch/MAC/ASIC host device. **GPIO** assignments are given in the Table 9-3, below.

VSC825x **GPIO** can also be assigned as inputs for the **MOD_ABS** (module absent) output of the SFP.

All other SFP signals, if used, can be connected to the VSC825x **GPIO**.

All single-ended SFP outputs are open-drain and require a pull-up resistor to 3.3V when used.

All VSC825x **GPIO** outputs are open-drain and require a pull-up resistor. When connected to an SFP, the pull-up voltage must be 3.3V and not 2.5V.

Figure 5-1 and Figure 5-2 illustrate the VSC825x to SFP+ connections. Figure 5-1 shows a typical scenario wherein most SFP signals are connected to the switch/MAC/ASIC host device rather than the VSC825x. Conversely, Figure 5-2 shows a less common scenario wherein the maximum number of SFP signals are connected to the VSC825x.

FIGURE 5-1: SFP+ CONNECTIONS WITH TWO-WIRE AND MOD_ABS TO THE SWITCH/MAC/ ASIC

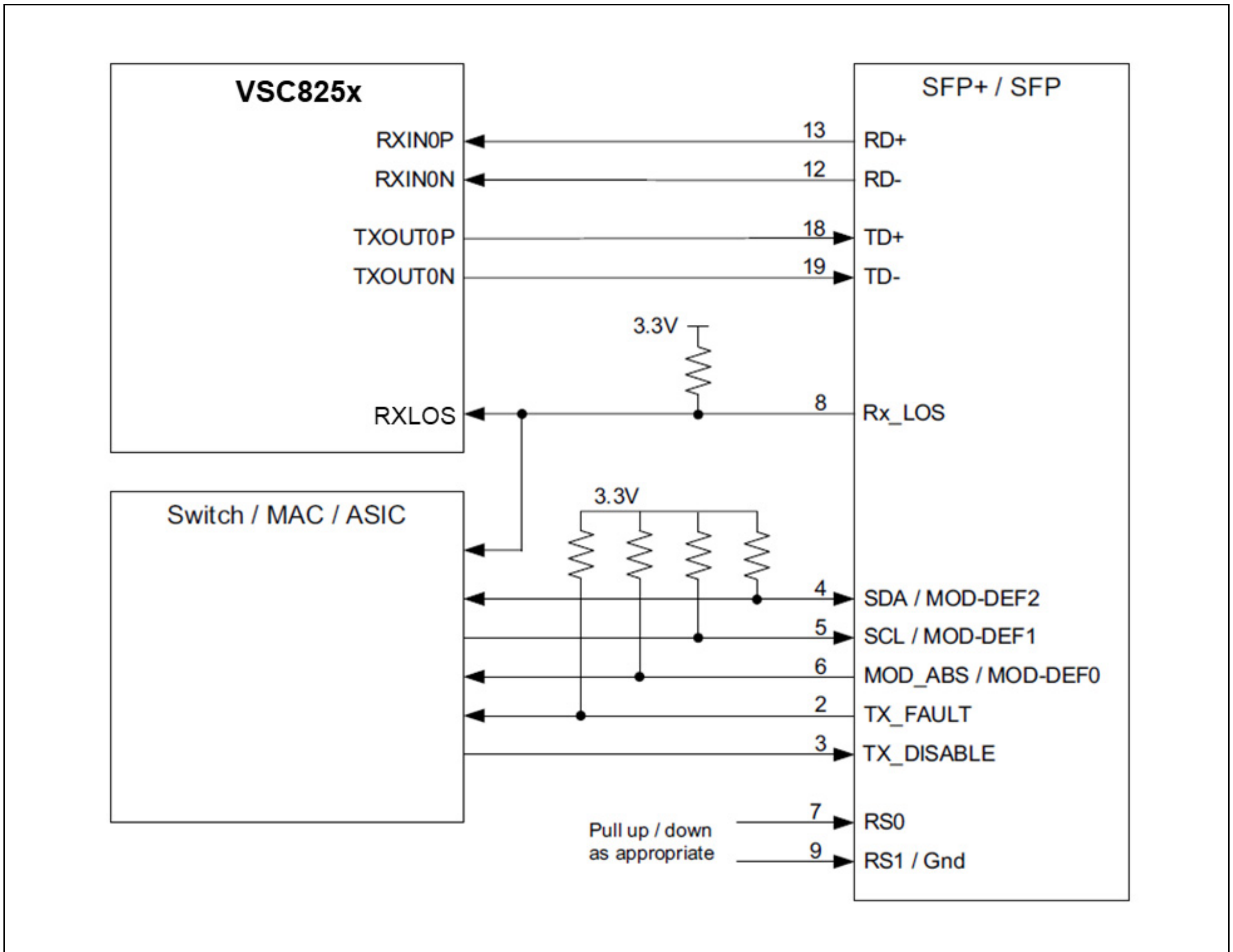
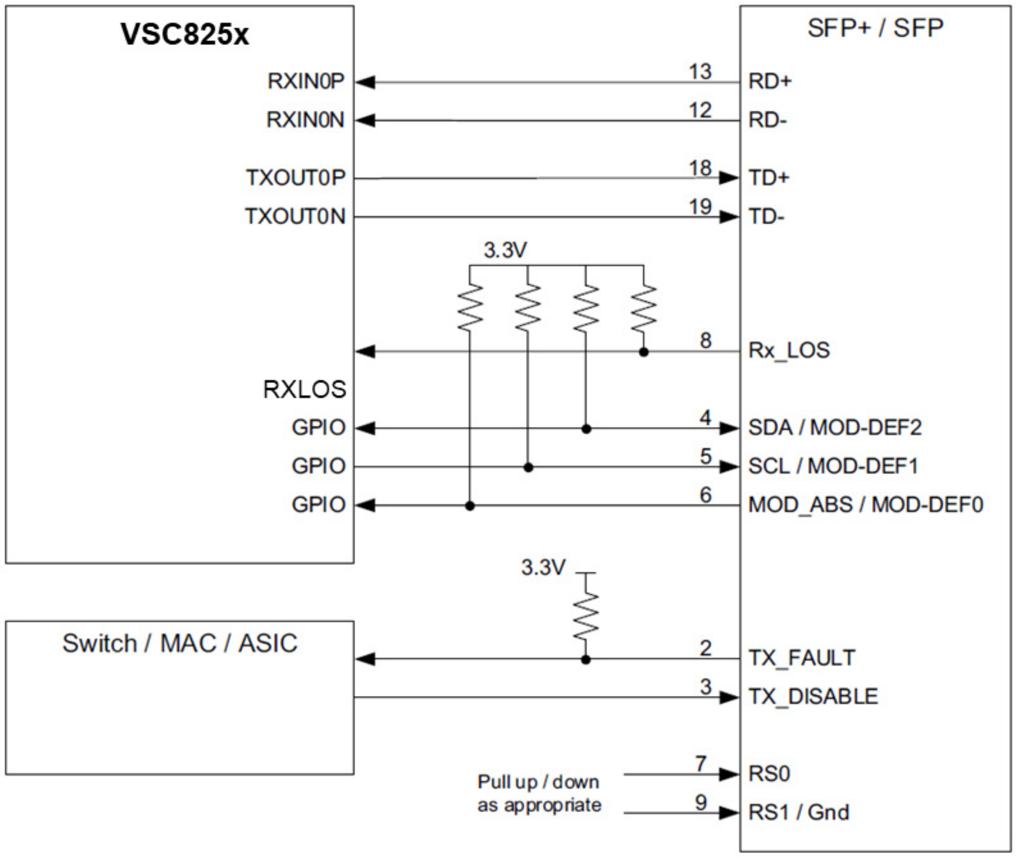


FIGURE 5-2: SFP+ CONNECTIONS WITH TWO-WIRE AND MOD_ABS TO THE VSC825X



6.0 HOST SERDES INTERFACE

Table 6-1 shows information on the Host SerDes interface. Best performance is achieved when SerDes traces are placed using the following design rules:

- Use AC coupling with 0.1 µF capacitors on RXOUT and TXIN for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing that is equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between SerDes pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If a port is unused, both the **RXOUT** and **TXIN** pins can be left floating (No Connect).

TABLE 6-1: HOST SERDES INTERFACE PINS

Pin Name	Pin	Type	Level	Description
RXOUT0N	B1	O	CML	Host receive channel 0 output data, complement
RXOUT0P	B2	O	CML	Host receive channel 0 output data, true
RXOUT1N	F1	O	CML	Host receive channel 1 output data, complement
RXOUT1P	F2	O	CML	Host receive channel 1 output data, true
RXOUT2N	K1	O	CML	Host receive channel 2 output data, complement
RXOUT2P	K2	O	CML	Host receive channel 2 output data, true
RXOUT3N	P1	O	CML	Host receive channel 3 output data, complement
RXOUT3P	P2	O	CML	Host receive channel 3 output data, true
TXIN0N	D1	I	CML	Host transmit channel 0 input data, complement
TXIN0P	D2	I	CML	Host transmit channel 0 input data, true
TXIN1N	H1	I	CML	Host transmit channel 1 input data, complement
TXIN1P	H2	I	CML	Host transmit channel 1 input data, true
TXIN2N	M1	I	CML	Host transmit channel 2 input data, complement
TXIN2P	M2	I	CML	Host transmit channel 2 input data, true
TXIN3N	T2	I	CML	Host transmit channel 3 input data, complement
TXIN3P	T3	I	CML	Host transmit channel 3 input data, true

7.0 REFERENCE CLOCKS

Table 7-1 shows information on reference clocks.

TABLE 7-1: REFERENCE CLOCKS

Pin Name	Pin	Type	Level	Description
HREFCKN	T7	I	CML	Host reference clock input, complement
HREFCKP	R7	I	CML	Host reference clock input, true
LREFCKN	T9	I	CML	Line reference clock input, complement
LREFCKP	R9	I	CML	Line reference clock input, true
SREFCKN	T11	I	CML	SyncE reference clock input, complement
SREFCKP	R11	I	CML	SyncE reference clock input, true

Note 1: HREFCKP/N and LREFCKP/N must be frequency locked together.

7.1 Device Reference Clocks

The VSC825x has three reference clock inputs: **HREFCK**, **LREFCK**, and **SREFCK**.

Synchronous Ethernet (SyncE) applications may use either one or two clocks, while non-SyncE applications use both **LREFCK** and **HREFCK**. Using all three reference clocks is unnecessary.

LREFCK and **HREFCK** are always required and must be synchronous. They may be either 125 MHz or 156.25 MHz. This rate must be selected at power-up using the **MODE[1:0]** pins as shown in Table 7-2.

TABLE 7-2: SELECTING LREFCK FREQUENCY

MODE1 Pin	MODE0 Pin	Frequency
0	0	156.25 MHz (default)
1	0	125 MHz

SREFCK may be used for SyncE applications but is not required. See Section 7.2, "Synchronous Ethernet (SyncE)" for more details.

Users must ensure that the following are executed when using reference clocks:

- The jitter requirements from the data sheet are met.
- The amplitude specifications in the data sheet are met. Note that **HREFCK_P/N** and **LREFCK_P/N** are configurable for either high-swing or low-swing inputs. An API call is used to configure it. **SREFCK_P/N** has a single amplitude range.
- Traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 µF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, make sure that termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC825x side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- Unused reference clocks can be left floating (No Connect).

7.2 Synchronous Ethernet (SyncE)

Hardware and software for VSC825x supports the following recovered clock frequencies:

TABLE 7-3: AVAILABLE RECOVERED CLOCK FREQUENCIES

Mode	Line Frequency (GHz)	CKOUT Frequency (MHz)	SCKOUT Frequency (MHz)	HW Support	SW Support
LAN	10.3125	322.265625 or 161.1328125	156.25 or 125	Divide by 32 or 64	Divide by 64
WAN	9.95328	311.04 or 155.52		Divide by 32 or 64	Divide By 64
1G	1.25	125 or 62.5		Divide by 32 or 64	Divide by 10

Note 1: The hardware provides support for the “Divide-by” values shown. However, the software API has only implemented one of the “Divide-by” values as shown.

2: CKOUT also includes a squelch function that can be used to configure the device to squelch (drive to a constant state) upon detecting certain conditions, such as loss of link on a PCS, or the state of a GPIO input.

In addition to the local reference clock input, LREFCK (which is required in any case), a second, optional reference clock, SREFCK, is available. SREFCK may be used as an alternate synchronization source when LREFCK is a simple local oscillator. SREFCK includes filtering to smooth out changes in frequency (on a clock source switch, for example). LREFCK does not include this capability; if using LREFCK as the clock source in SyncE applications, care must be taken to ensure that switching clock sources is glitch-less.

7.2.1 SYNCE OUTPUT CLOCK

Any recovered clock can be selected for the clock output from a dedicated SyncE output clock, SCKOUT. SCKOUT also includes a synthesizer that can be used to generate a SyncE-friendly clock rate regardless of the line-rate. In 10G LAN applications, for example, it can generate a 156.25 MHz clock derived from the 10.3125 GHz recovered clock. It can also generate a 156.25 MHz clock derived from the 9.95328 GHz recovered clock in a 10G WAN system.

SCKOUT also includes a squelch function that can be used to configure the device to squelch (drive to a constant state) upon detecting certain conditions, such as loss of link on a PCS, or the state of a GPIO input.

The device supports several SyncE configurations. In SyncE applications, typically, a single master clock for all transmit interfaces is selected from multiple potential sources:

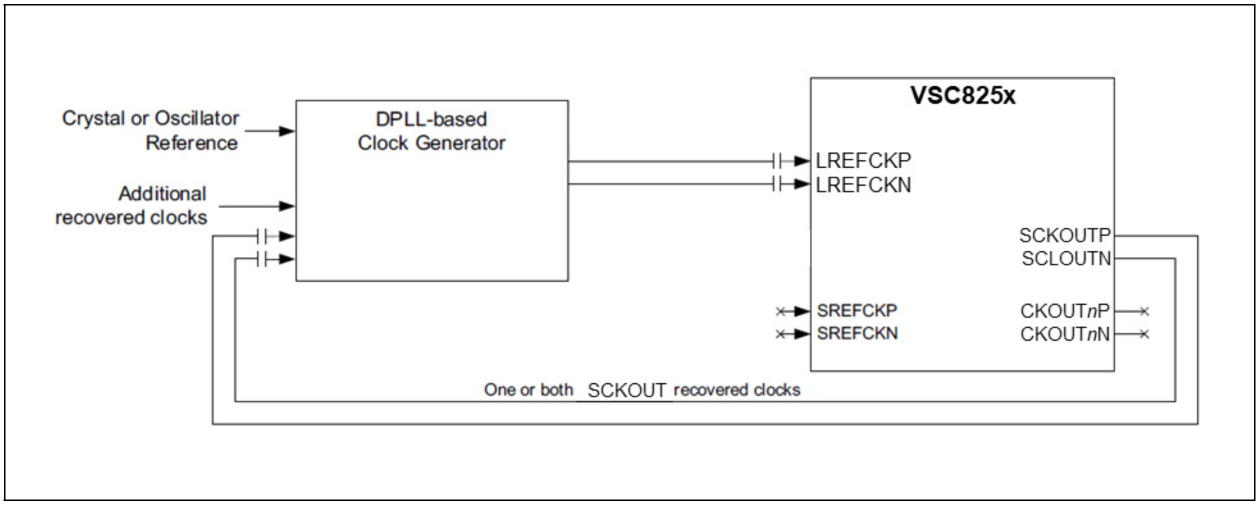
- *Single device, internal master:* The line-side Rx captures the serial data input and generates a clock signal that is then distributed to all ports of the line-side transmitter (Tx), creating a source synchronous function.

  Note: Lane Sync is required in this configuration.

- *Single clock LAN, external master:* The LREFCK frequency is gradually changed to the externally generated SyncE clock frequency using an external clock distribution chip. The change must be hitless to avoid data corruption. The LREFCK source may come from one of the recovered clocks using a CKOUTnP/N or SCKOUTP/N. Figure 7-1 shows a typical configuration.

  Note: Lane Sync is *not* required in this configuration for CKOUT. However, Lane Sync is required if SCKOUT is used.

FIGURE 7-1: TYPICAL SYNCE CLOCK CONFIGURATION



Note: The selectable clock outputs for channels 0-3 (CKOUT*n*P/N, where *n* = 0, 1, 2, 3) can be used instead of SCKOUTP/N when the need for redundant output clocks prevents the use of a single clock output.

- *Dual clock LAN, external master:* The LREFCK remains connected to the stable 156.25 MHz system clock or crystal. All line-side transmits are synchronized to SREFCK. One of the CKOUTnP/N (161.13 MHz) or the SCKOUTP/N (156.25 MHz) provides a recovered clock reference to the external master.

Note: Lane Sync is required in this configuration (all line-side transmits are synchronized to SREFCK). Lane Sync is required if SCKOUT is used.

- *Dual clock WAN, external master:* LREFCK remains connected to the stable 156.25 MHz system clock or crystal. All line side transmits are synchronized to SREFCKP/N (155.52 MHz). SCKOUTP/N provides a recovered clock (156.25 MHz or 155.52 MHz) to be used as a reference to the external master.

Note: Lane Sync is required in this configuration (all line-side transmits are synchronized to SREFCK). Lane Sync is required if SCKOUT is used.

7.3 Output Clocks

In addition to the SCKOUT output, another clock output for each port, **CKOUT[0:3]**, may be connected to any port's transmit clock or recovered clock. When connected to a transmit clock, it may be used to drive clocked optical modules. In SyncE applications, it may be used (in lieu of SCKOUT) to provide a recovered clock to an external timing master. The output clocks of this device are specified in Table 7-4.

TABLE 7-4: OUTPUT CLOCKS

Name	Pin	Type	Level	Description
SCKOUTN	P13	O	CML	SyncE recovered clock output, complement
SCKOUTP	N13	O	CML	SyncE recovered clock output, true
CKOUT0N	B13	O	CML	Selectable clock output channel 0, complement
CKOUT0P	A13	O	CML	Selectable clock output channel 0, true
CKOUT1N	E13	O	CML	Selectable clock output channel 1, complement
CKOUT1P	D13	O	CML	Selectable clock output channel 1, true
CKOUT2N	L13	O	CML	Selectable clock output channel 2, complement
CKOUT2P	K13	O	CML	Selectable clock output channel 2, true
CKOUT3N	H13	O	CML	Selectable clock output channel 3, complement
CKOUT3P	G13	O	CML	Selectable clock output channel 3, true

8.0 SERIAL MANAGEMENT INTERFACES (SMI)

8.1 SPI Management Interface

The VSC825x device supports the serial peripheral interface (SPI) for reading and writing registers for high bandwidth tasks, such as reading the IEEE 1588 time stamp data and performing MACsec key and classification updates for all secure associations (SAs) in a timely manner. The SPI interface is also capable of accessing all status and configuration registers. The SPI client port consists of a clock input (SCK), data input (MOSI), data output (MISO), and slave select input (SSN).

TABLE 8-1: SPI MANAGEMENT PINS

Name	Pin	Type	Level	Description
MISO	B6	O	LVTTL	SPI host data input/client data output
MOSI	B4	I	LVTTL	SPI host data output/client data input, internally pulled low
A6	A6	I	LVTTL	SPI client clock input, internally pulled low
A4	A4	I	LVTTL	SPI client chip select bar input, internally pulled high

The SPI client interface is the recommended interface to access status and configuration registers for the rest of the device.

Drive the SSN pin low to enable the interface. The interface is disabled when SSN is high and MISO is placed into a high impedance state.

8.2 MDIO Management Interface

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The maximum data rate of the MDIO interface is 2.5 Mbps.

TABLE 8-2: MDIO MANAGEMENT PINS

Name	Pin	Type	Level	Description
MDC	T5	I	LVTTL	MDIO clock input
MDIO	R5	B	LVTTLOD	MDIO data I/O
PADDR2	T8	I	LVTTL	Port address bit 2, internally pulled low
PADDR3	R8	I	LVTTL	Port address bit 3, internally pulled low
PADDR4	T6	I	LVTTL	Port address bit 4, internally pulled low

Note 1: A pull-up resistor (~2 kΩ) is required on MDIO. Depending on the master device, a pull-up may also be needed on MDC.

2: The **PADDR[4:2]** pins select the MDIO port addresses to which the VSC825x device will respond. Floating a **PADDR** pin sets the corresponding bit to zero. Pulling it up to 2.5V via a 2-4 kΩ resistor sets the corresponding bit to one.

A single VSC825x device requires the use of four MDIO port addresses, one for each channel. The port address transmitted in MDIO read/write commands to access registers in a particular VSC825x channel is shown in Table 8-3. The port address is a function of the PADDR pins and a preprogrammed number indicating the channel number. Up to eight VSC825x devices can be controlled by a single MDIO host.

Table 8-3 shows the MDIO port address for each channel.

TABLE 8-3: MDIO PORT ADDRESSES PER CHANNEL

Channel Number	Port Address
3	{PADDR[4:2],11}
2	{PADDR[4:2],10}
1	{PADDR[4:2],01}
0	{PADDR[4:2],00}

9.0 MISCELLANEOUS

9.1 IEEE 1588 Signals

TABLE 9-1: IEEE 1588 SIGNALS

Name	Pin	Type	Level	Description
CLK1588N	A11	I	CML	1588 local time counter clock input-complement
CLK1588P	A10	I	CML	1588 local time counter clock input-true
LS	C6	B	LVTTL	1588 load/save input. Internally pulled low.
PPS	C8	B	LVTTL	1588 pulse per second (output)
PPS_RI	C7	I	LVTTL	1588 pulse per second return input signal. Internally pulled low.
SPI_CLK_01	C9	O	LVTTL	Pushout SPI clock output for 1588 timestamp (channel 0 and channel 1)
SPI_CLK_23	P9	O	LVTTL	Pushout SPI clock output for 1588 timestamp (channel 2 and channel 3)
SPI_CS_01	C11	O	LVTTL	Pushout SPI chip select output for 1588 timestamp (channel 0 and channel 1)
SPI_CS_23	P11	O	LVTTL	Pushout SPI chip select output for 1588 timestamp (channel 2 and channel 3)
SPI_DO_01	C10	O	LVTTL	Pushout SPI data output for 1588 timestamp (channel 0 and channel 1)
SPI_DO_23	P10	O	LVTTL	Pushout SPI data output for1588 timestamp (channel 2 and channel 3)

9.1.1 1588 LOGIC CLOCK

The CLK1588_P/N input clock is used in most IEEE 1588 applications to clock the Local Time Counter (LTC). While it is also possible for the LTC to reference a data path clock or the host-side PLL instead of CLK1588_P/N, these options are not typically used.

Design guidelines for CLK1588_P/N are as follows:

- CLK1588_P/N supported frequencies are 125 MHz, 156.25 MHz, 200 MHz, and 250 MHz.
- For 1588 boundary clock applications, CLK1588 is typically supplied by a PLL-based reference.
- For 1588 transparent clock applications, CLK1588 should be sourced from a frequency locked clock that is common to all other timestamping interfaces.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Use AC coupling with 0.1 µF capacitors. Capacitors are best located close to the destination.
- The clock inputs are internally terminated, so external resistors are not needed.
- If CLK1588_P/N are unused, they can be left floating (No Connect).

9.1.2 PUSH OUT SPI HOST INTERFACE

Serial time stamps can be pushed out on the **SPI_CLK**, **SPI_CS**, and **SPI_DO** output pins. This interface is more often used in two-step 1588 mode because of the higher rate of timestamps needing to be processed by the external processor or FPGA. For applications such as one-step transparent clock, it is typically not used. If unused, these pins can be left floating (No Connect). The signals are 2.5V LVTTL.

9.2 GPIO Pins

The VSC825x has 39 GPIO pins that may be used for general purpose I/O or for dedicated functions. Refer to Table 9-2. The recommended use of GPIO pins is shown in Table 9-3.

When used as outputs, these pins are open-drain and require a 2 kΩ-to-10 kΩ pull-up. Any unused GPIO pins can be left floating (No Connect).

TABLE 9-2: GPIO PINS

Name	Pin	Type	Level	Description
GPIO_0	D4	B	LVTTLOD	General purpose I/O 0
GPIO_1	D5	B	LVTTLOD	General purpose I/O 1
GPIO_2	D6	B	LVTTLOD	General purpose I/O 2
GPIO_3	D7	B	LVTTLOD	General purpose I/O 3
GPIO_4	B8	B	LVTTLOD	General purpose I/O 4
GPIO_5	B9	B	LVTTLOD	General purpose I/O 5
GPIO_6	D8	B	LVTTLOD	General purpose I/O 6
GPIO_7	D9	B	LVTTLOD	General purpose I/O 7
GPIO_8	D10	B	LVTTLOD	General purpose I/O 8
GPIO_9	D11	B	LVTTLOD	General purpose I/O 9
GPIO_10	D12	B	LVTTLOD	General purpose I/O 10
GPIO_11	E4	B	LVTTLOD	General purpose I/O 11
GPIO_12	E5	B	LVTTLOD	General purpose I/O 12
GPIO_13	E6	B	LVTTLOD	General purpose I/O 13
GPIO_14	E7	B	LVTTLOD	General purpose I/O 14
GPIO_15	E8	B	LVTTLOD	General purpose I/O 15
GPIO_16	E9	B	LVTTLOD	General purpose I/O 16
GPIO_17	E10	B	LVTTLOD	General purpose I/O 17
GPIO_18	E11	B	LVTTLOD	General purpose I/O 18
GPIO_19	E12	B	LVTTLOD	General purpose I/O 19
GPIO_20	M4	B	LVTTLOD	General purpose I/O 20
GPIO_21	M5	B	LVTTLOD	General purpose I/O 21
GPIO_22	M6	B	LVTTLOD	General purpose I/O 22
GPIO_23	M7	B	LVTTLOD	General purpose I/O 23
GPIO_24	M8	B	LVTTLOD	General purpose I/O 24
GPIO_25	M9	B	LVTTLOD	General purpose I/O 25
GPIO_26	M10	B	LVTTLOD	General purpose I/O 26
GPIO_27	M11	B	LVTTLOD	General purpose I/O 27
GPIO_28	N4	B	LVTTLOD	General purpose I/O 28
GPIO_29	N5	B	LVTTLOD	General purpose I/O 29
GPIO_30	N6	B	LVTTLOD	General purpose I/O 30
GPIO_31	N7	B	LVTTLOD	General purpose I/O 31
GPIO_32/I2C_SDA	N8	B	LVTTLOD	General purpose I/O 32 (also I^2C data)
GPIO_33/I2C_SCL	N9	B	LVTTLOD	General purpose I/O 33 (also I^2C clock)
GPIO_34	N10	B	LVTTLOD	General purpose I/O 34
GPIO_35	N11	B	LVTTLOD	General purpose I/O 35
GPIO_36	P5	B	LVTTLOD	General purpose I/O 36
GPIO_37	P6	B	LVTTLOD	General purpose I/O 37
GPIO_38	P7	B	LVTTLOD	General purpose I/O 38
GPIO_39	P8	B	LVTTLOD	General purpose I/O 39

The recommended GPIO pin assignments are shown in Table 9-3. Contact Microchip applications support for recommendations on alternative GPIO configurations.

TABLE 9-3: RECOMMENDED GPIO CONFIGURATIONS

Channel	GPIO	Pin	Configuration
0	GPIO_0	D4	CH0_RATESEL0
	GPIO_1	D5	CH0_MOD_ABS
	GPIO_2	D6	CH0_I2C_MST_SCL
	GPIO_3	D7	CH0_I2C_MST_SDA
	GPIO_4	B8	CH0_TX_DIS
	GPIO_5	B9	CH0_TX_FAULT
	GPIO_6	D8	CH0_RXLOS (See Note 1)
	GPIO_7	D9	CH0_LINK_UP
1	GPIO_8	D10	CH1_RATESEL0
	GPIO_9	D11	CH1_MOD_ABS
	GPIO_10	D12	CH1_I2C_MST_SCL
	GPIO_11	E4	CH1_I2C_MST_SDA
	GPIO_12	E5	CH1_TX_DIS
	GPIO_13	E6	CH1_TX_FAULT
	GPIO_14	E7	CH1_RXLOS
	GPIO_15	E8	CH1_LINK_UP
2	GPIO_16	E9	CH2_RATESEL0
	GPIO_17	E10	CH2_MOD_ABS
	GPIO_18	E11	CH2_I2C_MST_SCL
	GPIO_19	E12	CH2_I2C_MST_SDA
	GPIO_20	M4	CH2_TX_DIS
	GPIO_21	M5	CH2_TX_FAULT
	GPIO_22	M6	CH2_RXLOS
	GPIO_23	M7	CH2_LINK_UP
3	GPIO_24	M8	CH3_RATESEL0
	GPIO_25	M9	CH3_MOD_ABS
	GPIO_26	M10	CH3_I2C_MST_SCL
	GPIO_27	M11	CH3_I2C_MST_SDA
	GPIO_28	N4	CH3_TX_DIS
	GPIO_29	N5	CH3_TX_FAULT
	GPIO_30	N6	CH3_RXLOS
	GPIO_31	N7	CH3_LINK_UP
N/A	GPIO_32/I2C_SDA	N8	I2C_SLAVE_SDA
	GPIO_33/I2C_SCL	N9	I2C_SLAVE_SCL
	GPIO_34	N10	INTR_A
	GPIO_35	N11	INTR_B
0	GPIO_36	P5	CH0_ACTIVITY
1	GPIO_37	P6	CH1_ACTIVITY
2	GPIO_38	P7	CH2_ACTIVITY
3	GPIO_39	P8	CH3_ACTIVITY

Note 1: Optional wire-or between RXLOS and LINK_UP.

9.3 Reset

The VSC825x must be reset at power-up. One option is to hold **RESETN** low for a minimum 1 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **RESETN** low for a minimum 1 ms after power up. **RESETN** is typically driven by a voltage monitor device or by the management processor or FPGA.

TABLE 9-4: RESET PIN

Pin Name	Pin	Type	Level	Description
RESETN	A9	I	LVTTL	Reset Bar. (Low = Reset) Internally pulled high. Ground to reset.

9.4 JTAG

If JTAG is not used, TRSTB should be pulled low via a 1 kΩ resistor and all the other pins can be left floating.

TABLE 9-5: JTAG PINS

Name	Pin	Type	Level	Description
TCK	B7	I	LVTTL	Boundary scan, test clock input. Internally pulled high.
TDI	A8	I	LVTTL	Boundary scan, test data input. Internally pulled high.
TDO	A7	O	LVTTL	Boundary scan, test data output.
TMS	B5	I	LVTTL	Boundary scan, test mode select. Internally pulled high.
TRSTB	A5	I	LVTTL	Boundary scan, test reset bar input. Internally pulled high.

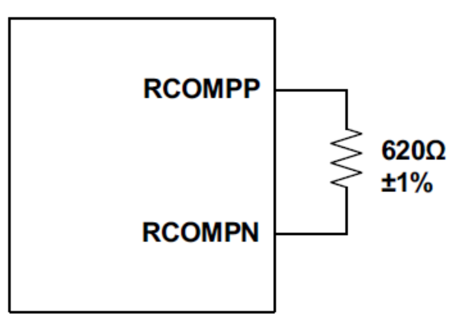
9.5 Reference Resistor

Connect a 620Ω ±1% resistor between **RCOMPN** and **RCOMPP** as shown in Figure 9-1. Refer to Table 9-6 for additional details on the pins.

TABLE 9-6: REFERENCE RESISTORS

Name	Pin	Type	Level	Description
RCOMPN	R12	—	Analog	Resistor comparator, complement
RCOMPP	T12	—	Analog	Resistor comparator, true

FIGURE 9-1: RCOMP RESISTOR

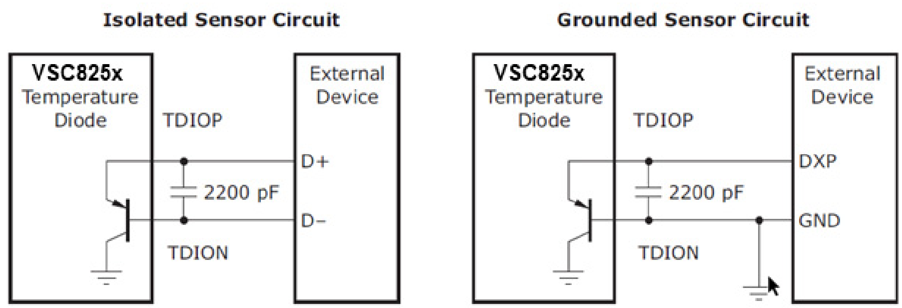


9.6 Temperature Sensor Diode

TABLE 9-7: TEMPERATURE SENSOR PINS

Name	Pin	Type	Level	Description
TDION	C4	—	Analog	Temperature diode, complement
TDIOP	C5	—	Analog	Temperature diode, true

FIGURE 9-2: THERMAL DIODE CONNECTIONS



9.7 Unused Pins

TABLE 9-8: UNUSED PIN

Name	Pin	Type	Level	Description
NC	A12	—	—	Reserved, No Connect
NC	B12	—	—	Reserved, No Connect
NC	C12	—	—	Reserved, No Connect
NC	M12	—	—	Reserved, No Connect
NC	N12	—	—	Reserved, No Connect
NC	P4	—	—	Reserved, No Connect
NC	P12	—	—	Reserved, No Connect
NC	T10	—	—	Reserved, No Connect

NOTES:

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	Design pins match the data sheet.		
	Section 2.3, "Ground"	All ground pins connect to a single ground. Solid ground planes should be used.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Ensure that the power rails can supply adequate current.		
	Section 3.2, "Power Supply Planes"	Make sure that the analog planes are filtered with ferrite beads, while digital planes are not. Consider possible resistive voltage drop in distribution.		
	Section 3.3, "Analog Power Plane Filtering"	Make sure that the analog planes are filtered with ferrite beads, while digital planes are not. Consider possible resistive voltage drop in distribution.		
	Section 3.4, "Decoupling Capacitors"	Ensure that there is one decoupling capacitor near each power pin and at least a 10 µF bulk capacitor per rail. See Figure 3-1.		
Section 4.0, "Thermal Considerations"	Section 4.0, "Thermal Considerations"	Use dedicated thermal vias. Do not use ground vias for thermal relief.		
Section 5.0, "Media SerDes Interface"	Section 5.1, "Media SerDes Design Rules"	Unless common mode voltages are compatible, make sure to use AC coupling capacitors for non-SFP applications. SFP modules include AC coupling. Follow good differential signal layout practices.		
	Section 5.2, "Connecting to 10G SFP+ or 1G SFP"	Take note that AC coupling capacitors are not needed. Connect TXOUT to TD of SFP and RXIN to RD. SFP single-ended outputs need pull-ups. Consider connecting the SFP Two-Wire and other controls to a host rather than the VSC825x. Other SFP status and control may also connect to the host.		
Section 6.0, "Host SerDes Interface"	Section 6.0, "Host SerDes Interface"	Unless Common-mode voltage levels are compatible, use AC coupling. Follow good differential signal layout practices.		
Section 7.0, "Reference Clocks"	Section 7.1, "Device Reference Clocks"	LREFCK and HREFCK are always required. They must be synchronous. Table 7-1 shows the available choices for LREFCK/HREFCK frequencies. Ensure that the jitter and amplitude requirements listed in the data sheet are met.		
	Section 7.2, "Synchronous Ethernet (SyncE)"	If using LREFCK as the clock source in SyncE applications, care must be taken to ensure that switching clock sources is glitch-less. (This is not an issue with SREFCK since it includes filtering to smooth out changes in frequency.)		
	Section 7.3, "Output Clocks"	The external receiver of the recovered clock for SyncE must be configured for an available frequency, as shown in Table 7-2.		
Section 8.0, "Serial Management Interfaces (SMI)"	Section 8.0, "Serial Management Interfaces (SMI)"	Only one of the management interface options (SPI or MDIO) can be used at a time. SPI is strongly recommended over MDIO. MDIO is only suitable if MACSec (for VSC825x) and two-step 1588 are not used.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Miscellaneous"	Section 9.1, "IEEE 1588 Signals"	Make sure to supply a quality clock for CLK 1588 input clock. The push-out SPI interface is only for outputting timestamps to the host processor.		
	Section 9.2, "GPIO Pins"	All GPIO pins are LVTTLOD and require external pull-ups when used as outputs.		
	Section 9.3, "Reset"	Ensure that there is a rising edge on RESETN following power rails and clock being up.		
	Section 9.4, "JTAG"	If JTAG is unused, TRSTB should be pulled low and the other JTAG pins can be left unconnected.		
	Section 9.5, "Reference Resistor"	Make sure to connect a 620Ω ±1% resistor between RCOMPN and RCOMPP.		
	Section 9.6, "Temperature Sensor Diode"	If used, connect to an external temperature sensor device such as the MCP9902, with TDIOP connected to the positive node and TDION to the negative node.		
	Section 9.7, "Unused Pins"	Verify that all "Reserved, No Connect" pins are left unconnected.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004841A (12-14-22)	Initial release	

NOTES:

NOTES:

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