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DOCUMENT DESCRIPTION

Schematic Checklist for the LAN8810, 72-pin QFN Package

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Schematic Checklist for LAN8810

Information Particular for the 72-pin QFN Package

LAN8810 QFN Phy Interface:

1. TR0P (pin 58); This pin is the transmit/receive positive channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

2. TR0N (pin 57); This pin is the transmit/receive negative channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

3. TR1P (pin 61); This pin is the transmit/receive positive channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

4. TR1N (pin 60); This pin is the transmit/receive negative channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

5. TR2P (pin 66); This pin is the transmit/receive positive channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

6. TR2N (pin 65); This pin is the transmit/receive negative channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

7. TR3P (pin 69); This pin is the transmit/receive positive channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

8. TR3N (pin 68); This pin is the transmit/receive negative channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor can be biased to a +2.5V through +3.3V supply. This pin also connects to the 10/100/1000 magnetics.

9. For Transmit/Receive Channel connections and termination details, refer to Figure 1.

10. **Note:** The bias voltage for the (8) 49.9 Ω terminations and the magnetic center taps must not exceed the VDDVARIO voltage level.

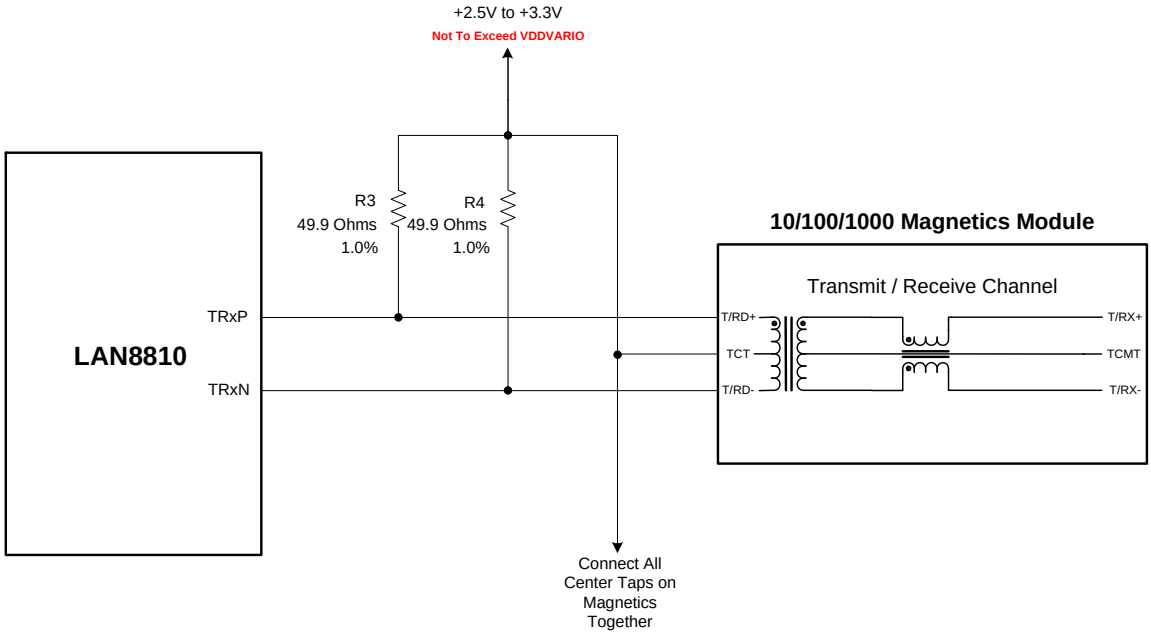


Figure 1 – Transmit / Receive Channel x Connections and Terminations

LAN8810 QFN Magnetics:

1. The center tap connection on the LAN8810 side for each channel must be connected to the same power supply as the bias supply for the Ethernet terminations.

2. The center tap connection on the cable side (RJ45 side) for each channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

3. Assuming the design of an end-point device (NIC), TR0P (pin 58) of the LAN8810 QFN should trace through the magnetics to pin 1 of the RJ45 connector.

4. Assuming the design of an end-point device (NIC), TR0N (pin 57) of the LAN8810 QFN should trace through the magnetics to pin 2 of the RJ45 connector.

5. Assuming the design of an end-point device (NIC), TR1P (pin 61) of the LAN8810 QFN should trace through the magnetics to pin 3 of the RJ45 connector.

6. Assuming the design of an end-point device (NIC), TR1N (pin 60) of the LAN8810 QFN should trace through the magnetics to pin 6 of the RJ45 connector.

7. Assuming the design of an end-point device (NIC), TR2P (pin 66) of the LAN8810 QFN should trace through the magnetics to pin 4 of the RJ45 connector.

8. Assuming the design of an end-point device (NIC), TR2N (pin 65) of the LAN8810 QFN should trace through the magnetics to pin 5 of the RJ45 connector.

9. Assuming the design of an end-point device (NIC), TR3P (pin 69) of the LAN8810 QFN should trace through the magnetics to pin 7 of the RJ45 connector.

10. Assuming the design of an end-point device (NIC), TR3N (pin 68) of the LAN8810 QFN should trace through the magnetics to pin 8 of the RJ45 connector.

RJ45 Connector:

1. The RJ45 shield should be attached directly to chassis ground.

VDDVARIO Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN8810. All power pins on the LAN8810 must be supplied by external power supplies.

2. The power drawn by the VDDVARIO pins, the Ethernet terminations and the 10/100/1000 magnetics is approximately 238 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

3. The VDDVARIO supply pins on the LAN8810 QFN are 6, 14, 23, 32, 41 & 49. These pins require a connection to +3.3V - +2.5V.

4. Each VDDVARIO pin should also have one .01 μF (or smaller) capacitor to decouple the LAN8810. The capacitor size should be SMD_0603 or smaller.

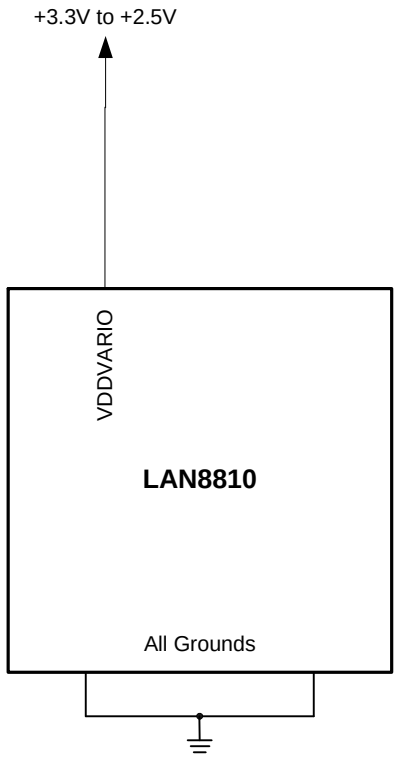


Figure 2 - VDDVARIO Power Supply Connections

+1.2V Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN8810. All power pins on the LAN8810 must be supplied by external power supplies.

2. The power drawn by the VDD12CORE pins, the VDD12A pins, the VDD12BIAS pin, and the VDD12PLL pin is approximately 454 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

3. VDD12CORE (pins 7, 15, 24, 31, 40 & 48), these six pins must be connected to an external +1.2V supply and provide power to the +1.2V core of the LAN8810.

4. The VDD12CORE pins should each have one .01 μF (or smaller) capacitor to decouple the LAN8810. The capacitor size should be SMD_0603 or smaller.

5. VDD12A (pins 59, 62, 67 & 70), these four pins supply power to the analog block of the LAN8810. These pins must be connected to an external +1.2V supply through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. The VDD12A pins should each have one .01 μF (or smaller) capacitor to decouple the LAN8810. The capacitor size should be SMD_0603 or smaller.

7. VDD12BIAS (pin 63), this pin must be connected to an external +1.2V supply directly (no ferrite bead required).

8. The VDD12BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN8810. The capacitor size should be SMD_0603 or smaller.

9. VDD12PLL (pin 64), this pin supplies power for the Ethernet PLL. This pin must be connected to an external +1.2V power supply through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

10. The VDD12PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN8810. The capacitor size should be SMD_0603 or smaller.

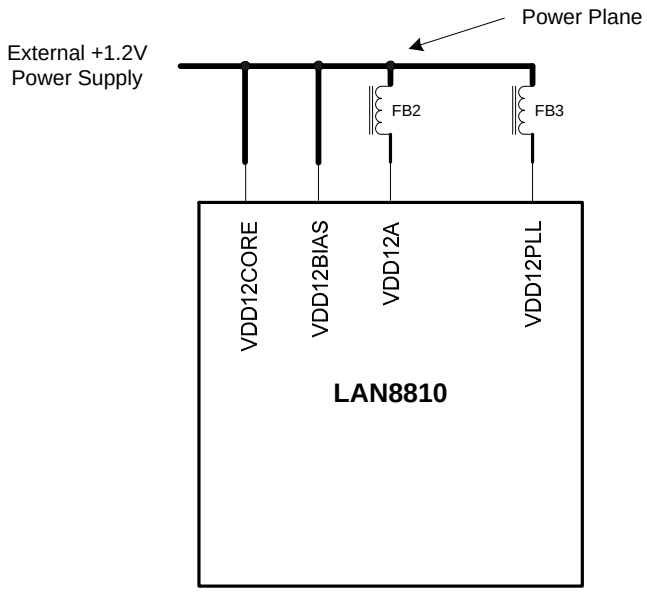


Figure 3 - LAN8810 +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN8810 QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN8810 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN8810 QFN. For exact specifications and tolerances refer to the latest revision LAN8810 data sheet.

2. XI (pin 4) on the LAN8810 QFN is the clock circuit input. This pin requires a 27 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 5) on the LAN8810 QFN is the clock circuit output. This pin requires a matching 27 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN8810 QFN.

ETHRBIAS Resistor:

1. ETHRBIAS (pin 54) on the LAN8810 QFN should connect to digital ground through a 8.06K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 71) requires an external pull-up resistor to VDDVARIO as this output is an Open Drain type.

2. When using the MII or the GMII interface of the LAN8810 with a MAC device on board, a pull-up resistor on the MDIO signal (pin 53) is required. A pull-up resistor of 1.5KΩ to VDDVARIO is required for this application

GMII Interface:

1. The following table indicates the proper connections for the 27 GMII signals.

From:	Connects To:	
LAN8810 QFN	**GMII MAC Device**	**Notes**
RXD0 (pin 8)	RXD<0>	
RXD1 (pin 9)	RXD<1>	
RXD2 (pin 10)	RXD<2>	
RXD3 (pin 11)	RXD<3>	
RXD4 (pin 12)	RXD<4>	
RXD5 (pin 13)	RXD<5>	
RXD6 (pin 16)	RXD<6>	
RXD7 (pin 17)	RXD<7>	
RX_DV (pin 18)	RX_DV	
RX_ER (pin 19)	RX_ER	
RX_CLK (pin 22)	RX_CLK	Used For MII & GMII Modes
TX_ER (pin 37)	TX_ER	
TXD0 (pin 35)	TXD<0>	
TXD1 (pin 34)	TXD<1>	
TXD2 (pin 33)	TXD<2>	
TXD3 (pin 30)	TXD<3>	
TXD4 (pin 29)	TXD<4>	
TXD5 (pin 28)	TXD<5>	
TXD6 (pin 27)	TXD<6>	
TXD7 (pin 26)	TXD<7>	
TX_EN (pin 36)	TX_EN	
TX_CLK (pin 38)	TX_CLK	MII Mode Only
GTXCLK (pin 39)	GTX_CLK	GMII Mode Only (Input From MAC)
CRS (pin 20)	CRS	
COL (pin 21)	COL	
MDIO (pin 53)	MDIO	
MDC (pin 52)	MDC	

2. Provisions should be made for series terminations for all outputs on the MII/GMII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8810 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω.

CONFIG[3..0] Pins:

1. CONFIG0 (pin 51) This pin sets the PHYADD[1:0] bits of the 10/100 Special Modes Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

2. CONFIG1 (pin 50) This pin sets the PAUSE bit of the Auto Negotiation Advertisement Register and PHYADD [2] bit of the 10/100 Special Modes Register on reset or power up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

3. CONFIG2 (pin 47) This pin sets the MOD[1:0] bits of the Extended Mode Control/Status Register on reset or power up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

4. CONFIG3 (pin 46) This pin sets the CLK125DIS bit and MOD[3] bit of the Extended Mode Control/Status Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

LED pins:

1. 10_LED (pin 45) This LED pin indicates the 10BASE-T Link status of the Phy.

2. 100_LED (pin 44) This LED pin indicates the 100BASE-TX Link status of the Phy.

3. 1000_LED (pin 43) This LED pin indicates the 1000BASE-T Link status of the Phy.

4. ACT_LED (pin 42) This LED pin indicates the Activity status of the Phy.

Dedicated Configuration Strap Pins:

1. HPD_MODE (pin 44), this configuration strap is used to select the Hardware Power Down (HPD) mode. When pulled-up, the PLL is not disabled when HPD is asserted. When pulled-down, the PLL is disabled when HPD is asserted. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDDVARIO.

2. REFCLK_SEL (pin 45), this configuration strap is used to select the XI pin's reference clock frequency input. When pulled-up, a 125MHz reference clock is selected. When pulled-down, a 25MHz reference clock is selected. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDDVARIO.

Miscellaneous:

1. There is one No-Connect pin on the LAN8810. It is very important that this pin remains as a no-connect. This is pin 25 on the device.

2. nRESET (pin 55), this pin is an active-low reset input. This signal resets all logic and registers within the LAN8810. This signal is pulled high with a weak internal pull-up resistor. The nRESET should not be left unconnected as the +3.3V internal power-on reset circuitry is RC based. SMSC strongly recommends the use of an external POR for the nRESET pin.

3. HPD (pin 56), this pin places the device into Hardware Power Down (HPD) mode. Refer to the latest revision of the data sheet, Section 3.7.3, "Hardware Power-Down," for additional information. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDDVARIO.

4. The LAN8810 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN8810 data sheet.

5. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

6. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

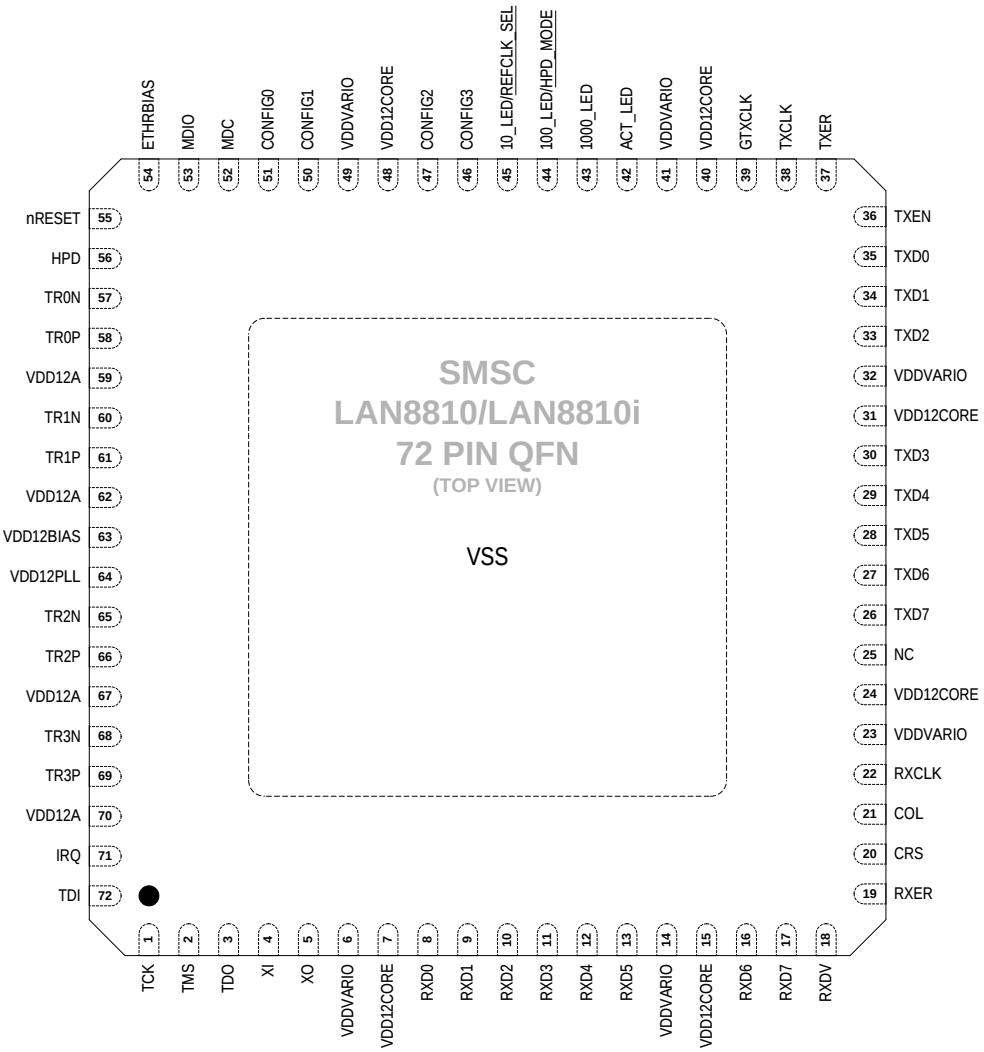
LAN8810 QFN QuickCheck Pinout Table:

Use the following table to check the LAN8810 QFN shape in your schematic.

LAN8810 QFN			
Pin No.	Pin Name	Pin No.	Pin Name
1	TCK	37	TXER
2	TMS	38	TXCLK
3	TDO	39	GTXCLK
4	XI	40	VDD12CORE
5	XO	41	VDDVARIO
6	VDDVARIO	42	ACT_LED
7	VDD12CORE	43	1000_LED
8	RXD0	44	100_LED / HPD_MODE
9	RXD1	45	10_LED / REFCLK_SEL
10	RXD2	46	CONFIG3
11	RXD3	47	CONFIG2
12	RXD4	48	VDD12CORE
13	RXD5	49	VDDVARIO
14	VDDVARIO	50	CONFIG1
15	VDD12CORE	51	CONFIG0
16	RXD6	52	MDC
17	RXD7	53	MDIO
18	RXDV	54	ETHRBIAS
19	RXER	55	nRESET
20	CRS	56	HPD
21	COL	57	TR0N
22	RXCLK	58	TR0P
23	VDDVARIO	59	VDD12A
24	VDD12CORE	60	TR1N
25	NC1	61	TR1P
26	TXD7	62	VDD12A
27	TXD6	63	VDD12BIAS
28	TXD5	64	VDD12PLL
29	TXD4	65	TR2N
30	TXD3	66	TR2P
31	VDD12CORE	67	VDD12A
32	VDDVARIO	68	TR3N
33	TXD2	69	TR3P
34	TXD1	70	VDD12A
35	TXD0	71	IRQ
36	TXEN	72	TDI
73		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN8810 QFN Package Drawing:



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Reference Material:

1. SMSC LAN8810 Data Sheet; check web site for latest revision.
2. SMSC LAN8810 Reference Design, check web site for latest revision.
3. SMSC Reference Designs are schematics only; there are no associated PCBs.
4. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smsc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smsc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm