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DOCUMENT DESCRIPTION
Routing Checklist for the LAN9252, 64-pin SQFN Package

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Routing Checklist for LAN9252

Information Particular for the 64-pin QFN Package

LAN9252 SQFN Port A Copper Twisted Pair Phy Interface:

1. The traces connecting the transmit outputs (TXPA, pin 53) & (TXNA, pin 52) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
2. The traces connecting the receive inputs (RXPA, pin 55) & (RXNA, pin 54) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
3. For differential traces running from the LAN controller to the magnetics, Microchip recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. The VDD33TXRX1 power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

LAN9252 SQFN Port B Copper Twisted Pair Phy Interface:

1. The traces connecting the transmit outputs (TXPB, pin 62) & (TXNB, pin 63) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
2. The traces connecting the receive inputs (RXPB, pin 60) & (RXNB, pin 61) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
3. For differential traces running from the LAN controller to the magnetics, Microchip recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. The VDD33TXRX2 power supply should be routed as a mini-plane and can be routed on an internal power plane layer.



LAN9252 QFN Ports A & B Copper Twisted Pairs Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
3. For differential traces running from the magnetics to the RJ45 connector, Microchip recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

Copper Twisted Pair RJ45 Connector Ports A & B:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.
2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.



LAN9252 SQFN Port A Fiber Phy (100BASE-FX) Interface:

1. The traces connecting the transmit outputs (TXPA, pin 53) & (TXNA, pin 52) to the fiber module must be run as differential pairs. 50 ohm microstrip signal paths are recommended.
2. The traces connecting the receive inputs (RXPA, pin 55) & (RXNA, pin 54) from the fiber module must be run as differential pairs. 50 ohm microstrip signal paths are recommended.
3. For differential traces running from the LAN controller to the fiber module, Microchip recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. The +5V power supply for the fiber module should be routed as a mini-plane and can be routed on an internal power plane layer.

LAN9252 SQFN Port B Fiber Phy (100BASE-FX) Interface:

1. The traces connecting the transmit outputs (TXPB, pin 62) & (TXNB, pin 63) to the fiber module must be run as differential pairs. 50 ohm microstrip signal paths are recommended.
2. The traces connecting the receive inputs (RXPB, pin 60) & (RXNB, pin 61) from the fiber module must be run as differential pairs. 50 ohm microstrip signal paths are recommended.
3. For differential traces running from the LAN controller to the fiber module, Microchip recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.
4. The +5V power supply for the fiber module should be routed as a mini-plane and can be routed on an internal power plane layer.



CTP / FX-SD / FX-LOS Configuration Pins:

1. There are no critical routing instructions for the CTP / FX-SD / FX-LOS interface.

+3.3V Power Supply Connections:

1. Route the VDD33 pin of the LAN9252 SQFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. In addition, route the VDD33 decoupling capacitor for the LAN9252 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
3. Route the VDD33TXRX1 pin of the LAN9252 SQFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.
4. In addition, route the VDD33TXRX1 decoupling capacitor for the LAN9252 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
5. Also, route the VDD33TXRX1 bulk capacitor for the LAN9252 SQFN power pins as short as possible directly to the VDD33TXRX1 power plane.
6. Route the VDD33TXRX2 pin of the LAN9252 SQFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.
7. In addition, route the VDD33TXRX2 decoupling capacitor for the LAN9252 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
8. Also, route the VDD33TXRX2 bulk capacitor for the LAN9252 SQFN power pin as short as possible directly to the VDD33TXRX2 power plane.
9. Route the VDD33BIAS (pin 58) of the LAN9252 SQFN directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.
10. In addition, route the VDD33BIAS decoupling capacitor for the LAN9252 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.
11. Also, route the VDD33BIAS bulk capacitor for the LAN9252 SQFN power pin as short as possible directly to the VDD33BIAS power plane.



+1.8V to +3.3V Variable I/O Power Supply Connections:

1. Route the (5) VDDIO pins of the LAN9252 SQFN directly into a solid, +1.8V to +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. In addition, route the (5) VDDIO decoupling capacitors for the LAN9252 SQFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+V power plane & digital ground plane) for each cap.

VDDCR:

1. The VDDCR (pins 6, 24 & 38) must be routed with a heavy, wide trace with multiple vias to the three decoupling caps and the single bulk capacitor associated with it. All three pins and the caps should be routed directly into a solid, +1.2V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.
2. The VDD12TX1 (pin 56) and the VDD12TX2 pin (pin 59) must be routed with a heavy, wide trace with multiple vias to the two decoupling caps and the single bulk capacitor associated with them. Pins 56 & 59 and the caps should be routed through the associated ferrite bead directly into a solid, +1.2V power plane (VDDCR).

Ground Connections:

1. The single digital ground pin (pin 65, EDP) on the LAN9252 SQFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 36 power vias in a 6x6 grid.
2. We recommend that all Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.
2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.



RBIAS Resistor:

1. The RBIAS resistor (pin 57) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the RBIAS resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-ups/Pull-down connections.

MII Interface:

1. The MII interface on the LAN9252 should be constructed using 68-ohm traces.
2. The value of the series termination (if utilized) and the impedance of the internal driver of the LAN9252 should roughly equal that of the PCB trace impedance. The value of the series termination can be adjusted slightly to achieve the best signal integrity possible.
3. The trace lengths of the MII signals should be matched to within 1.0".

Host Bus Interface (HBI) Indexed Mode:

1. There are no critical routing instructions for the Host Bus Interface (HBI) Indexed Mode connections for the LAN9252.
2. Microchip recommends consulting the processor's vendor for specific HBIM routing guidelines.

Host Bus Interface (HBI) Multiplexed Mode:

1. There are no critical routing instructions for the Host Bus Interface (HBI) Multiplexed Mode connections for the LAN9252.
2. Microchip recommends consulting the processor's vendor for specific HBIMM routing guidelines.

EtherCAT® Digital I/O Mode:

1. There are no critical routing instructions for the EtherCAT® Digital I/O Interface connections for the LAN9252.



Serial Peripheral Interface (SPI) Bus Mode:

1. There are no critical routing instructions for the Serial Peripheral Interface (SPI) Mode connections for the LAN9252.

GPI Mode:

1. There are no critical routing instructions for the GPI Mode connections for the LAN9252.

GPO Mode:

1. There are no critical routing instructions for the GPO Mode connections for the LAN9252.

LED Pins:

1. There are no critical routing instructions for the LED pins on the LAN9252.

SYNC / LATCH Pins:

1. There are no critical routing instructions for the SYNC / LATCH pins on the LAN9252.

I²C (2-wire) EEPROM Interface:

1. There are no critical routing instructions for the I²C EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

Dedicated Configuration Strap Pins:

1. There are no critical routing instructions for the Dedicated Configuration Strap Pins connections.



Miscellaneous:

1. Microchip recommends utilizing at least a four-layer design for boards for the LAN9252 SQFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.
2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.
3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.
4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.
5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.

