

Designing For LAN9118 Family Footprint Compatibility

1 Introduction

This application note will discuss forward and backward footprint compatibility among the LAN9118 family of Ethernet controllers. Various external component placement strap possibilities supporting configuration of the Ethernet controller will also be discussed.

1.1 References

All references can be found at SMSC's web site: www.smSC.com

- SMSC LAN9118 Family of datasheets
- Application Note 8.13: Suggested Magnetics - an813.pdf
- Application Note 12.5: Designing with the LAN9118 - Getting Started - an125.pdf
- Application Note 12.12: LAN9118 Family Programmers Reference Guide - an1212.pdf
- Reference Design Files
- LAN9118 Reference Design Schematic - 9118sch.pdf
- LAN9118 Reference Design Bill of Materials - 9118bom.pdf

2 The LAN9118 Family of Ethernet Controllers

The LAN9118 family of Ethernet controllers offer a high-performance, cost competitive solution for most embedded applications requiring Ethernet LAN connectivity. The LAN9118 family of Ethernet Controllers include the LAN9115, LAN9116, LAN9117 and LAN9118. [Table 2.1, "LAN9118 Family Comparison"](#), describes the basic feature differences between each family member. As shown, the LAN9118 and LAN9116 support both 16-bit and 32-bit Host Bus architectures.

The LAN9117 and LAN9115 are 16-bit devices. Pins assigned to the upper 16 data bits in the LAN9118 and LAN9116 devices support an external MII interface in the LAN9117 and LAN9115 devices. The external MII feature allows the LAN9117 and LAN9115 devices to support an external PHY. It is important to remember, however, that even though the bus width supported by the LAN9118 family of Ethernet controllers varies externally, the internal bus architecture of all the devices is 32-bits.

Please refer to SMSC's web site (www.smSC.com) for additional information on the differences between each device that would suit a particular application.

Table 2.1 LAN9118 Family Comparison

SMSC LAN DEVICE	COMMENT
LAN9118	32-/16-bit Selectable
LAN9117	16-Bit Only External MII Selectable
LAN9116	32-/16-bit Selectable
LAN9115	16-bit Only External MII Selectable

3 Configuration options

The LAN9118 family of Ethernet controllers utilize pins for device configuration. [Table 3.1, "LAN9118 Family Configuration Pins"](#) denotes the applicable configuration pins.

Note: As shown in the table, some pins are multi-function.

For a complete description of the device pins defined, please refer to the LAN9118, LAN9117, LAN9116 or LAN9115 datasheets available on SMSC's web site outlined in the reference section above.

Table 3.1 LAN9118 Family Configuration Pins

SMSC LAN DEVICE	DEVICE PINS USED FOR CONFIGURATION			
	SPEED_SEL	FIFO_SEL	EEDIO/ GPO3/ TX_EN/ TX_CLK/ (D32/nD16)	MDIO (EXT_PHY_DET)
LAN9118	✓	✓	✓	
LAN9117	✓	✓		✓
LAN9116	✓	✓	✓	
LAN9115	✓	✓		✓

The LAN9118 family reference schematic shown in [Figure 3.1](#) depicts a typical device application. This schematic describes configuration strap options for the full family of LAN9118 Ethernet controllers using the pins defined in [Table 3.1](#).

Note 3.1 It is important to note that this schematic specifically captures a LAN9118 implementation that is compatible with all members of the LAN9118 family of Ethernet controllers.

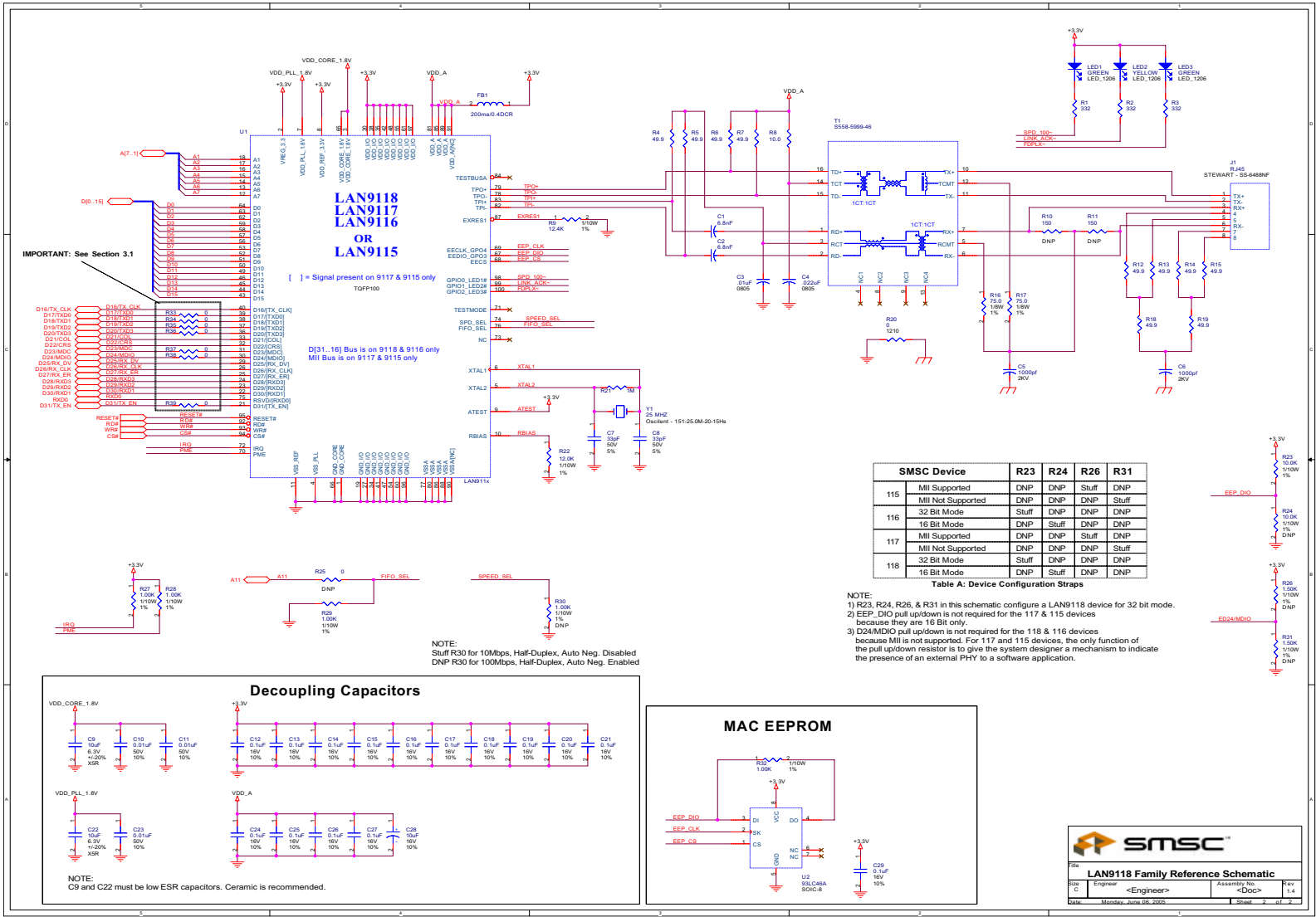


Figure 3.1 LAN9118 Family Reference Schematic

3.1 Migration Between LAN9118/116 and LAN9117/115

PCB footprints for R33 - R39 in [Figure 3.1](#) are only necessary in the unusual case when anticipating the installation of a 16-bit LAN9117/LAN9115 device in a 32-bit LAN9118/LAN9116 system. In this case R33 - R39 must be populated for use with a LAN9118 or LAN9116, and depopulated for use with a LAN9117 or LAN9115. Removal of R33 - R39 prevents contention of the MII outputs with the system data bus when a LAN9117 or LAN9115 is installed. Note that if migration is not a consideration, PCB footprints for R33 - R39 are not required.

[Table 3.2](#) illustrates the requirements for R33 - R39. The table shows migration paths which require PCB footprints for these resistors. Blank boxes do not require PCB footprints. In these cases R33 - R39 may be omitted from the design and the associated signals can be connected directly to the LAN controller. Boxes that are checked require footprints for R33 - R39, and require that these resistors are populated when a LAN9118/LAN9116 is installed, and depopulated when a LAN9117/LAN9115 is installed.

Table 3.2 PCB Footprint Requirements for R33 - R39

SYSTEM DESIGNED FOR...	MIGRATING TO...					
	LAN9118 32-BIT	LAN9118 16-BIT	LAN9117	LAN9116 32-BIT	LAN9116 16-BIT	LAN9115
LAN9118/32-bit			✓			✓
LAN9118/16-bit						
LAN9117						
LAN9116/32-bit			✓			✓
LAN9116/16-bit						
LAN9115						

For example, if a design incorporates a 32-bit data bus for the LAN controller, PCB footprints for resistors R33 - R39 must be included if it is anticipated that this design will utilize a LAN9115 or LAN9117. In such a design, when a LAN9118 or LAN9116 is installed, R33 - R39 are populated with zero-ohm resistors, thereby fully connecting the upper portion of the data bus. When a LAN9117 or LAN9115 is installed, R33 - R39 are depopulated, thereby isolating the upper portion of the system data bus from the MII outputs of the LAN9117/LAN9115.

3.2 EEDIO and MDIO Strap Configurations

Table A, shown in the schematic diagram in [Figure 3.1](#) above, defines the device configuration straps allowing the configuration of the LAN9118 family of Ethernet controllers for:

- 32-bit Host Bus Mode Support
- 16-bit Host Bus Mode Support
- External MII Support

Table A in [Figure 3.1](#), enumerates the specific population options for device configuration.

3.3 FIFO_SEL and SPEED_SEL Strap Configurations

As shown in [Figure 3.1](#), pins FIFO_SEL and SPEED_SEL are used as device configuration straps allowing the configuration of the LAN9118 family of Ethernet controllers for:

- Network Default Mode Support (SPEED_SEL; pull-down resistor R30)
- FIFO Direct Access Mode Support (FIFO_SEL; pull-down resistor R29 and series resistor R25)

Resistor R30 configures the default network speed for each device in the LAN9118 Family. When R30 is populated, the LAN9118 family device is configured for 10Mbps, Half-Duplex and Auto-Negotiation is disabled. When R30 is not populated, the LAN9118 family device is configured for 100Mbps, Half-Duplex and Auto-Negotiation is enabled.

Resistor R29, which is used to pull-down FIFO_SEL, is populated when FIFO direct access mode support is not required. In this case, R25 must also be removed to isolate FIFO_SEL from address line A11.

When R25 is populated and R29 is depopulated, the TX and RX FIFOs are accessed via address decode. The FIFO_SEL pin can be tied to a higher-order address bit (A11 for example) to support this mode of operation. In this case, FIFO direct access read and write cycles occur when A11 is driven high.

Note: Address line A11 is used in this example because it corresponds to the 2KB offset from the base address of the LAN controller. This address line may vary in other system implementations. Using a high-order address line is one implementation. Other implementations are possible.

Please refer to the appropriate LAN9118 Family of datasheet(s) for additional information on this function.

4 Additional Notes

- The external pull down on the EXRES1 pin must be a 12.4K Ohm, 1% resistor.
- External pull down on RBIAS must be a 12.0K Ohm, 1% resistor.
- It is required that C9 and C22 are low ESR 10uF, ceramic Capacitors.



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