

REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		12-16-11
B	Added 2K EEPROM Size to EEPROM Interface Section		1-17-13

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DOCUMENT DESCRIPTION
Schematic Checklist for the LAN9513, 64-pin QFN Package

 	SMSC 80 Arkay Drive Hauppauge, New York 11788	
	Document Number	Revision
	SC471236	B

Schematic Checklist for LAN9513

Information Particular for the 64-pin QFN Package

LAN9513 QFN Phy Interface:

1. TXP (pin 55); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.
2. TXN (pin 56); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.
3. For Transmit Channel connection and termination details, refer to Figure 1.
4. RXP (pin 52); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.
5. RXN (pin 53); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω , 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.
6. For Receive Channel connection and termination details, refer to Figure 2.

LAN9513 QFN Magnetics:

1. The center tap connection on the LAN9513 side for the transmit channel must be connected to VDD33A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.
2. The center tap connection on the LAN9513 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a $0.022\ \mu\text{F}$ capacitor is required from the receive channel center tap of the magnetics to digital ground.
3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a $1000\ \text{pF}$, 2KV capacitor (C_{magterm}) to chassis ground.
4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a $1000\ \text{pF}$, 2KV capacitor (C_{magterm}) to chassis ground.
5. Only one $1000\ \text{pF}$, 2KV capacitor (C_{magterm}) to chassis ground is required. It is shared by both TX & RX center taps.
6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 55) of the LAN9513 QFN.
7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN (pin 56) of the LAN9513 QFN.
8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 52) of the LAN9513 QFN.
9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN (pin 53) of the LAN9513 QFN.
10. When using the SMSC LAN9513 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 4 & 5 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:
 - a) Pins 7 & 8 can be connected together with two 49.9 Ω resistors. The common connection of these resistors should be connected through a third 49.9 Ω to the 1000 pF, 2KV capacitor (C_{rjterm}).
 - b) For a lower component count, the resistors can be combined. The two 49.9 Ω resistors in parallel look like a 25 Ω resistor. The 25 Ω resistor in series with the 49.9 Ω makes the whole circuit look like a 75 Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75 Ω resistor in series with the 1000 pF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.
3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN9513 QFN are 19, 27, 33, 39, & 46. They require a connection to +3.3V.
2. Each power pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9513. The capacitor size should be SMD_0603 or smaller.
3. The analog supply (VDD33A) pins on the LAN9513 QFN are 5, 10, 49, 51, 54, 57 & 64. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
4. Each VDD33A pin should have one .01 μ F (or smaller) capacitor to decouple the LAN9513. The capacitor size should be SMD_0603 or smaller.

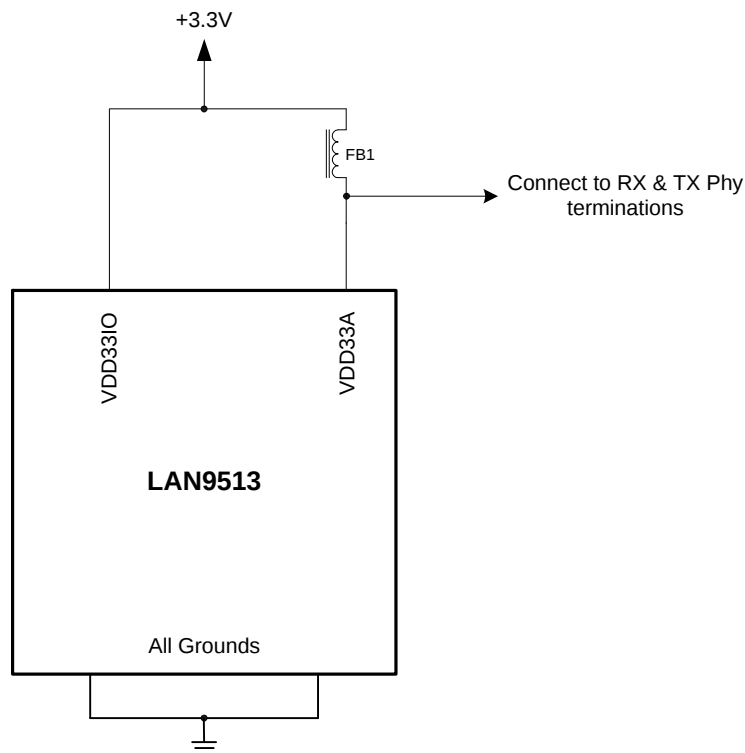


Figure 3 - +3.3V Power Supply Connections

VDD18CORE:

1. VDD18CORE (pins 15 & 38), these two pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF decoupling/bypass capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 38 requires a bulk capacitor placed as close as possible to pin 38. The bulk capacitor must have a value of at least 1.0 μF , and have an ESR (equivalent series resistance) of no more than 2.0 Ω . SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD18CORE to VDD18USBPLL.

Caution: This +1.8V supply is for internal logic only and LAN9513 use only. **Do Not** power other external circuits or devices with this supply.

VDD18USBPLL:

1. VDD18USBPLL (pin 62), this pin supplies power from the +1.8V USB PLL regulator. This pin requires a bulk capacitor placed as close as possible to pin 62. The bulk capacitor must have a value of at least 1.0 μF , and have an ESR (equivalent series resistance) of no more than 2.0 Ω . SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.
2. The VDD18USBPLL pin should also have one .01 μF (or smaller) bypass capacitor on pin 62. The capacitor size should be SMD_0603 or smaller.
3. VDD18ETHPLL (pin 48), this pin supplies power to the core PLL. This pin must be connected to VDD18USBPLL through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.
4. The VDD18ETHPLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN9513. The capacitor size should be SMD_0603 or smaller.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD18USBPLL to VDD18CORE.

Caution: This +1.8V supply is for internal logic only and LAN9513 use only. **Do Not** power other external circuits or devices with this supply.

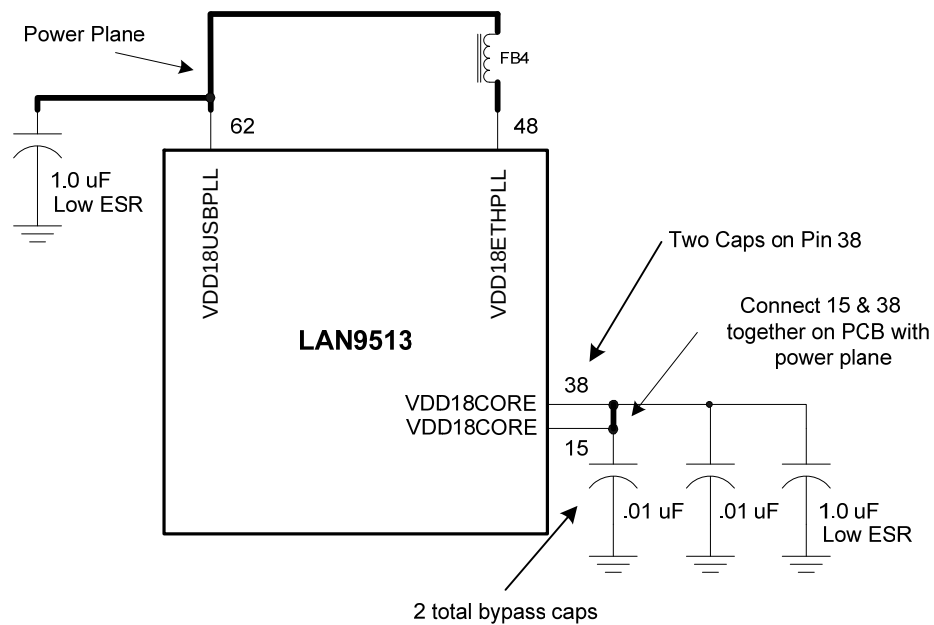


Figure 4 - LAN9513 +1.8V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN9513QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN9513 must be connected directly to a solid, contiguous digital ground plane.
2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9513 QFN. For exact specifications and tolerances refer to the latest revision LAN9513 data sheet.
2. XI (pin 61) on the LAN9513 QFN is the clock circuit input. This pin requires a 15 – 33 pF capacitor to digital ground. One side of the crystal connects to this pin.
3. XO (pin 60) on the LAN9513 QFN is the clock circuit output. This pin requires a matching 15 – 33 pF capacitor to ground and the other side of the crystal.
4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.
5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

EEPROM Interface:

1. EECS (pin 24) on the LAN9513 QFN connects to the external EEPROM's CS pin.
2. EECLK (pin 23) on the LAN9513 QFN connects to the external EEPROM's serial clock pin.
3. EEDI (pin 26) on the LAN9513 QFN connects to the external EEPROM's Data Out pin.
4. EEDO (pin 25) on the LAN9513 QFN connects to the external EEPROM's Data In pin.
5. Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.

EXRES Resistor:

1. EXRES (pin 50) on the LAN9513 QFN should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

USBRBIAS Resistor:

1. USBRBIAS (pin 63) on the LAN9513 QFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

Required External Pull-ups/Pull-downs:

1. GPIO0 (pin 20) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
2. GPIO1 (pin 21) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
3. GPIO2 (pin 22) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
4. GPIO3 (pin 35) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
5. GPIO4 (pin 36) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
6. GPIO5 (pin 37) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
7. GPIO6 (pin 42) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.
8. GPIO7 (pin 43) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

USB Upstream Interface Port 0:

1. USBDP0 (pin 59), this pin is the USB Upstream channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, upstream USB connector (Type “B”).
2. USBDM0 (pin 58), this pin is the USB Upstream channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, upstream USB connector (Type “B”).
3. Typical Bus Powered applications will connect pin 1 (VCC) on a standard 4-pin, upstream USB connector (Type “B”) directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the LAN9513.
4. We recommend no bulk capacitance be placed on pin 1 (VCC) of the USB connector in Bus Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB specification.
5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, upstream USB connector (Type “B”) directly to digital ground.
6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.
7. VBUS_DET (pin 11), this pin detects the state of the supplied upstream power. This pin must be tied to VDD33IO when operating in Bus-Powered mode. When using the LAN9513 in Self-Powered mode, this pin should be tied to the USB power through the recommended circuit below. This pin has a weak internal pull-down.

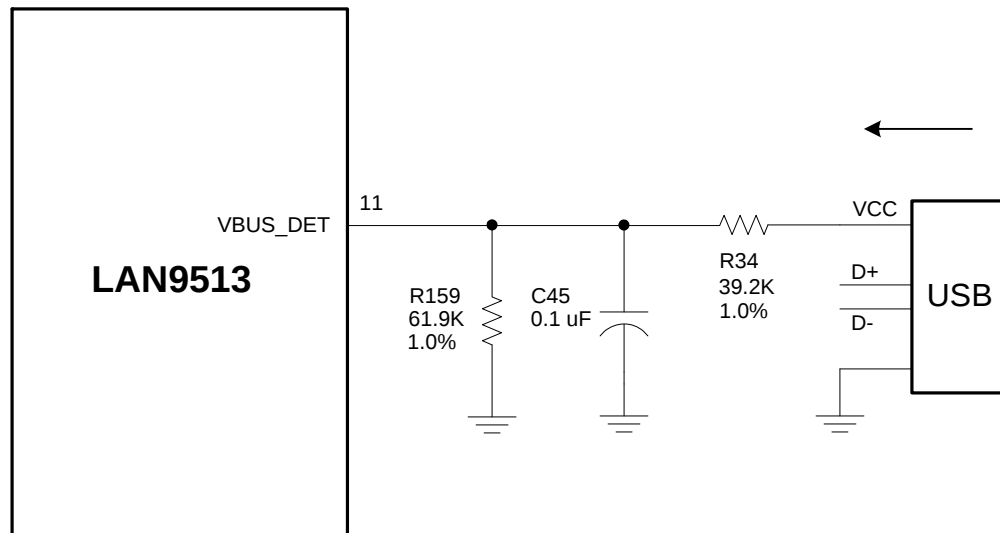


Figure 5 – Self-Powered Mode Circuitry

USB Downstream Interface Port 2:

1. USBDP2 (pin 2), this pin is the USB Downstream Port 2 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").
2. USBDM2 (pin 1), this pin is the USB Downstream Port 2 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").
3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the LAN9513 data sheet for more details on using a poly fuse for USB power distribution.
4. In addition, SMSC recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.
5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.
6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.
7. PRTCTL2 (pin 14), this Input/Output pin is the USB downstream Port 2 channel power control pin. When used as an output, this pin enables power to the USB downstream Port 2 device. When used as an output, the polarity of the signal is an enable high.

When used as an input, this pin samples the output signal from the power distribution switch for the USB downstream Port 2 device. An over-current condition is indicated when the signal input is low.

For this reason, care must be taken when selecting a power distribution switch for the LAN9513. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with our combined Fault/Enable PRTCTL2 pin. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

USB Downstream Interface Port 3:

1. USBDP3 (pin 4), this pin is the USB Downstream Port 3 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").
2. USBDM3 (pin 3), this pin is the USB Downstream Port 3 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").
3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the LAN9513 data sheet for more details on using a poly fuse for USB power distribution.
4. In addition, SMSC recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.
5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.
6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.
7. PRTCTL3 (pin 16), this Input/Output pin is the USB downstream Port 3 channel power control pin. When used as an output, this pin enables power to the USB downstream Port 3 device. When used as an output, the polarity of the signal is an enable high.

When used as an input, this pin samples the output signal from the power distribution switch for the USB downstream Port 3 device. An over-current condition is indicated when the signal input is low.

For this reason, care must be taken when selecting a power distribution switch for the LAN9513. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with our combined Fault/Enable PRTCTL3 pin. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

USB Downstream Interface Port 4:

1. USBDP4 (pin 7), this pin is the USB Downstream Port 4 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").
2. USBDM4 (pin 6), this pin is the USB Downstream Port 4 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").
3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the LAN9513 data sheet for more details on using a poly fuse for USB power distribution.
4. In addition, SMSC recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.
5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.
6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.
7. PRTCTL4 (pin 17), this Input/Output pin is the USB downstream Port 4 channel power control pin. When used as an output, this pin enables power to the USB downstream Port 4 device. When used as an output, the polarity of the signal is an enable high.

When used as an input, this pin samples the output signal from the power distribution switch for the USB downstream Port 4 device. An over-current condition is indicated when the signal input is low.

For this reason, care must be taken when selecting a power distribution switch for the LAN9513. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with our combined Fault/Enable PRTCTL4 pin. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

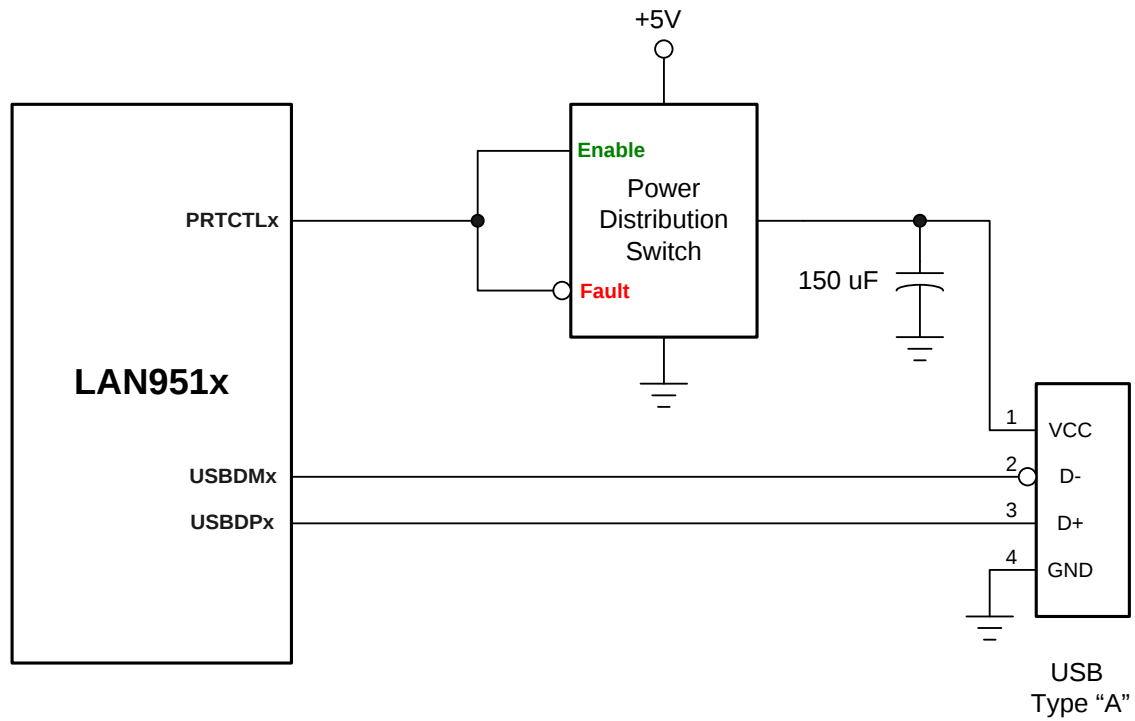


Figure 6 – Typical LAN9513 USB Downstream Port Application

Configuration Straps:

1. All configuration strap values are latched in on Power-On Reset and System Reset. For more detailed information of each bit and functionality, consult the latest version of the LAN9513 data sheet.
2. AUTOMDIX_EN (pin 41), this pin determines the default Auto MDIX setting. The settings are as follows:

0 = Auto MDIX is disabled
1 = Auto MDIX is enabled

See the latest version of the LAN9513 data sheet for complete details. This pin has a weak internal pull-up and can be driven low with an external 10.0K Ω resistor to digital ground.

Miscellaneous:

1. There are three No-Connect pins on the LAN9513. It is very important that these pins remain as no-connects. These pins are 8, 9 & 18.
2. nRESET (pin 12), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9513. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9513 will rely on its internal power-on reset circuitry.
3. nFDX_LED (pin 20), nLNKA_LED (pin 21) & nSPD_LED (pin 22), can be programmed via register settings to display various Ethernet activity such as Speed, Link & Duplex Status. See the latest version of the LAN9513 data sheet for complete details. These pins have weak internal pull-ups.
4. CLK24_EN (pin 44), this pin enables the generation of a 24 MHz clock on the CLK24_OUT pin. This input signal has no internal termination and should be terminated with an external resistor. The settings are as follows:

1. 0 = CLK_24_OUT is disabled
2. 1 = CLK_24_OUT is enabled

See the latest version of the LAN9513 data sheet for complete details.

5. CLK24_OUT (pin 45), this pin outputs a 24 MHz clock that can be used as a reference clock for a partner hub.
6. The LAN9513 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN9513 data sheet.
7. TEST1 (pin 13), this pin must remain as a no-connection in order to ensure proper operation.
8. TEST2 (pin 34), this pin must be tied directly to digital ground in order to ensure proper operation.
9. TEST3 (pin 40), this pin must be tied directly to +3.3V in order to ensure proper operation.
10. TEST4 (pin 47), this pin must remain as a no-connection in order to ensure proper operation.
11. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.
12. Be sure to incorporate enough bulk capacitors (4.7 - 22 μ F caps) for each power plane.

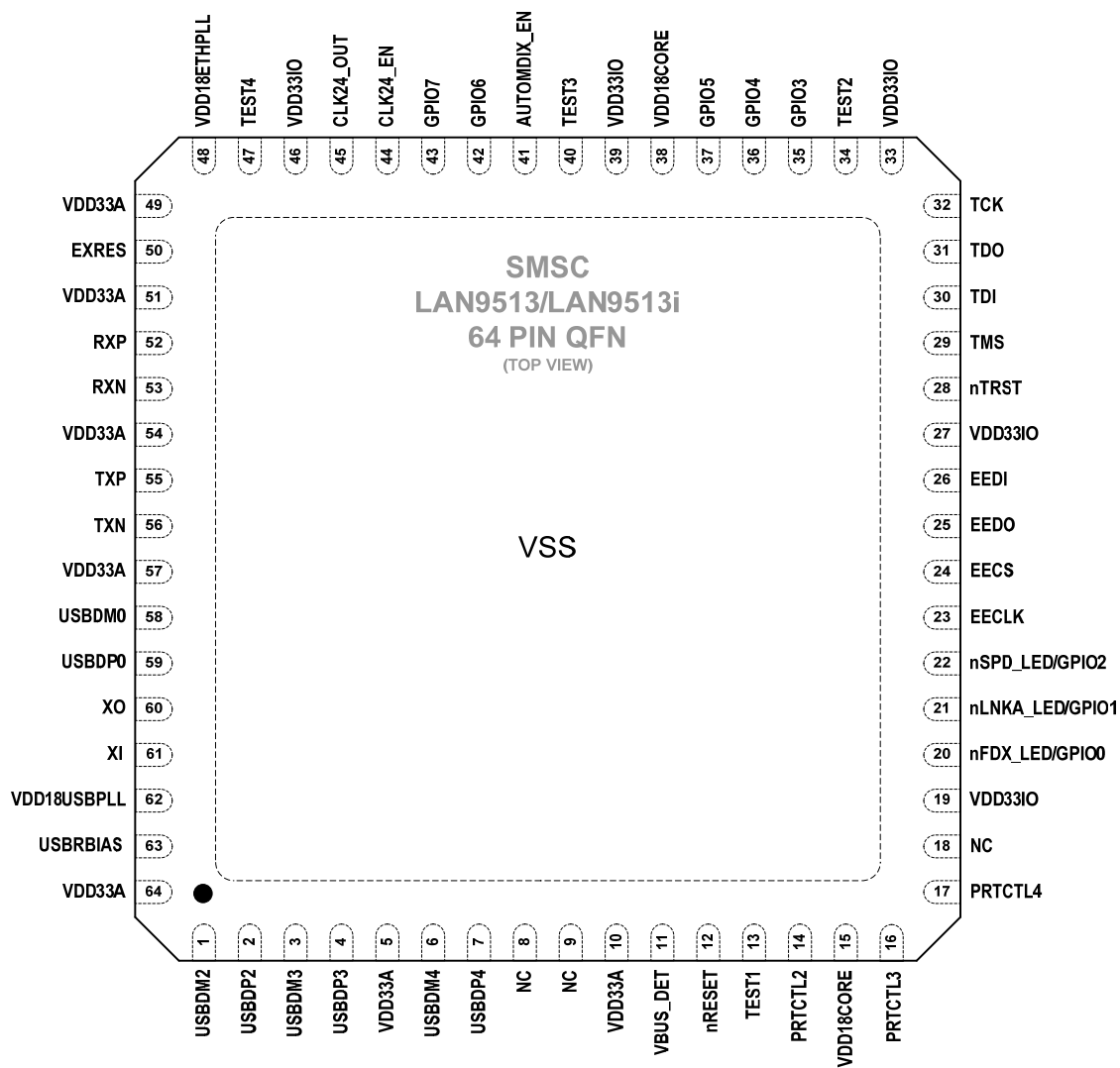
LAN9513 QFN QuickCheck Pinout Table:

Use the following table to check the LAN9513 QFN shape in your schematic.

LAN9513 QFN			
Pin No.	Pin Name	Pin No.	Pin Name
1	USBDM2	33	VDD33IO
2	USBDP2	34	TEST2
3	USBDM3	35	GPIO3
4	USBDP3	36	GPIO4
5	VDD33A	37	GPIO5
6	USBDM4	38	VDD18CORE
7	USBDP4	39	VDD33IO
8	NC1	40	TEST3
9	NC2	41	AUTOMDIX_EN
10	VDD33A	42	GPIO6
11	VBUS_DET	43	GPIO7
12	nRESET	44	CLK24_EN
13	TEST1	45	CLK24_OUT
14	PRTCTL2	46	VDD33IO
15	VDD18CORE	47	TEST4
16	PRTCTL3	48	VDD18ETHPLL
17	PRTCTL4	49	VDD33A
18	NC3	50	EXRES
19	VDD33IO	51	VDD33A
20	nFDX_LED / GPIO0	52	RXP
21	nLNKA_LED / GPIO1	53	RXN
22	nSPD_LED / GPIO2	54	VDD33A
23	EECLK	55	TXP
24	EECS	56	TXN
25	EEDO	57	VDD33A
26	EEDI	58	USBDM0
27	VDD33IO	59	USBDP0
28	nTRST	60	XO
29	TMS	61	XI
30	TDI	62	VDD18USBPLL
31	TDO	63	USBRBIAS
32	TCK	64	VDD33A
65		EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package	

Notes:

LAN9513 QFN Package Drawing:



Reference Material:

1. SMSC LAN9513 Data Sheet; check web site for latest revision.
2. SMSC LAN9514 CEB Schematic, Assembly No. 6569 ; check web site for latest revision.
3. SMSC LAN9514 CEB PCB, Assembly No. 6569 ; order PCB from web site.
4. SMSC LAN9514 CEB PCB Bill of Materials, Assembly No. 6569 ; check web site for latest revision.
5. CEB stands for Customer Evaluation Board.
6. SMSC LAN9513 Reference Design, check web site for latest revision.
7. SMSC Reference Designs are schematics only; there are no associated PCBs.
8. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smisc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smisc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm