

---

**AT07973: SAM G51 Schematic Checklist**

---

**ATSAM G51**

---

**Introduction**

---

A good hardware design comes from a proper schematic. Since SAM G51 devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when building and reviewing the schematics of a SAM G51 application design.

The document covers the following general aspect:

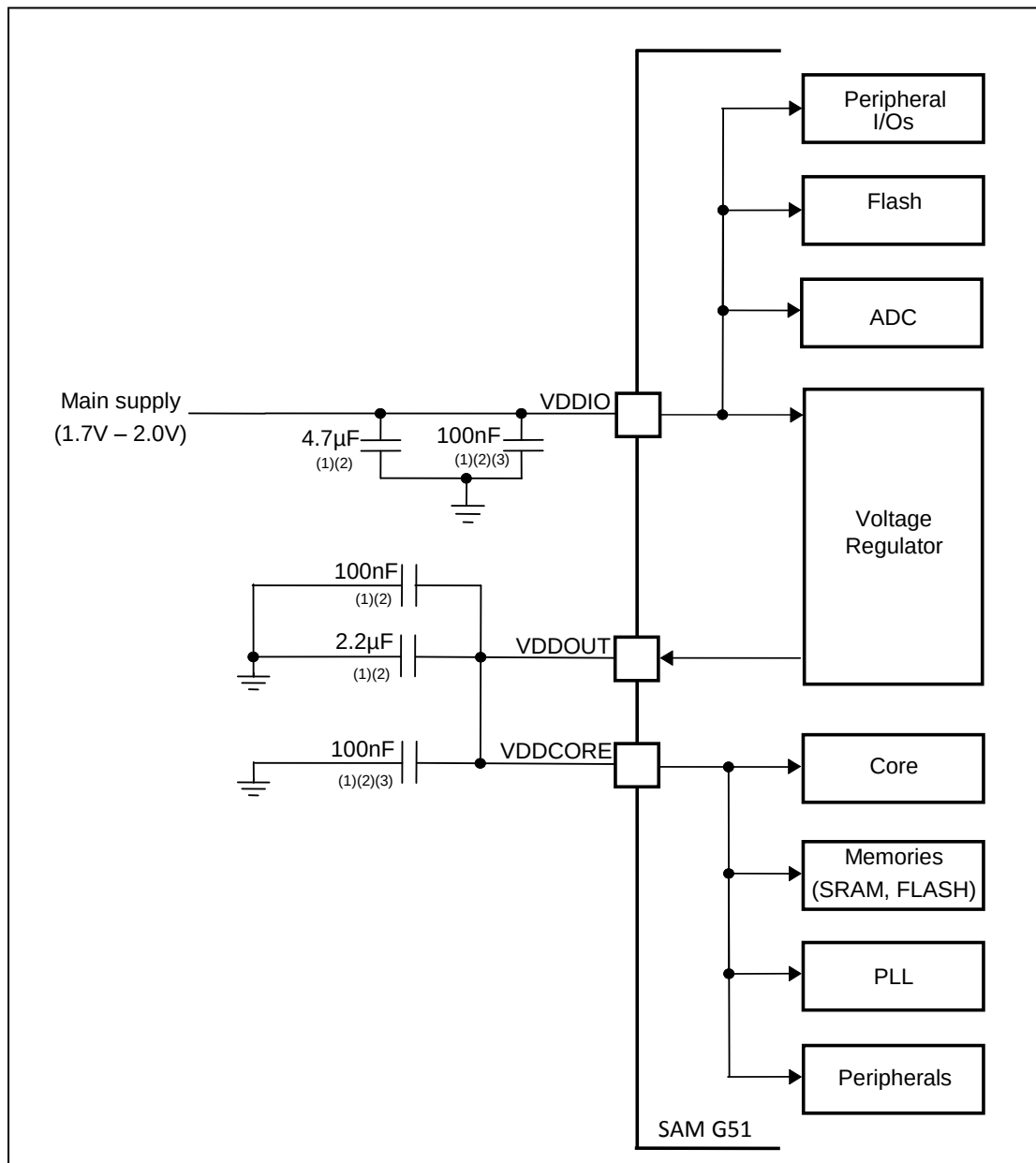
- Power supply strategies
- Clock and crystal oscillators
- JTAG and SWD debug ports
- Suggested reading

# 1 Schematic Checklist

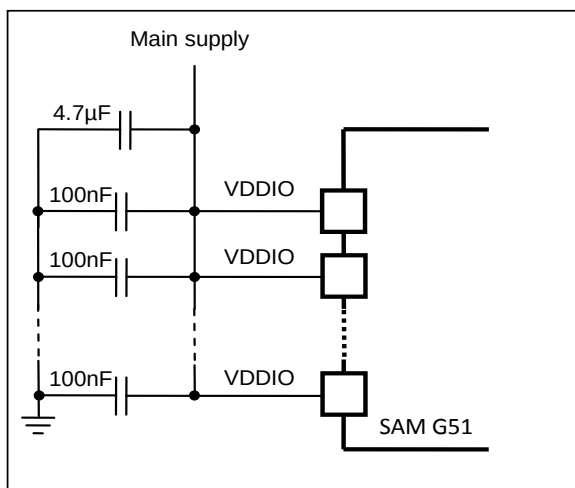
## 1.1 Power Supply Strategy

Single power supply strategy is mandatory on SAM G51. VDDCORE should always be connected to VDDOUT. [Figure 1-1](#) shows the standard power supply.

**Figure 1-1. Power Supply Schematic Example**



- Notes:
1. These values are given only as a typical example.
  2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.
  3. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



The following checklist (Table 1-1) must be followed in order to ensure correct hardware configuration for power supply.

**Table 1-1. Single Power Supply Checklist**

| ✓ | Signal name | Recommended pin connection                                                                                  | Description                                                                                                                                                                                                         |
|---|-------------|-------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   | VDDIO       | 1.7V to 2.0V<br>Decoupling/Filtering capacitors<br>(100nF and 4.7µF) <sup>(1)(2)</sup>                      | Powers the peripheral I/Os, Flash memory (dual rail), ADC, 32kHz crystal oscillator and oscillator pads. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. |
|   | VDDOUT      | Decoupling/filtering capacitor<br>(100nF and 2.2µF) <sup>(1)(2)</sup>                                       | 1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.                                                                                                    |
|   | VDDCORE     | Must be connected directly to<br>VDDOUT pin.<br>Decoupling/filtering capacitor<br>(100nF) <sup>(1)(2)</sup> | Powers the Core, the embedded memories (SRAM, Flash), the PLL, and integrated peripherals.                                                                                                                          |
|   | GND         | Ground                                                                                                      | Ground pins GND are common to VDDIO and VDDCORE                                                                                                                                                                     |

Notes: 1. These values are given only as typical examples.  
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.

## 1.2 Clocks and Oscillators Configuration

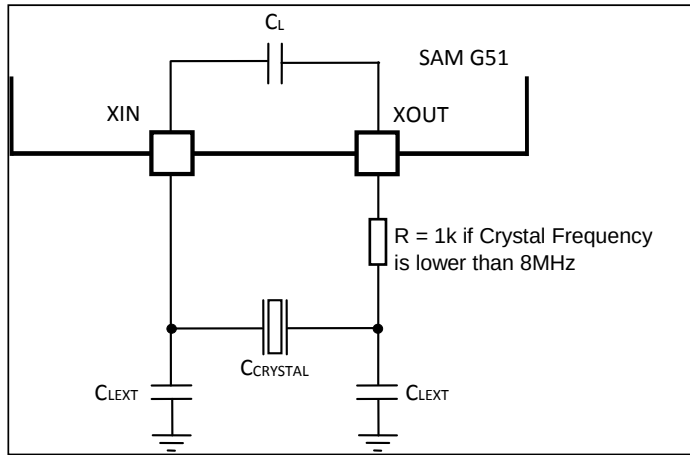
There are three possible configurations for Main and 32kHz clocks:

- Oscillator in Normal Mode
- Oscillator in Bypass
- Internal RC Oscillator

### 1.2.1 Main Clock/oscillators

Figure 1-2 shows a standard main Crystal hardware implementation.

**Figure 1-2. Main Crystal Schematic Example**



The following checklist (Table 1-2) must be followed in order to ensure correct hardware configuration for main Clock/oscillators.

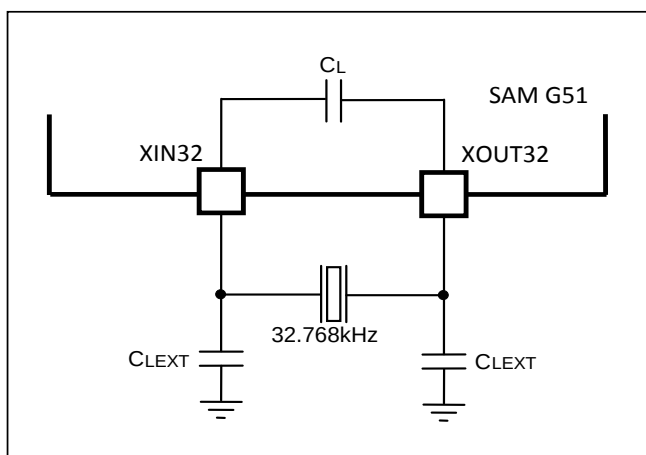
**Table 1-2. Main Clock, Oscillators Checklist**

| ✓ | Signal name                                               | Recommended pin connection                                                                                                                                                                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---|-----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   | PB9/XIN PB8/XOUT<br><b>Main Oscillator in Normal Mode</b> | Crystals between 3 and 20MHz<br><br>Capacitors on XIN and XOUT (crystal load capacitance dependent)<br><br>1kΩ resistor on XOUT only required for crystals with frequencies lower than 8MHz. | Internal Equivalent Load Capacitance ( $C_L = 12.5\text{pF}$ to $17.5\text{pF}$ ):<br><br>Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate.<br><br>The external load capacitance is calculated with the following formula:<br>$C_{LEXT} = 2 (C_{crystal} - C_L - C_{PCB})$<br><br>Refer to the <i>Crystal Oscillators Design Consideration Information</i> section of the SAM G5x Series Datasheet.<br><br><b>By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.</b> |
|   | PB9/XIN PB8/XOUT<br><b>Main Oscillator in Bypass Mode</b> | PB9/XIN: external clock source<br>PB8/XOUT: can be left unconnected or used as GPIO.                                                                                                         | 1.7V to 2.0V Square wave signal ( $V_{DDIO}$ )<br>External Clock Source up to 50MHz Duty Cycle: 40 to 60%<br><br><b>By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.</b>                                                                                                                                                                                                                                                                                                                        |
|   | 8/16/24MHz<br><b>Fast Internal RC Oscillator</b>          | PB9/XIN and PB8/XOUT: can be left unconnected or used as GPIO                                                                                                                                | Powered up by $V_{DDIO}$<br>The output frequency is configurable through the PMC registers.<br>The Fast RC oscillator is calibrated in production. The frequency can be trimmed by software.<br>Duty Cycle: 40 to 60%<br><br><b>By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.</b>                                                                                                                                                                                                            |

## 1.2.2 32kHz Clock/oscillators

Figure 1-3 shows a standard 32kHz Crystal hardware implementation.

Figure 1-3. 32kHz Crystal Schematic Example



The following checklist (Table 1-3) must be followed in order to ensure correct hardware configuration for 32kHz Clock/oscillator.

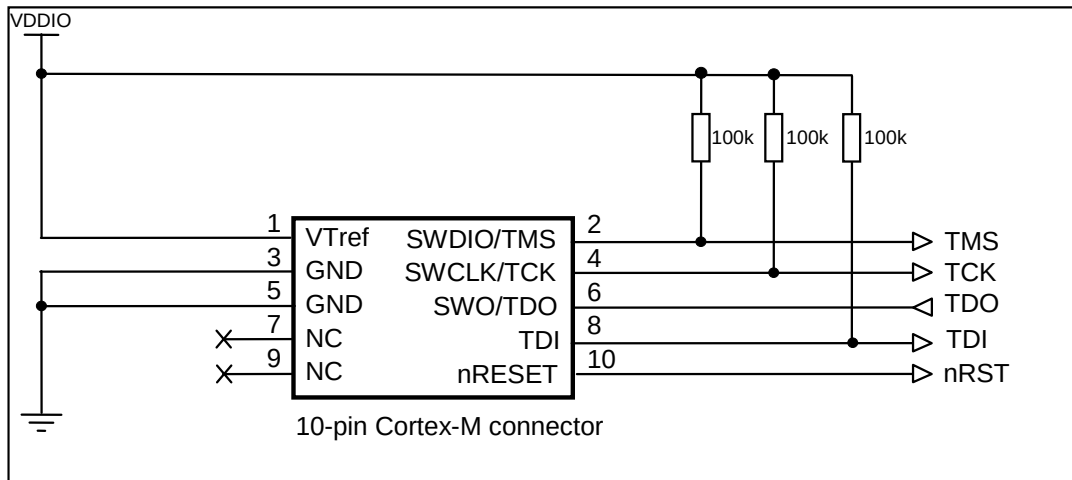
Table 1-3. 32kHz Clock, Oscillators Checklist

| <input checked="" type="checkbox"/> | Signal name                                                           | Recommended pin connection                                                              | Description                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                     | PA7/XIN32<br>PA8/XOUT32<br><br><b>32kHz Crystal used</b>              | 32.768kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)   | Internal parasitic capacitance $C_{para}=0.7pF$ Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate.<br>$C_{LEXTmax}=17pF$<br>$C_{LEXT}= 2 \times (C_{crystal} - C_{para} - C_{pcb})$<br>Refer to the <i>Crystal Oscillators Design Consideration Information</i> section of the SAM G5x Series Datasheet.<br><b>By default at start-up the chip runs out of the embedded 32kHz RC oscillator</b> |
|                                     | PA7/XIN32<br>PA8/XOUT32<br><br><b>32kHz Oscillator in bypass mode</b> | PA7/XIN32: external clock source<br>PA8/XOUT32: can be left unconnected or use as GPIO. | 1.7V to 2.0V Square wave signal ( $V_{DDIO}$ )<br>External Clock Source up to 44kHz<br>Duty Cycle: 40 to 60%<br><b>By default at start-up the chip runs out of the embedded 32kHz RC oscillator</b>                                                                                                                                                                                                                         |

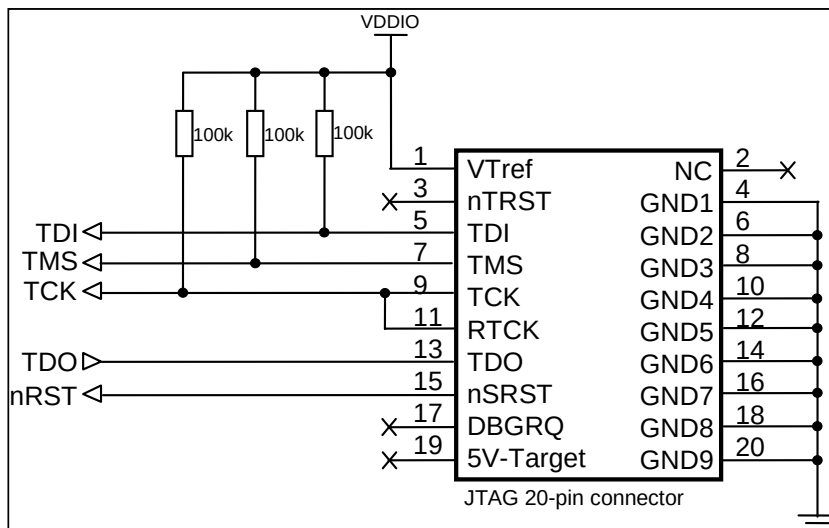
## 1.3 Serial Wire and JTAG

Figure 1-4, Figure 1-5, Figure 1-6, and Figure 1-7 shows a standard JTAG/SWD hardware implementation with 10-pin Cortex®-M connector and 20-pin connector. It is recommended to establish accessibility to a JTAG/SWD connector for debug in any case.

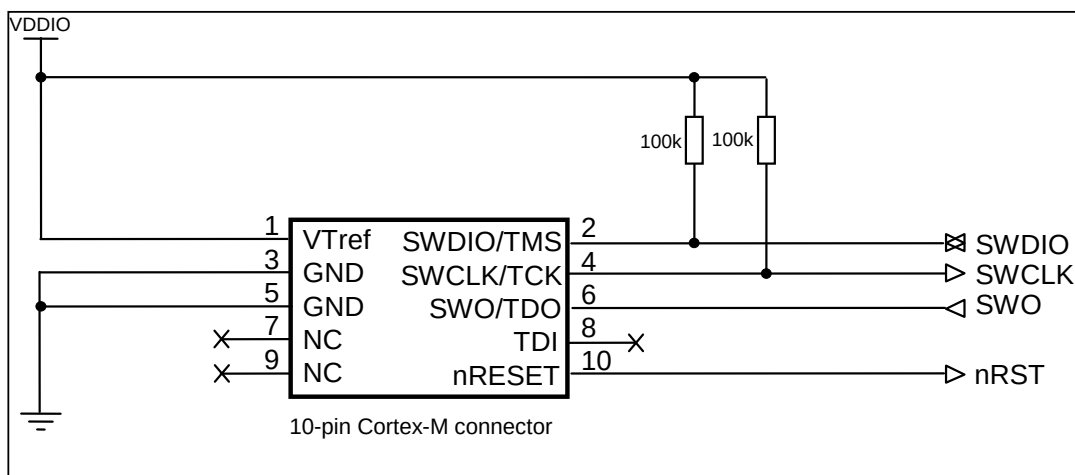
**Figure 1-4. JTAG Schematic Example: 10-pin Cortex-M Connector**



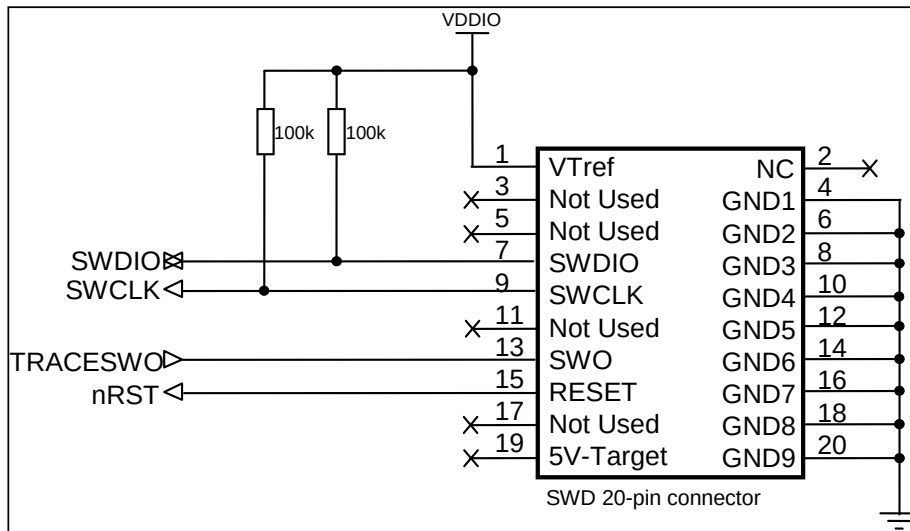
**Figure 1-5. JTAG Schematic Example: JTAG 20-pin Connector**



**Figure 1-6. SWD Schematic Example: 10-pin Cortex-M Connector**



**Figure 1-7. SWD Schematic Example: SWD 20-pin Connector**



The following checklist ([Table 1-4](#)) must be followed in order to ensure correct hardware configuration for JTAG/SWD.

**Table 1-4. Serial Wire and JTAG Checklist**

| <input checked="" type="checkbox"/> | Signal name      | Recommended pin connection                                                                                                                                                   | Description                                                                               |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
|                                     | TCK/SWCLK/PB7    | Application dependent<br>If debug mode is not required this pin can be use as GPIO                                                                                           | Reset State:<br>- SWJ-DP Mode<br>- Internal pull-up disabled<br>- Schmitt Trigger enabled |
|                                     | TMS/SWDIO/PB6    | Application dependent<br>If debug mode is not required this pin can be use as GPIO                                                                                           | Reset state:<br>- SWJ-DP Mode<br>- Internal pull-up disabled<br>- Schmitt Trigger enabled |
|                                     | TDI/PB4          | Application dependent<br>If debug mode is not required this pin can be use as GPIO                                                                                           | Reset state:<br>- SWJ-DP Mode<br>- Internal pull-up disabled<br>- Schmitt Trigger enabled |
|                                     | TDO/TRACESWO/PB5 | Application dependent<br>If debug mode is not required this pin can be use as GPIO                                                                                           | Reset state:<br>- SWJ-DP Mode<br>- Internal pull-up disabled<br>- Schmitt Trigger enabled |
|                                     | JTAGSEL          | Application dependent.<br>Must be tied to V <sub>DDIO</sub> to enter JTAG Boundary Scan.<br><b>In harsh environments, It is strongly recommended to tie this pin to GND.</b> | Permanent Internal pull-down resistor (15kΩ)                                              |

## 1.4 Flash Memory

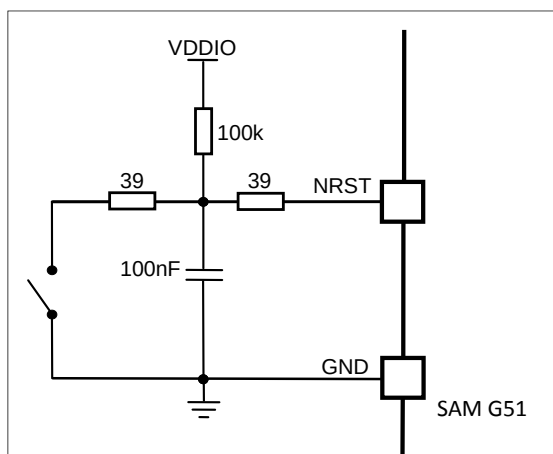
| ✓ | Signal name | Recommended pin connection                                                                 | Description                                                                                                                                                                                                                                                                    |
|---|-------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   | ERASE/PB12  | Application dependent.<br>If hardware erase is not required<br>this pin can be use as GPIO | Internal pull-down resistor (100kΩ).<br>Must be tied to V <sub>DDIO</sub> to erase the General Purpose<br>NVM bits (GPNVMx), the whole Flash content, and<br>the security bit.<br><br>Reset state: Erase Input, with a 100kΩ Internal pull<br>down and Schmitt trigger enabled |

Note: The minimum erase pin assertion for erase effectiveness is 200ms.

## 1.5 Reset and Test Pins

Figure 1-8, shows a standard Reset hardware implementation.

Figure 1-8. Reset Hardware Implementation



| ✓ | Signal name | Recommended pin connection                                                                                                                                                                               | Description                                                                                                      |
|---|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
|   | NRST        | Application dependent.<br>Can be connected to a push button for hardware reset.                                                                                                                          | By default, the NRST pin is configured as an input<br>Permanent internal pull-up resistor to V <sub>DDIO</sub> . |
|   | TST         | TST pin can be left unconnected in normal mode.<br>To enter in FFPI mode TST pin must be tied to V <sub>DDIO</sub> .<br><b>In harsh environments, It is strongly recommended to tie this pin to GND.</b> | Permanent internal pull-down resistor (15kΩ).                                                                    |



## 1.6 PIOs

| <input checked="" type="checkbox"/> | Signal name | Recommended pin connection                              | Description                                                                                                                                                                                                                                                           |
|-------------------------------------|-------------|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                     | PAx - PBx   | Application dependent (Pulled-up on V <sub>DDIO</sub> ) | <p>At reset, all PIOs are in I/O or System I/O mode with Schmitt trigger inputs and internal pull-up enabled.</p> <p>To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled.</p> |

## 2 Suggested Reading

### 2.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. It also contains the electrical specifications and expected characteristics of the device.

The datasheet is available on <http://www.atmel.com/> in the Datasheets section of the product page.

### 2.2 Xplained Pro User Guide

The SAM G51 Xplained PRO user guide contains schematics that can be used as a starting point when designing with the SAM G51 devices. This user guide is available on <http://www.atmel.com/> in the documents section of the SAM G51 Xplained Pro.

### 2.3 ARM Documentation on Cortex-M4 Core

- Cortex-M4 Devices Generic User Guide for revision r0p1
- Cortex-M4 Technical Reference Manual for revision r0p1

These documents are available at <http://www.arm.com/> in the info center section.

### 3 Revision History

| Doc Rev. | Date    | Comments                                                                               |
|----------|---------|----------------------------------------------------------------------------------------|
| 42311B   | 11/2015 | Figure 1-1 has been updated.<br>Main supply voltage has been corrected to 1.7V – 2.0V. |
| 42311A   | 5/2014  | Initial document release.                                                              |



**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA T: (+1)(408) 441.0311 F: (+1)(408) 436.4200 | [www.atmel.com](http://www.atmel.com)

© 2015 Atmel Corporation. / Rev.: Atmel-42311B-SAM-G51-Schematic-Checklist-ApplicationNote\_AT07973\_112015.

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities®, and others are registered trademarks or trademarks of Atmel Corporation in U.S. and other countries. ARM®, ARM Connected® logo, Cortex®, and others are the registered trademarks or trademarks of ARM Ltd. Other terms and product names may be trademarks of others.

**DISCLAIMER:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

**SAFETY-CRITICAL, MILITARY, AND AUTOMOTIVE APPLICATIONS DISCLAIMER:** Atmel products are not designed for and will not be used in connection with any applications where the failure of such products would reasonably be expected to result in significant personal injury or death ("Safety-Critical Applications") without an Atmel officer's specific written consent. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Atmel products are not designed nor intended for use in military or aerospace applications or environments unless specifically designated by Atmel as military-grade. Atmel products are not designed nor intended for use in automotive applications unless specifically designated by Atmel as automotive-grade.