APPLICATION NOTE

AT07973: SAM G51 Schematic Checklist

ATSAM G51

Introduction

A good hardware design comes from a proper schematic. Since SAM G51 devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when building and reviewing the schematics of a SAM G51 application design.

The document covers the following general aspect:

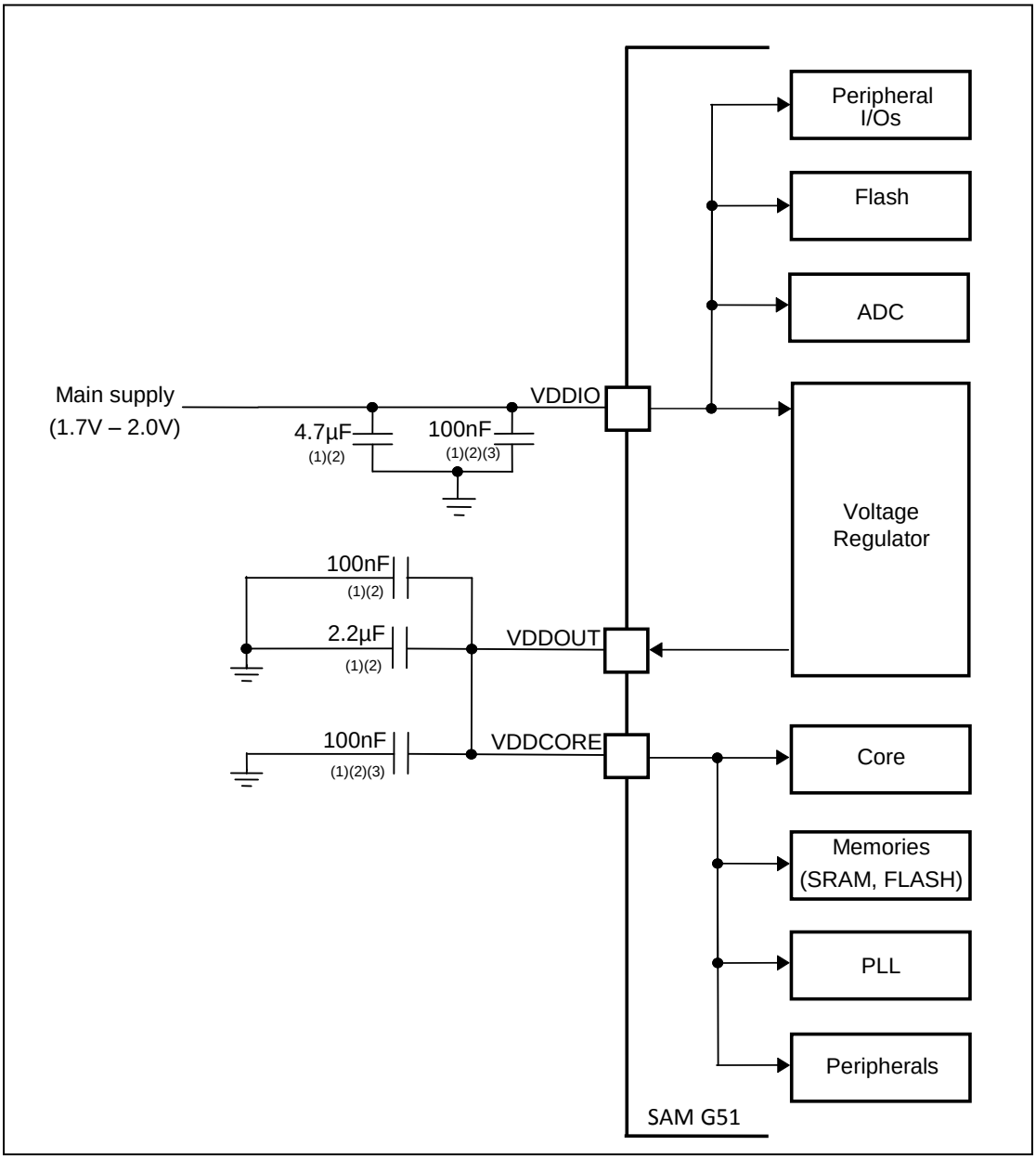
- Power supply strategies
- Clock and crystal oscillators
- JTAG and SWD debug ports
- Suggested reading

1 Schematic Checklist

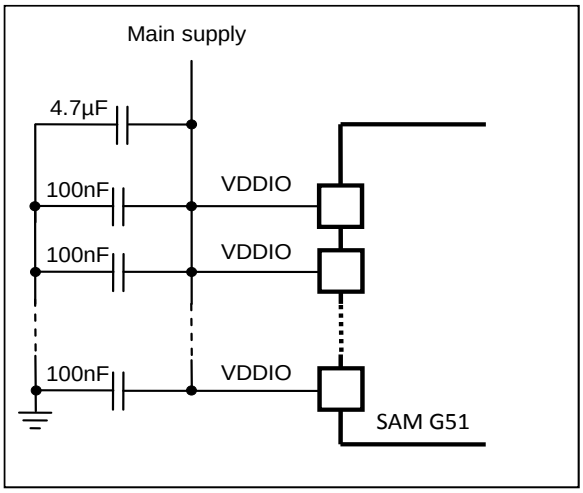
1.1 Power Supply Strategy

Single power supply strategy is mandatory on SAM G51. VDDCORE should always be connected to VDDOUT. Figure 1-1 shows the standard power supply.

Figure 1-1. Power Supply Schematic Example



Notes:
1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



The following checklist (Table 1-1) must be followed in order to ensure correct hardware configuration for power supply.

Table 1-1. Single Power Supply Checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	1.7V to 2.0V Decoupling/Filtering capacitors (100nF and 4.7µF) (1)(2)	Powers the peripheral I/Os, Flash memory (dual rail), ADC, 32kHz crystal oscillator and oscillator pads. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF) (1)(2)	1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling/filtering capacitor (100nF) (1)(2)	Powers the Core, the embedded memories (SRAM, Flash), the PLL, and integrated peripherals.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE

Notes: 1. These values are given only as typical examples.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.

1.2 Clocks and Oscillators Configuration

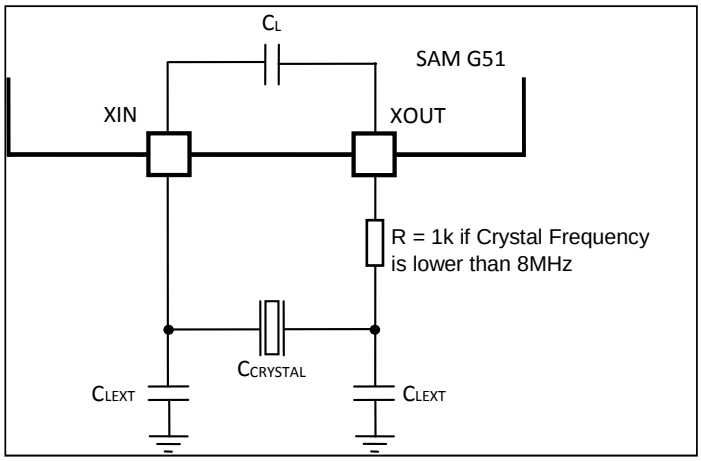
There are three possible configurations for Main and 32kHz clocks:

- Oscillator in Normal Mode
- Oscillator in Bypass
- Internal RC Oscillator

1.2.1 Main Clock/oscillators

Figure 1-2 shows a standard main Crystal hardware implementation.

Figure 1-2. Main Crystal Schematic Example



The following checklist (Table 1-2) must be followed in order to ensure correct hardware configuration for main Clock/oscillators.

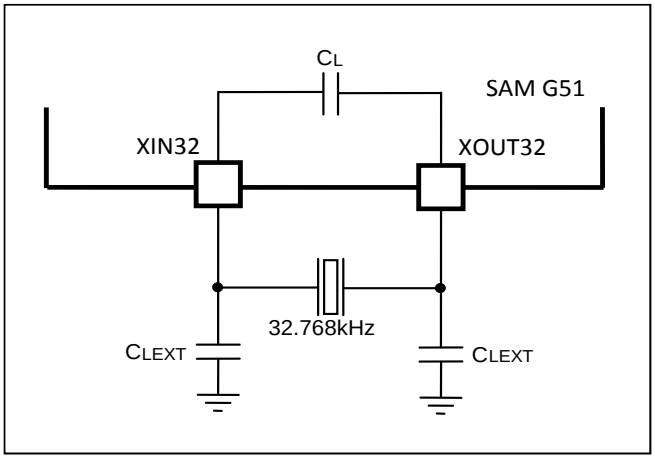
Table 1-2. Main Clock, Oscillators Checklist

☑	Signal name	Recommended pin connection	Description
	PB9/XIN PB8/XOUT **Main Oscillator in Normal Mode**	Crystals between 3 and 20MHz Capacitors on XIN and XOUT (crystal load capacitance dependent) 1kΩ resistor on XOUT only required for crystals with frequencies lower than 8MHz.	Internal Equivalent Load Capacitance (C_L = 12.5pF to 17.5pF): Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate. The external load capacitance is calculated with the following formula: $C_{LEXT}=2\ (C_{crystal}-C_L-C_{PCB})$ Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM G5x Series Datasheet. **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**
	PB9/XIN PB8/XOUT **Main Oscillator in Bypass Mode**	PB9/XIN: external clock source PB8/XOUT: can be left unconnected or used as GPIO.	1.7V to 2.0V Square wave signal (V_{DDIO}) External Clock Source up to 50MHz Duty Cycle: 40 to 60% **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**
	8/16/24MHz **Fast Internal RC Oscillator**	PB9/XIN and PB8/XOUT: can be left unconnected or used as GPIO	Powered up by V_{DDIO} The output frequency is configurable through the PMC registers. The Fast RC oscillator is calibrated in production. The frequency can be trimmed by software. Duty Cycle: 40 to 60% **By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**

1.2.2 32kHz Clock/oscillators

Figure 1-3 shows a standard 32kHz Crystal hardware implementation.

Figure 1-3. 32kHz Crystal Schematic Example



The following checklist (Table 1-3) must be followed in order to ensure correct hardware configuration for 32kHz Clock/oscillator.

Table 1-3. 32kHz Clock, Oscillators Checklist

☑	Signal name	Recommended pin connection	Description
	PA7/XIN32 PA8/XOUT32 **32kHz Crystal used**	32.768kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Internal parasitic capacitance C_{para}=0.7pF Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate. C_{LEXT}max=17pF C_{LEXT}= 2x($C_{crystal}$-C_{para}- C_{pcb}) Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM G5x Series Datasheet. **By default at start-up the chip runs out of the embedded 32kHz RC oscillator**
	PA7/XIN32 PA8/XOUT32 **32kHz Oscillator in bypass mode**	PA7/XIN32: external clock source PA8/XOUT32: can be left unconnected or use as GPIO.	1.7V to 2.0V Square wave signal (V_{DDIO}) External Clock Source up to 44kHz Duty Cycle: 40 to 60% **By default at start-up the chip runs out of the embedded 32kHz RC oscillator**

1.3 Serial Wire and JTAG

Figure 1-4, Figure 1-5, Figure 1-6, and Figure 1-7 shows a standard JTAG/SWD hardware implementation with 10-pin Cortex®-M connector and 20-pin connector. It is recommended to establish accessibility to a JTAG/SWD connector for debug in any case.

Figure 1-4. JTAG Schematic Example: 10-pin Cortex-M Connector

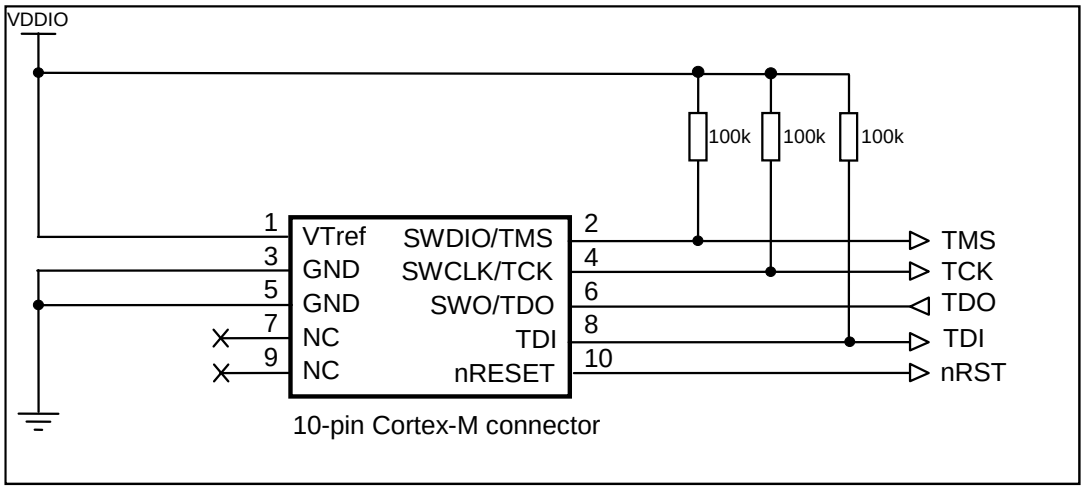


Figure 1-5. JTAG Schematic Example: JTAG 20-pin Connector

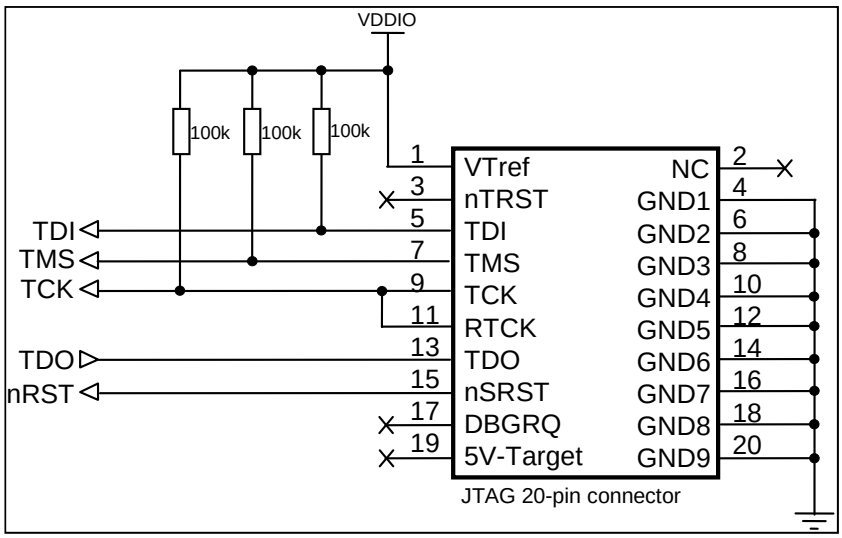


Figure 1-6. SWD Schematic Example: 10-pin Cortex-M Connector

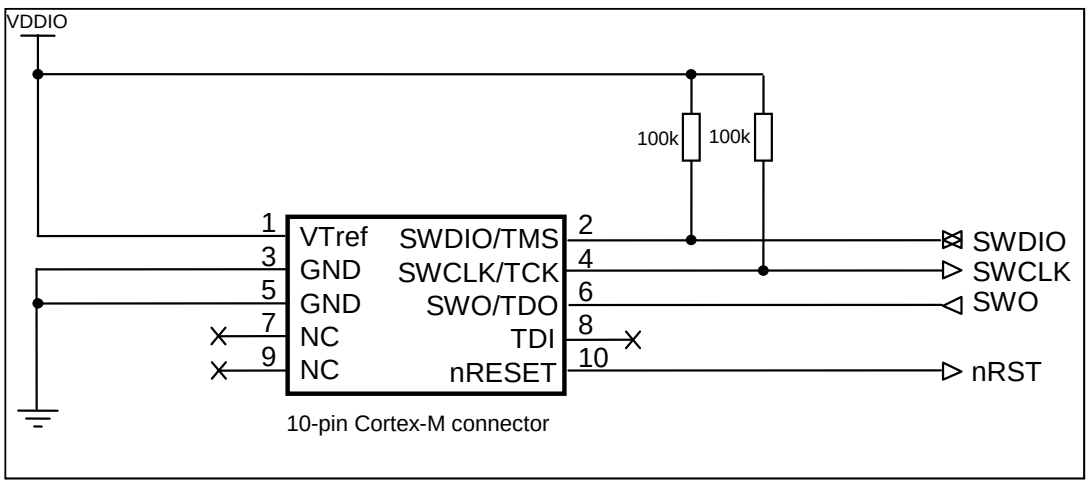
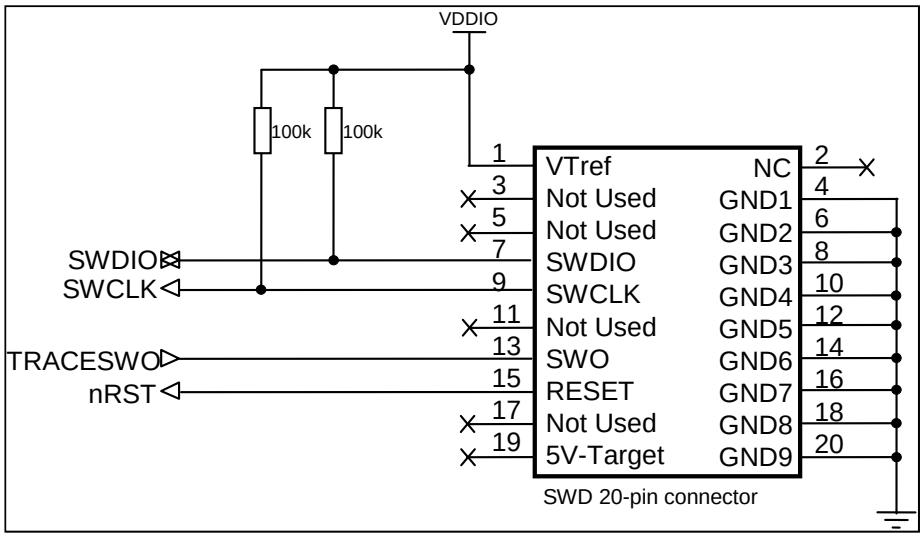


Figure 1-7. SWD Schematic Example: SWD 20-pin Connector



The following checklist (Table 1-4) must be followed in order to ensure correct hardware configuration for JTAG/SWD.

Table 1-4. Serial Wire and JTAG Checklist

☑	Signal name	Recommended pin connection	Description
	TCK/SWCLK/PB7	Application dependent If debug mode is not required this pin can be use as GPIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TMS/SWDIO/PB6	Application dependent If debug mode is not required this pin can be use as GPIO	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDI/PB4	Application dependent If debug mode is not required this pin can be use as GPIO	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDO/TRACESWO/PB5	Application dependent If debug mode is not required this pin can be use as GPIO	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	JTAGSEL	Application dependent. Must be tied to V_{DDIO} to enter JTAG Boundary Scan. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent Internal pull-down resistor (15kΩ)

1.4 Flash Memory

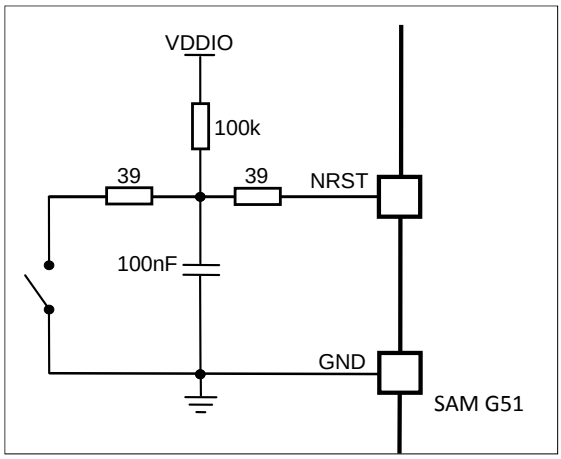
☑	Signal name	Recommended pin connection	Description
	ERASE/PB12	Application dependent. If hardware erase is not required this pin can be use as GPIO	Internal pull-down resistor (100kΩ). Must be tied to V_{DDIO} to erase the General Purpose NVM bits (GPNVMx), the whole Flash content, and the security bit. Reset state: Erase Input, with a 100kΩ Internal pull down and Schmitt trigger enabled

Note: The minimum erase pin assertion for erase effectiveness is 200ms.

1.5 Reset and Test Pins

Figure 1-8, shows a standard Reset hardware implementation.

Figure 1-8. Reset Hardware Implementation



☑	Signal name	Recommended pin connection	Description
	NRST	Application dependent. Can be connected to a push button for hardware reset.	By default, the NRST pin is configured as an input Permanent internal pull-up resistor to V_{DDIO}.
	TST	TST pin can be left unconnected in normal mode. To enter in FFPI mode TST pin must be tied to V_{DDIO}. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent internal pull-down resistor (15kΩ).

1.6 PIOs

☑	Signal name	Recommended pin connection	Description
	PAx - PBx	Application dependent (Pulled-up on V_{DDIO})	At reset, all PIOs are in I/O or System I/O mode with Schmitt trigger inputs and internal pull-up enabled. To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled.

2 Suggested Reading

2.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. It also contains the electrical specifications and expected characteristics of the device.

The datasheet is available on http://www.atmel.com/ in the Datasheets section of the product page.

2.2 Xplained Pro User Guide

The SAM G51 Xplained PRO user guide contains schematics that can be used as a starting point when designing with the SAM G51 devices. This user guide is available on http://www.atmel.com/ in the documents section of the SAM G51 Xplained Pro.

2.3 ARM Documentation on Cortex-M4 Core

- Cortex-M4 Devices Generic User Guide for revision r0p1
- Cortex-M4 Technical Reference Manual for revision r0p1

These documents are available at http://www.arm.com/ in the info center section.

3 Revision History

Doc Rev.	Date	Comments
42311B	11/2015	Figure 1-1 has been updated. Main supply voltage has been corrected to 1.7V – 2.0V.
42311A	5/2014	Initial document release.

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**