AT91SAM7X and AT91SAM7XC Microcontroller Series Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM7X and AT91SAM7XC families of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM7X or AT91SAM7XC Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontroller

Application Note

6260C–ATARM–18-Dec-07

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM7X and AT91SAM7XC Series Microcontrollers on Atmel's Web site.

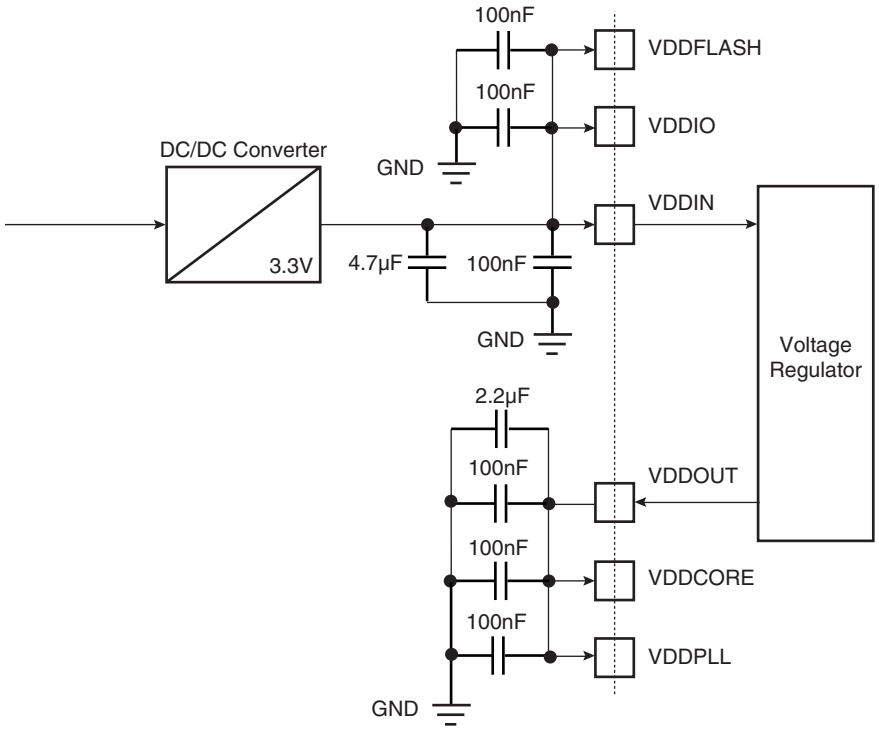
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM7X Series Product Datasheet AT91SAM7XC Series Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI® Datasheet
Evaluation Kit User Guide	AT91SAM7X-EK Evaluation Board User Guide for AT91SAM7X and AT91SAM7XC

3. Schematic Check List

3.3V Single Power Supply Strategy (On-chip Voltage Regulator Used)
To reduce power consumption, voltage regulator can be put in standby mode.

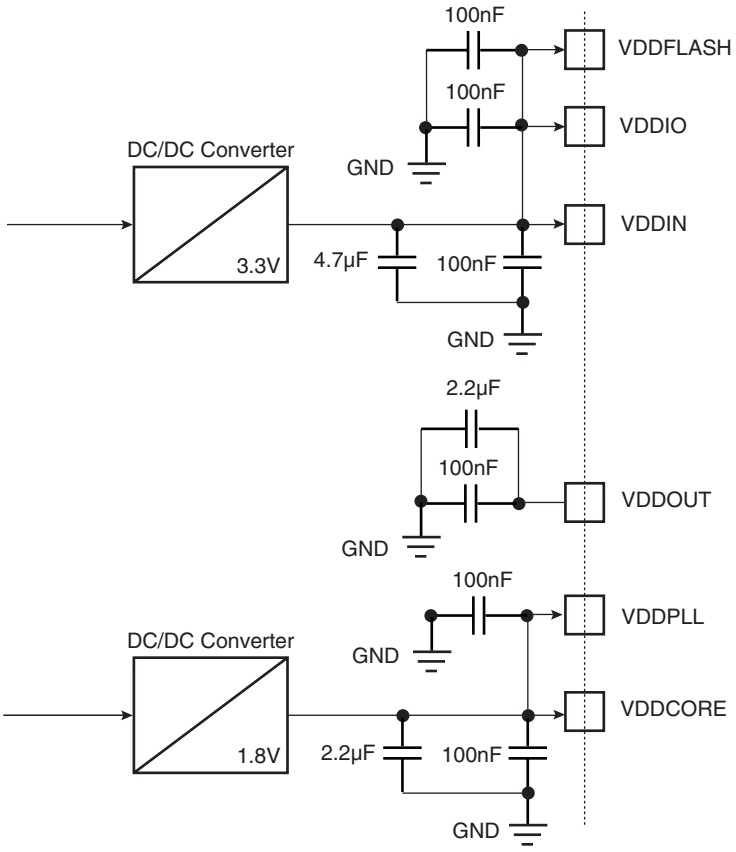


3.3V Single Power Supply Schematic Example:(1)
On-chip Voltage regulator is used - Power Supply on VDDIO: 3.3V

☑	Signal Name	Pin Connection	Description
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)(1)(2)	Powers on-chip voltage regulator and ADC. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **$V_{VDDIN\ SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)(1)(2)	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to guarantee 1.8V stability
	VDDIO	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers I/O lines.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)(1)(2)	Powers Flash (charge pump) and USB transceivers.

☑	Signal Name	Pin Connection	Description
	VDDCORE	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF)[1][2]	Powers device and flash logic, on-chip RC.
	VDDPLL	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

3.3V and 1.8V Dual Power Supply Strategy (On-chip Voltage Regulator NOT Used and ADC Used)
To reduce power consumption, voltage regulator can be put in standby mode.

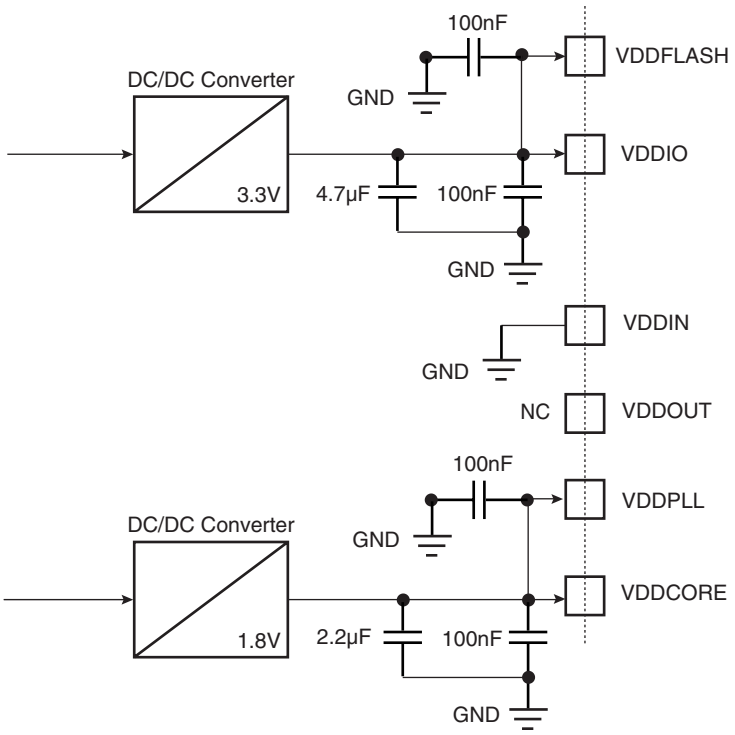


3.3V and 1.8V Dual Power Supply Schematic Example:[1]
On-chip Voltage regulator is not used - ADC is used - Power Supply on VDDIO: 3.3V

☑	Signal Name	Pin Connection	Description
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	Powers ADC. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to prevent on-chip voltage regulator oscillations.
	VDDIO	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers I/O lines.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers Flash (charge pump) and USB transceivers. **$V_{VDDFLASH}$ must always be superior or equal to $V_{VDDCORE}$.**

☑	Signal Name	Pin Connection	Description
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Powers device logic, on-chip RC and Flash. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **$V_{VDDCORE\ SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.**
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

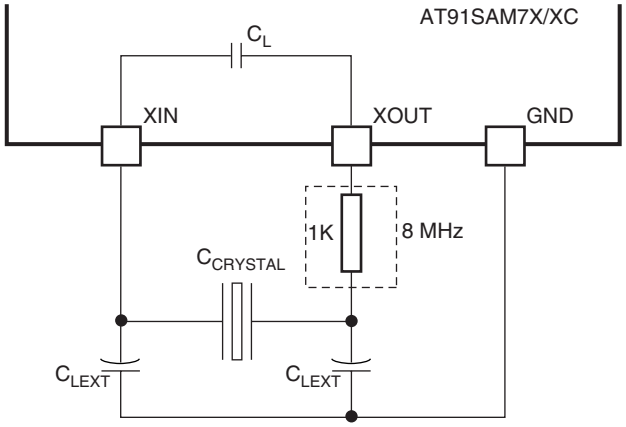
3.3V and 1.8V Dual Power Supply Strategy (On-chip Voltage Regulator and ADC NOT Used)

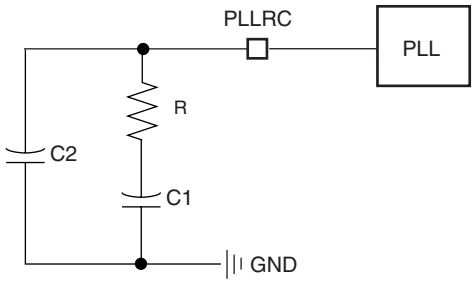


3.3V and 1.8V Dual Power Supply Schematic Example:[(1)]
On-chip Voltage regulator is not used - ADC is not used - Power Supply on VDDIO: 3.3V

☑	Signal Name	Pin Connection	Description
	VDDIN	Connected to GND.	-
	VDDOUT	Can be left unconnected.	-
	VDDIO	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7µF)[(1)(2)]	Powers I/O lines. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF)[(1)(2)]	Powers Flash (charge pump) and USB transceivers. **$V_{VDDFLASH}$ must always be superior or equal to $V_{VDDCORE}$.**

☑	Signal Name	Pin Connection	Description
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Powers device logic, on-chip RC and Flash. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **$V_{VDDCORE\ SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.**
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF)[1][2]	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

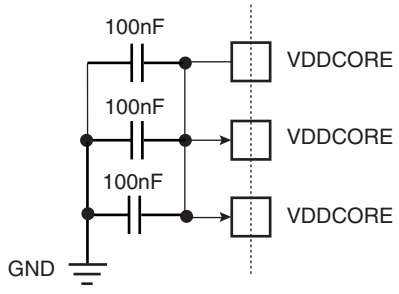
☑	Signal Name	Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Internal Equivalent Load Capacitance (C_L): C_L = 20 pF Crystal Load Capacitance to check ($C_{CRYSTAL}$).  Example: for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 20 pF, no external capacitors (C_{LEXT}) are required ($C_{CRYSTAL} = C_L$) Refer to the electrical specifications of AT91SAM7X or AT91SAM7XC Series Product Datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected.	1.8V Square wave signal (VDDPLL) External Clock Source up to 50 MHz Duty Cycle: 40 to 60%

☑	Signal Name	Pin Connection	Description
	PLLRC	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: “ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  R, C1 and C2 must be placed as close as possible to the pins.

☑	Signal Name	Pin Connection	Description
		ICE and JTAG[3]	
	TCK	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TD0	Floating	-
	JTAGSEL	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDIO} to enter JTAG Boundary Scan. Internal pull-down resistor (15 kOhm).
		Flash Memory	
	ERASE	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	Must be tied to V_{VDDIO} to erase the General Purpose NVM bits (GPNVMx), the whole flash content and the security bit (SECURITY). Internal pull-down resistor (15 kOhm). This pin is debounced by the RC oscillator to improve the glitch tolerance. Minimum debouncing time is 200 ms.
		Reset/Test	
	NRST	Can be left unconnected.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIO} (10 kOhm) is available for User Reset and External Reset control.
[5]	TST	**In harsh environments[4], It is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).**	IMust be tied to V_{VDDIO} to enter Fast Flash Programming (FFPI) mode.[5] Internal pull-down resistor (15 kOhm).

☑	Signal Name	Pin Connection	Description
PIO			
	PAx - PBx	Application Dependant	All PIOs are pulled-up inputs at reset and are 5V tolerant. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
ADC			
	ADVREF	2.6V to V_{VDDIN} Decoupling capacitor(s)	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used: connect ADVREF to GND.
	AD0 to AD7	0V to V_{ADVREF}	AD0 to AD3 are digital pulled-up inputs at reset. AD4 to AD7 are pure analog inputs. To reduce power consumption, if ADC is not used: connect AD4, AD5, AD6 and AD7 to GND.
USB Device (UDP) **To reduce power consumption, USB Device Built-in Transceivers can be disabled (enabled by default).**			
	DDP	Application Dependant(6) Typically, 1.5 kOhm resistor to $V_{VDDFLASH}$	No internal pull-up/pull-down resistors. To reduce power consumption, if USB Device is not used: connect DDP to $V_{VDDFLASH}$.
	DDM	Application Dependant(6)	No internal pull-down resistor. To reduce power consumption, if USB Device is not used: connect DDM to GND.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
5. See: Test Pin description in I/O Lines Considerations section of the corresponding AT91SAM7X or AT91SAM7XC product datasheet for more details on the different conditions to enter FFPI mode.
6. Example of USB Device connection:
   As there is no embedded pull-up, an external circuitry can be added to enable and disable the pull-up.
   To prevent over consumption when the host is disconnected, an external pull-down can be added to DDP and DDM.

A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM7X or AT91SAM7XC product datasheet.

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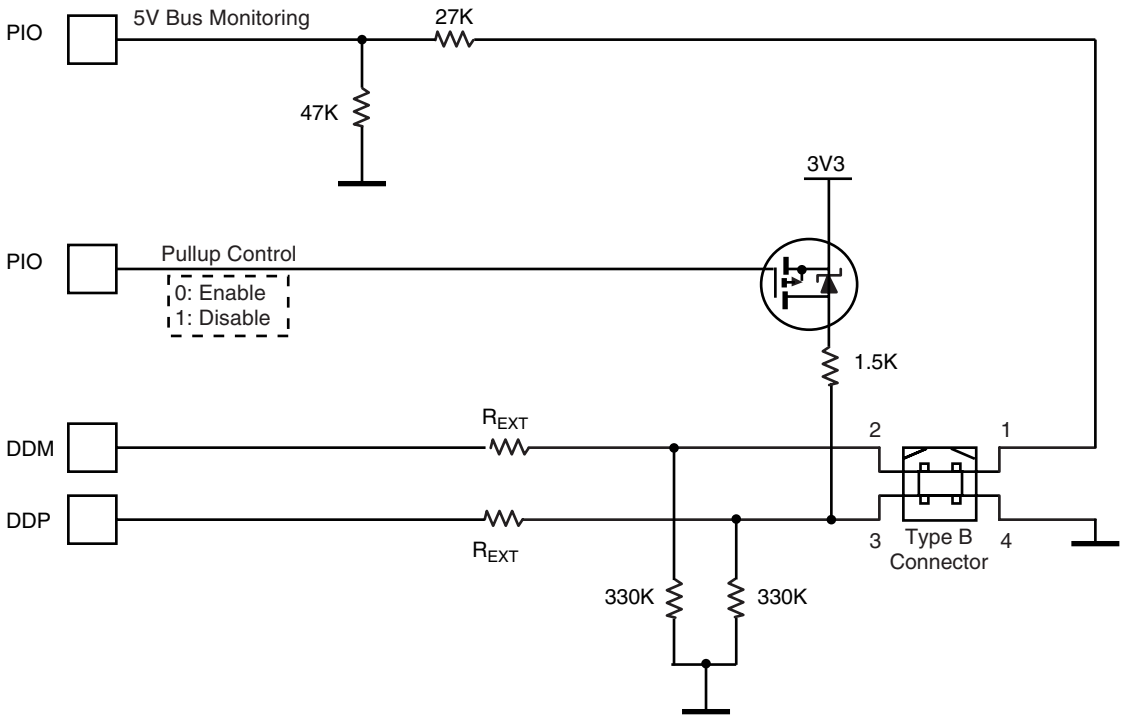

4. AT91SAM Boot Program Hardware Constraints

See the AT91SAM Boot Program section of the corresponding AT91SAM7X or AT91SAM7XC datasheet for more details on the boot program.

4.1 SAM-BA Boot

The SAM-BA™ Boot Assistant supports serial communication via the DBGU or the USB Device Port:

- DBGU Hardware Requirements: 3 to 20 MHz crystal or 1 to 50 MHz external clock.
- USB Device Hardware Requirements:
  - 18.432 MHz crystal.
  - 1.5 kOhm Pull-up on DDP to $V_{VDDFLASH}$.

Revision History

Doc. Rev	Comments	Change Request Ref.
6260A	First issue	
6260B	Section 3. "Schematic Check List" , Precisions added to schematics of power supply strategies. Note added for use in harsh environments. Precisions added to ADC and descriptions. "Clock, Oscillator and PLL" on page 9, schematic updated.	3293
6260C	Updated Recommended Pin Connection for "JTAGSEL", "ERASE", "TST"	5072

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

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