AT91SAM7X and AT91SAM7XC Microcontroller Series Schematic Check List

AMEL

AT91 ARM Thumb-based Microcontroller

Application Note

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM7X and AT91SAM7XC families of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM7X or AT91SAM7XC Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.





2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM7X and AT91SAM7XC Series Microcontrollers on Atmel's Web site.

Table 2-1 gives the associated documentation needed to support full understanding of this application note.

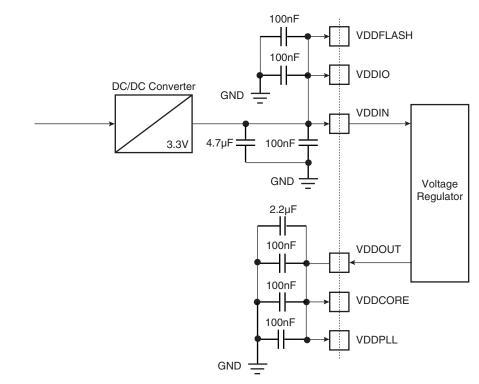
Table 2-1. Associated Documentation

Information	Document Title
User Manual	
Electrical/Mechanical Characteristics	AT91SAM7X Series Product Datasheet
Ordering Information	AT91SAM7XC Series Product Datasheet
Errata	
Internal architecture of processor	
ARM/Thumb instruction sets	ARM7TDMI® Datasheet
Embedded in-circuit-emulator	
Evaluation Kit User Guide	AT91SAM7X-EK Evaluation Board User Guide for AT91SAM7X and AT91SAM7XC

3. Schematic Check List

3.3V Single Power Supply Strategy (On-chip Voltage Regulator Used)

To reduce power consumption, voltage regulator can be put in standby mode.



3.3V Single Power Supply Schematic Example:⁽¹⁾
On-chip Voltage regulator is used - Power Supply on VDDIO: 3.3V

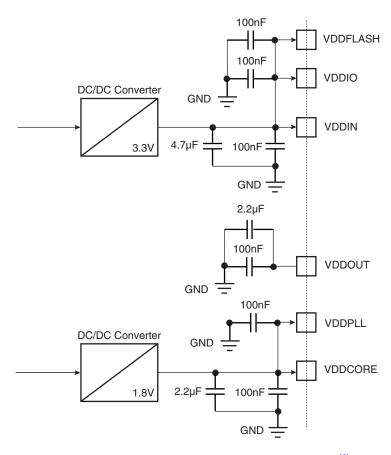
Ø	Signal Name	Pin Connection	Description
			Powers on-chip voltage regulator and ADC.
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 μ F) ⁽¹⁾⁽²⁾	Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
			$V_{VDDIN SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 μF) ⁽¹⁾⁽²⁾	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to guarantee 1.8V stability
	VDDIO	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers I/O lines.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers Flash (charge pump) and USB transceivers.





Ø	Signal Name	Pin Connection	Description
	VDDCORE	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers device and flash logic, on-chip RC.
	VDDPLL	1.65 to 1.95V Can be connected directly to VDDOUT pin Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

3.3V and 1.8V Dual Power Supply Strategy (On-chip Voltage Regulator NOT Used and ADC Used) To reduce power consumption, voltage regulator can be put in standby mode.



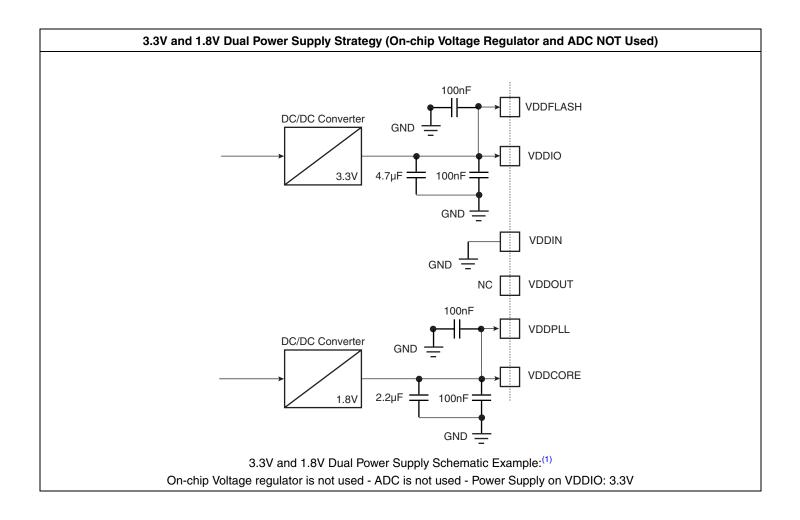
3.3V and 1.8V Dual Power Supply Schematic Example:⁽¹⁾
On-chip Voltage regulator is not used - ADC is used - Power Supply on VDDIO: 3.3V

\square	Signal Name	Pin Connection	Description
	VDDIN	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF) ⁽¹⁾⁽²⁾	Powers ADC. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 μF) ⁽¹⁾⁽²⁾	Output of the on-chip 1.8V voltage regulator. Decoupling/Filtering capacitors must be added to prevent on-chip voltage regulator oscillations.
	VDDIO	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers I/O lines.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers Flash (charge pump) and USB transceivers. V _{VDDFLASH} must always be superior or equal to V _{VDDCORE} .





\square	Signal Name	Pin Connection	Description
			Powers device logic, on-chip RC and Flash.
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF) ⁽¹⁾⁽²⁾	Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
			$V_{VDDCORE\ SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.



$\overline{\mathbf{A}}$	Signal Name	Pin Connection	Description
	VDDIN	Connected to GND.	-
	VDDOUT	Can be left unconnected.	-
	VDDIO	3.0V to 3.6V Decoupling/Filtering capacitors	Powers I/O lines.
		$(100 \text{ nF and } 4.7 \mu\text{F})^{(1)(2)}$	Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDFLASH	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers Flash (charge pump) and USB transceivers. V _{VDDFLASH} must always be superior or equal to V _{VDDCORE} .



\square	Signal Name	Pin Connection	Description
			Powers device logic, on-chip RC and Flash.
	VDDCORE	1.65 to 1.95V Decoupling/Filtering capacitors (100 nF and 2.2 µF) ⁽¹⁾⁽²⁾	Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
			$V_{VDDCORE\ SLOPE}$ (T_{SLOPE}) must be superior or equal to 6V/ms.
	VDDPLL	1.65 to 1.95V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the main oscillator and the PLL.
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

Ø	Signal Name	Pin Connection	Description
		Clock, Oscillator a	nd PLL
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependant) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Internal Equivalent Load Capacitance (C_L): $C_L = 20 \text{ pF}$ $Crystal \text{ Load Capacitance to check (} C_{CRYSTAL}).$ $AT91SAM7X/XC$ C_L XIN $C_{CRYSTAL}$ IK $C_{CRYSTAL}$ IK IK $Example: for an 18.432 \text{ MHz crystal with a load capacitance of } C_{CRYSTAL} = 20 \text{ pF, no external capacitors} $ $(C_{LEXT}) \text{ are required (} C_{CRYSTAL} = C_L)$ $Refer to the electrical specifications of AT91SAM7XC Series Product Datasheet.}$
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected.	1.8V Square wave signal (VDDPLL) External Clock Source up to 50 MHz Duty Cycle: 40 to 60%





Ø	Signal Name	Pin Connection	Description
			See the Excel spreadsheet: "ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip" (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.
	PLLRC	Second-order filter Can be left unconnected if PLL not used.	PLLRC PLL R C2 C1 GND
			R, C1 and C2 must be placed as close as possible to the pins.

Application Note

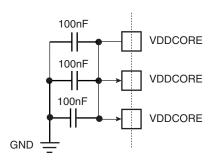
V	Signal Name	Pin Connection	Description	
	ICE and JTAG ⁽³⁾			
	TCK	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.	
	TMS	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.	
	TDI	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.	
	TD0	Floating	-	
	JTAGSEL	In harsh environments ⁽⁴⁾ , It is strongly recommended to tie this pin to GND if not used or to add an external low-	Must be tied to V _{VDDIO} to enter JTAG Boundary Scan.	
		value resistor (such as 1 kOhm).	Internal pull-down resistor (15 kOhm).	
	T	Flash Memor	у	
		In harsh environments ⁽⁴⁾ , It is strongly	Must be tied to V_{VDDIO} to erase the General Purpose NVM bits (GPNVMx), the whole flash content and the security bit (SECURITY).	
	ERASE	recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 kOhm).	Internal pull-down resistor (15 kOhm).	
		value recietor (euch de 1 kemin).	This pin is debounced by the RC oscillator to improve the glitch tolerance.	
			Minimum debouncing time is 200 ms.	
		Reset/Test		
			NRST is configured as an output at power up.	
	NRST	Can be left unconnected.	NRST is controlled by the Reset Controller (RSTC).	
			An internal pull-up resistor to V_{VDDIO} (10 kOhm) is available for User Reset and External Reset control.	
(5)	TST	In harsh environments ⁽⁴⁾ , It is strongly recommended to tie this pin to GND if not used or to add an external low-	IMust be tied to V _{VDDIO} to enter Fast Flash Programming (FFPI) mode. ⁽⁵⁾	
		value resistor (such as 1 kOhm).	Internal pull-down resistor (15 kOhm).	





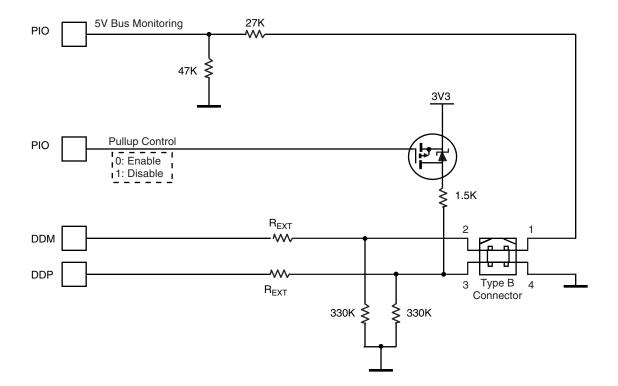
V	Signal Name	Pin Connection	Description
		PIO	
	PAx - PBx	Application Dependant	All PIOs are pulled-up inputs at reset and are 5V tolerant. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
		ADC	
		2.6V to V _{VDDIN}	ADVREF is a pure analog input.
	ADVREF	Decoupling capacitor(s)	To reduce power consumption, if ADC is not used: connect ADVREF to GND.
			AD0 to AD3 are digital pulled-up inputs at reset. AD4 to AD7 are pure analog inputs.
	AD0 to AD7	0V to V _{ADVREF}	
			To reduce power consumption, if ADC is not used: connect AD4, AD5, AD6 and AD7 to GND.
		USB Device (UI	DP)
	To reduce power	er consumption, USB Device Built-in Trans	sceivers can be disabled (enabled by default).
	DDD	Application Dependant ⁽⁶⁾	No internal pull-up/pull-down resistors.
	DDP	Typically, 1.5 kOhm resistor to V _{VDDFLASH}	To reduce power consumption, if USB Device is not used: connect DDP to V_{VDDFLASH} .
			No internal pull-down resistor.
	DDM	Application Dependant ⁽⁶⁾	To reduce power consumption, if USB Device is not used: connect DDM to GND.

- Notes: 1. These values are given only as a typical example.
 - 2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



- 3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
- 4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
- 5. See: Test Pin description in I/O Lines Considerations section of the corresponding AT91SAM7XC product datasheet for more details on the different conditions to enter FFPI mode.
- 6. Example of USB Device connection: As there is no embedded pull-up, an external circuitry can be added to enable and disable the pull-up. To prevent over consumption when the host is disconnected, an external pull-down can be added to DDP and DDM.

A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM7XC product datasheet.





4. AT91SAM Boot Program Hardware Constraints

See the AT91SAM Boot Program section of the corresponding AT91SAM7X or AT91SAM7XC datasheet for more details on the boot program.

4.1 SAM-BA Boot

The SAM-BA[™] Boot Assistant supports serial communication via the DBGU or the USB Device Port:

- DBGU Hardware Requirements: 3 to 20 MHz crystal or 1 to 50 MHz external clock.
- USB Device Hardware Requirements:
 - 18.432 MHz crystal.
 - 1.5 kOhm Pull-up on DDP to $V_{VDDFLASH.}$

Revision History

Doc. Rev	Comments	Change Request Ref.
6260A	First issue	
6260B	Section 3. "Schematic Check List", Precisions added to schematics of power supply strategies. Note added for use in harsh environments. Precisions added to ADC and descriptions. "Clock, Oscillator and PLL" on page 9, schematic updated.	3293
6260C	Updated Recommended Pin Connection for "JTAGSEL", "ERASE", "TST"	5072





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