KSZ8041RNL

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8041RNL. These checklist items should be followed when utilizing the KSZ8041RNL in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 11. Detailed information on these subjects can be found in the corresponding section:

- General Considerations on page 1
- Power on page 1
- Ethernet Signals on page 3
- Clock Circuit on page 6
- Digital Interfaces on page 8
- Startup on page 9
- Miscellaneous on page 10

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

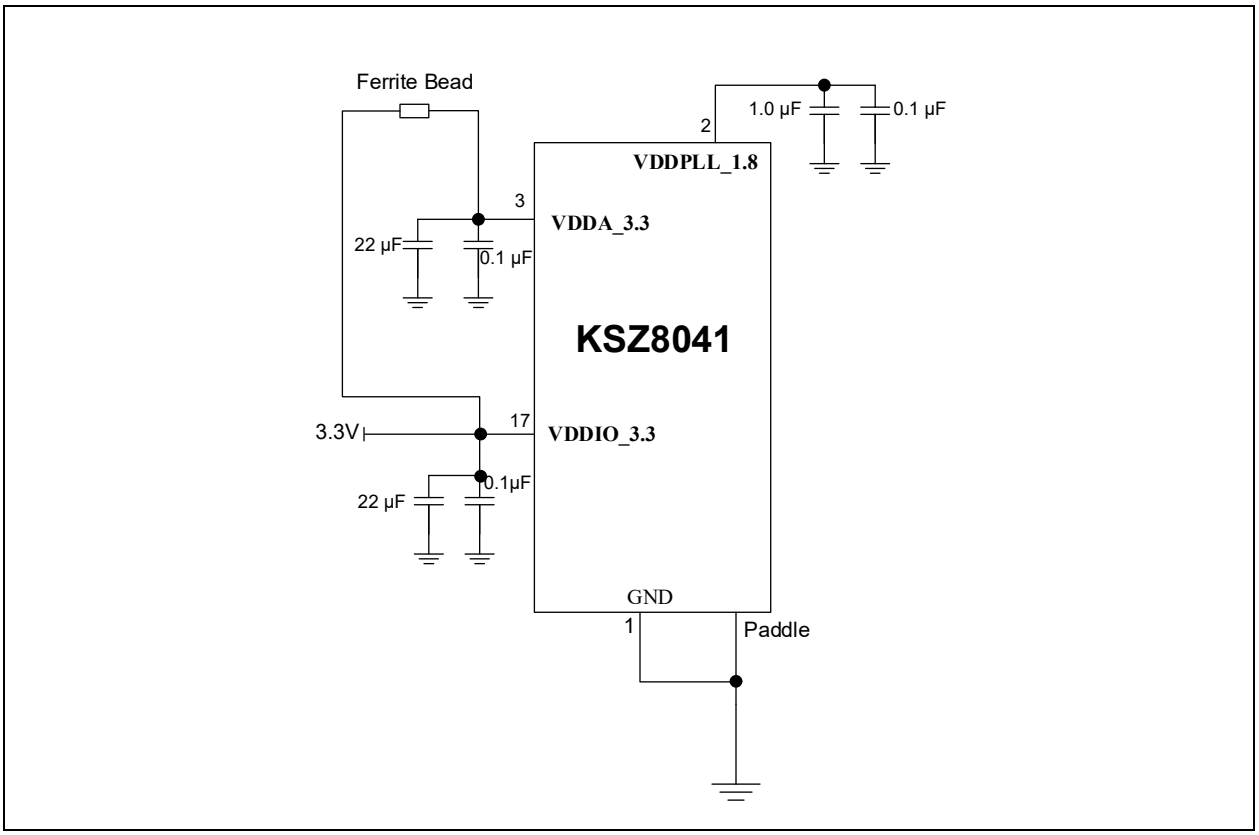
- The ground pin, **GND**, should be connected to the solid ground plane on the board. The KSZ8041RNL has a paddle ground on the bottom side of the chip which must be connected directly to a solid, contiguous digital ground plane.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- The analog supply (**VDDA_3.3**) is located on pin 3, and requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used.
- The **VDDA_3.3** pin should include 0.1 µF and 22 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pin 17 (**VDDIO_3.3**) should be connected to the board's +3.3V supply.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



VDDPLL_1.8 (pin 2) is used to provide bypassing for the on-chip +1.8V core regulator. This pin requires a 0.1 µF bypass capacitor. This capacitor should be located as close as possible to the pin without using vias.

In addition, pin 2 requires a bulk capacitor placed as close as possible to the pin. The bulk capacitor should have a value from 1.0 µF to 2.2 µF, and have an Equivalent Series Resistance (ESR) of no more than 1.0Ω. Microchip recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances, and characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

4.0 ETHERNET SIGNALS

4.1 PHY Interface

- **TX+** (pin 7): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 µF capacitor is required on this pin.
- **TX-** (pin 6): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 µF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to Figure 4-1.
- **RX+** (pin 5): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 µF capacitor is required on this pin.
- **RX-** (pin 4): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 µF capacitor is required on this pin.
- For receive channel connection and termination details, refer to Figure 4-2.

FIGURE 4-1: TRANSMIT CHANNEL CONNECTIONS AND TERMINATIONS

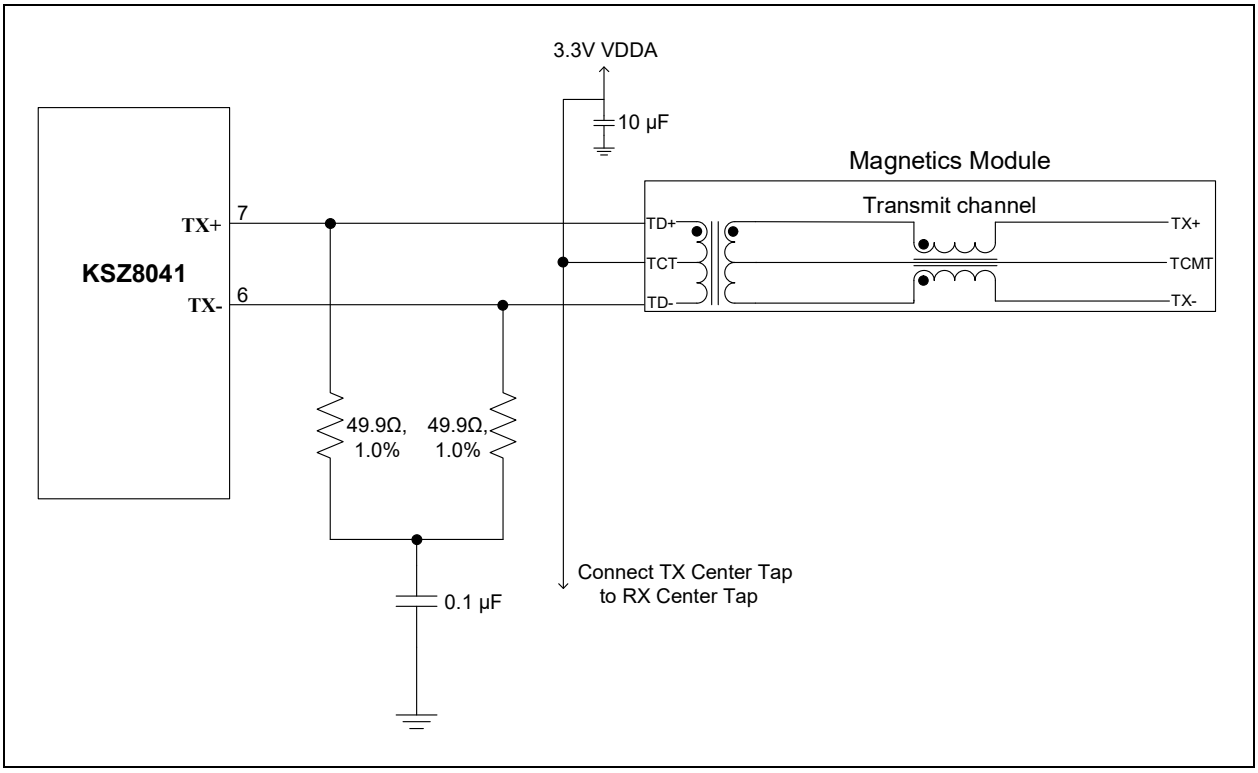
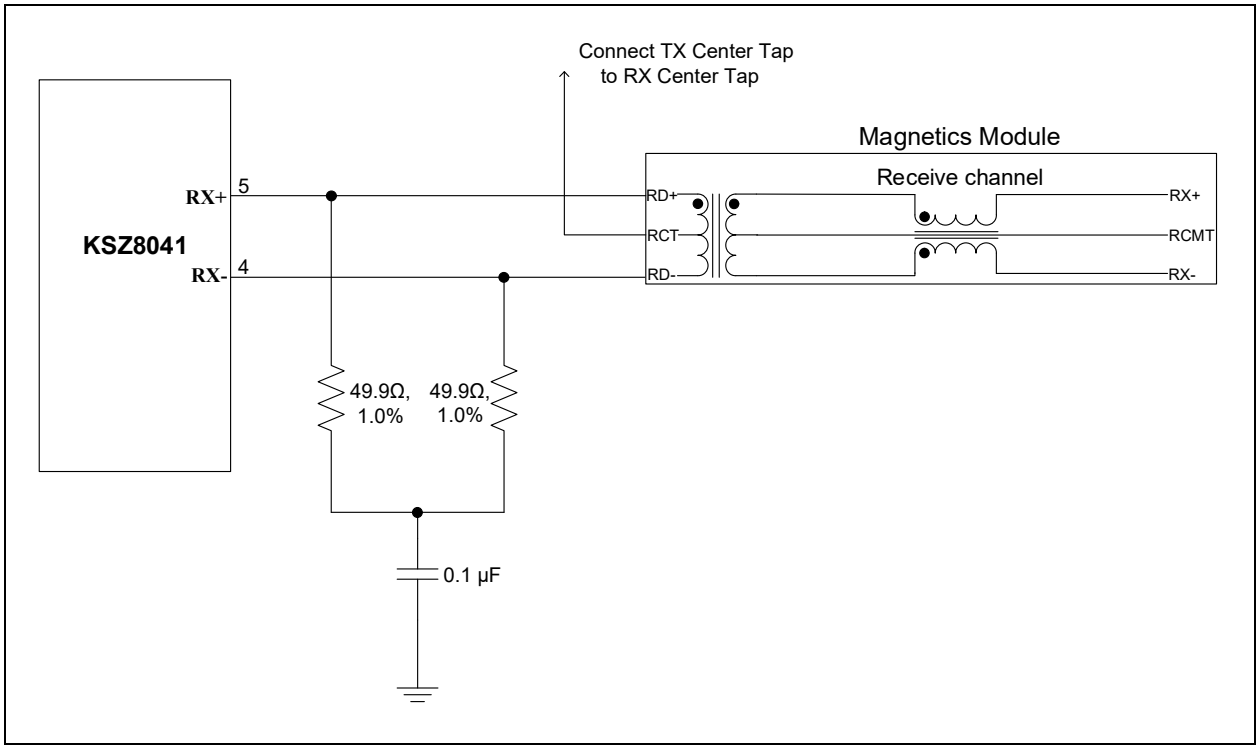


FIGURE 4-2: RECEIVE CHANNEL CONNECTIONS AND TERMINATIONS



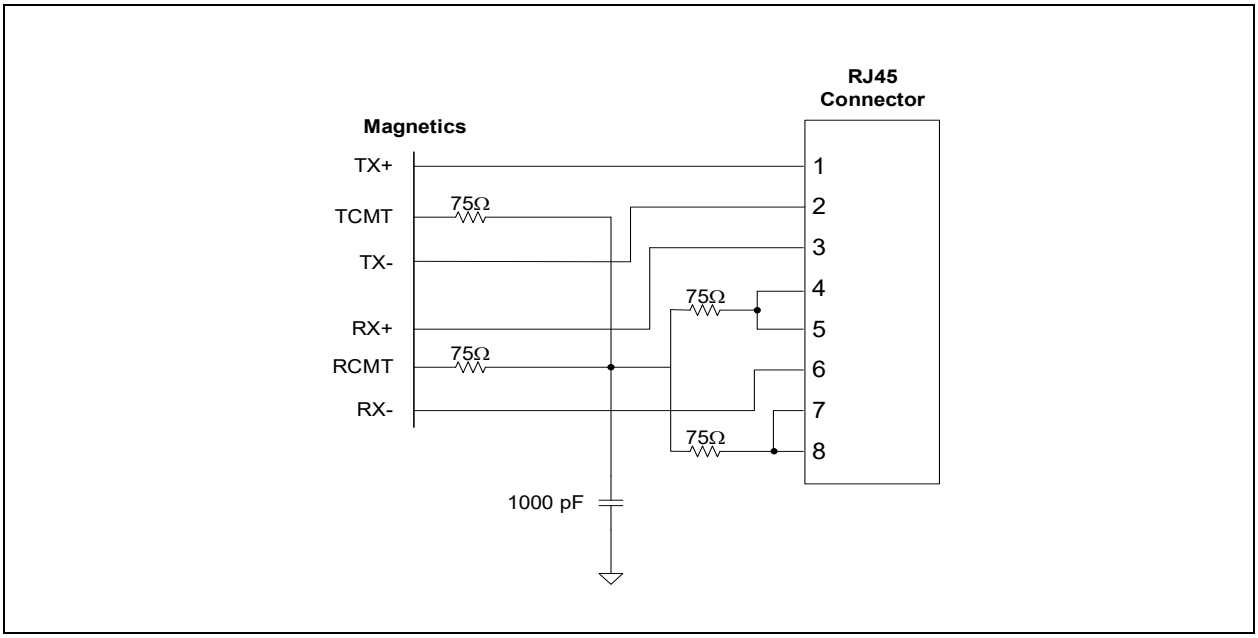
4.2 Magnetics Connection

- The center tap connection on the KSZ8041RNL side for the transmit channel must be connected to **VDDA** (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics. In addition, a 10 µF capacitor is required from the receive channel center tap of the magnetics to digital ground.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC):
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TX+ (pin 7) of the KSZ8041RNL.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to TX- (pin 6) of the KSZ8041RNL.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to RX+ (pin 5) of the KSZ8041RNL.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to RX- (pin 4) of the KSZ8041RNL.
- When using the KSZ8041RNL device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (TX channels and RX channels are symmetrical with each other) is required.

4.3 RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground.

FIGURE 4-3: RJ45 CONNECTIONS

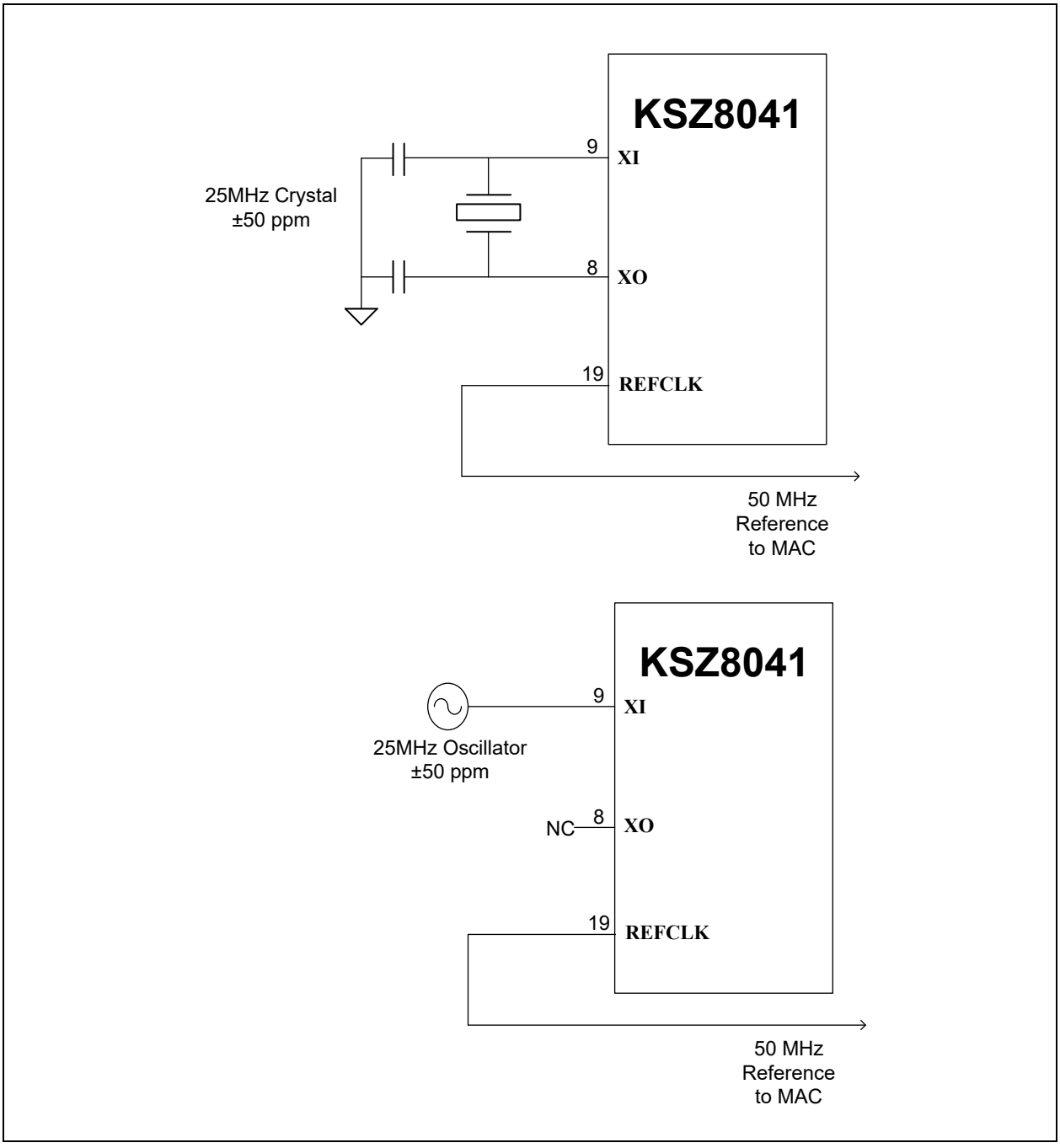


5.0 CLOCK CIRCUIT

5.1 External Clock Connections for RMII Mode

- A 25.000 MHz clock crystal or oscillator is used to provide the clock source for the KSZ8041RNL in RMII mode. For exact specifications and tolerances, refer to the latest revision of the device data sheet. A 50.000 MHz clock signal is output on the REFCLK pin to the MAC.
- **XI** (pin 9) is the clock circuit input. If a crystal is used, connect this pin to one terminal of the crystal.
- **XO** (pin 8) should be left floating as a No Connect (NC) when an oscillator is used. If a crystal is used, connect this pin to the other terminal of the crystal.
- Since every system design is unique, the PCB design, oscillator, and layout all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, stability, and voltage level of the circuit to guarantee it meets all design criteria as presented in the data sheet.

FIGURE 5-1: CLOCK OSCILLATOR CONNECTIONS FOR RMII MODE



Note: KSZ8041RNL supports RMII clock mode (25 MHz mode) only.

6.0 DIGITAL INTERFACES

6.1 RMII Interface

- When using an external RMII MAC interface, Table 6-1 indicates the proper connections for the 10 signals, including two management pins (MDC, MDIO).

TABLE 6-1: RMII CONNECTIONS

From:	Connects to:
KSZ8041RNL	**RMII MAC Device**
REFCLK (pin 19)	REF_CLK
RXD0 (pin 16)	RXD<0>
RXD1 (pin 15)	RXD<1>
CRSDV (pin 18)	CRS_DV
RX_ER (pin 20)	RX_ER
TXD0 (pin 24)	TXD<0>
TXD1 (pin 25)	TXD<1>
TX_EN (pin 23)	TX_EN
MDIO (pin 11)	MDIO
MDC (pin 12)	MDC

- Provisions should be made for the series terminations for all outputs on the RMII interface. Series resistors enable the designer to closely match the output driver impedance of the KSZ8041RNL and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these resistors is 33Ω.
- The series terminations on the REFCLK, RXD0, RXD1, CRSDV, and RXER lines should be placed close to the KSZ8041RNL.
- The series terminations on the TXD0, TXD1, and TX_EN lines should be placed close to the MAC.

6.2 Required External Pull-Ups

- When using the KSZ8041RNL MDC/MDIO management pins, a pull-up resistor of 4.7 kΩ on the **MDIO** signal (pin 11) is required.
- If used, the **INTRP** (pin 21) requires a 4.7 kΩ external pull-up resistor since this output is an open drain. If **INTRP** is not used, the pull-up resistor is not necessary.

7.0 STARTUP

7.1 Reset Circuit

RST# (pin 32) is an active-low reset input. This signal resets all logic and registers within the KSZ8041RNL. A hardware reset (**RST#** assertion) is required following power-up. Please refer to the latest copy of the *KSZ8041RNL Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ8041RNL when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

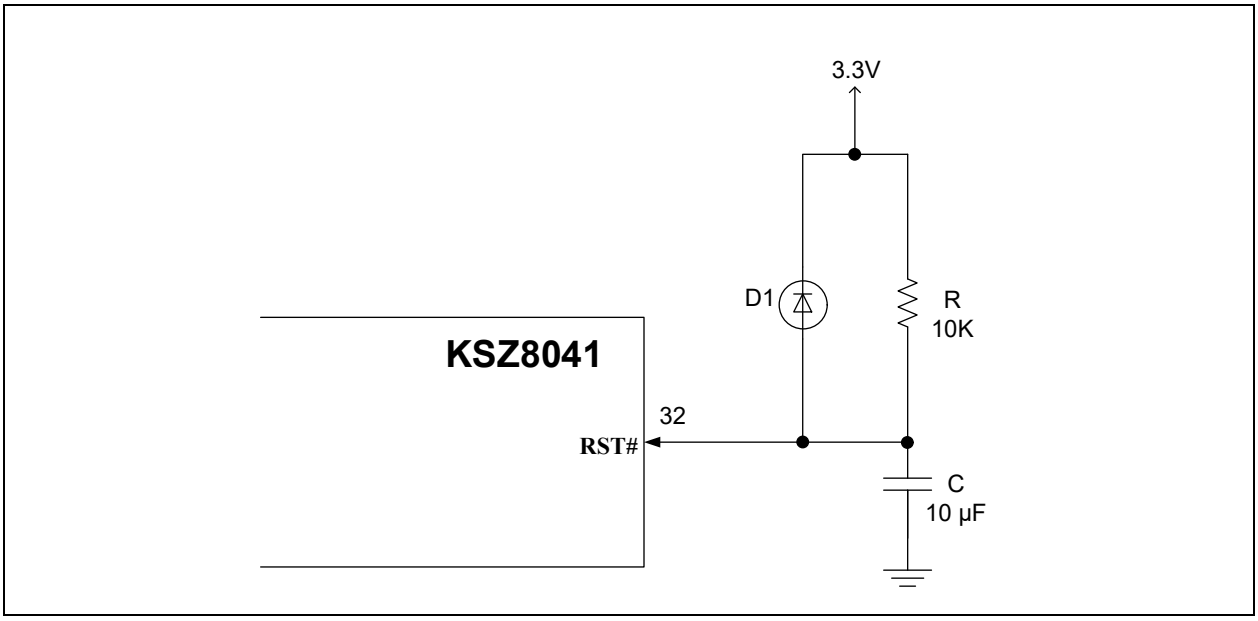
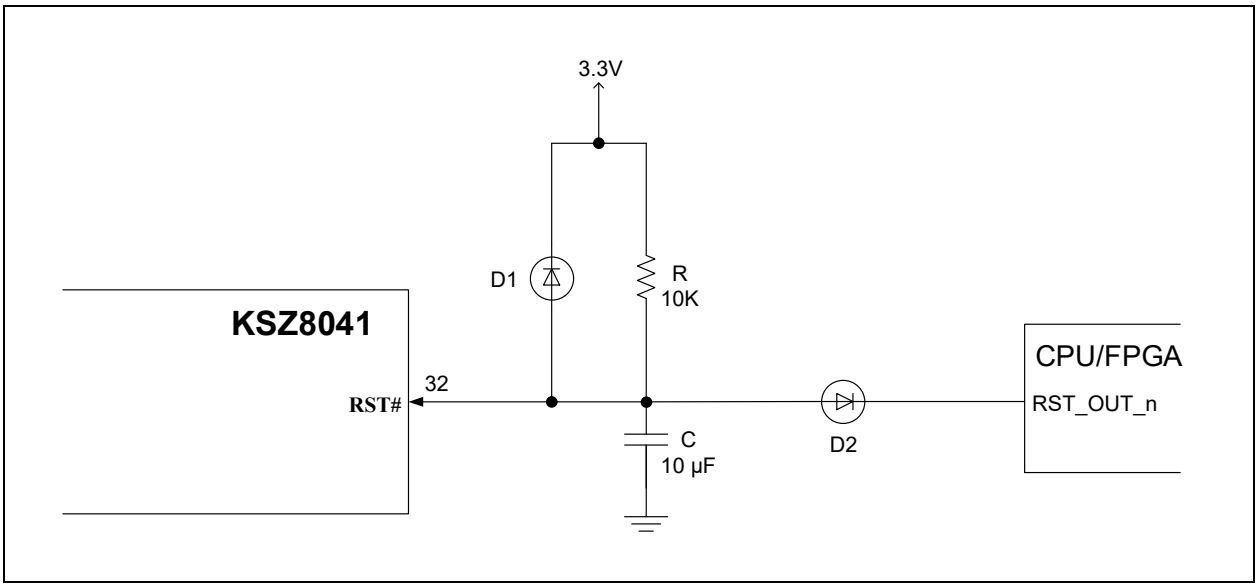


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (RST_OUT_n) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be directly connected.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Strapping Pins

The strapping pins control the configuration, speed, duplex, auto-negotiation, power-down functionality, and PHY address of the KSZ8041RNL. The value of these strapping pins are latched upon power-up and reset. In some systems, the MAC receive input pins may drive high during power-up or reset and consequently cause the PHY strap in pins on the MII/RMII signals to be latched high. In this case (with the exception of speed, duplex, and PHY address bit 0 strapping options), it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to ISOLATE mode or is not configured with an incorrect PHY address. Refer to the *KSZ8041RNL Data Sheet* for complete details for the operation of these pins.

7.3 LED Pins

- The KSZ8041RNL provides two LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220Ω - 470Ω). Refer to the *KSZ8041RNL Data Sheet* for further details on how to connect each pin for correct operation.
- The LED functionality signal pins are shared with the following pin strapping functions:
  - LED0 is shared with **NWAYEN** on pin 30.
  - LED1 is shared with **SPEED** on pin 31.

8.0 MISCELLANEOUS

8.1 REXT Resistor

The **REXT** pin on the KSZ8041RNL should connect to digital ground through a 6.49 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100 Ethernet physical device. A 100 pF capacitor should be connected in parallel with the 6.49 kΩ resistor.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a zero ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7-22 µF) for each power plane.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify pins match the data sheet.		
	Section 2.2, "Ground"	Verify grounds should be tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure **VDDA_3.3** and **VDDIO_3.3** is in the range 3.135V to 3.465V and a 22 µF capacitor is on each pin. • **VDDPLL_1.8** requires a 1.0 µF capacitor.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY Interface"	Verify the termination resistors (49.9Ω, 1.0%) and capacitors (0.1 µF) on the TX and RX pins.		
	Section 4.2, "Magnetics Connection"	Verify the center taps are connected to the **VDDA_3.3** (pin 3) supply on the KSZ8041RNL device side, and are terminated with 75Ω resistors through a 1000 pF, 2 kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.3, "RJ45 Connector"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "External Clock Connections for RMII Mode"	Verify a 25 MHz or 25 MHz ±50 ppm external oscillator is used.		
Section 6.0, "Digital Interfaces"	Section 6.1, "RMII Interface", Section 6.2, "Required External Pull-Ups"	Confirm proper RMII signals between MAC and PHY interface with correct termination resistors (33Ω) and external pull-up for MDIO signal.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2, "Strapping Pins"	In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1 kΩ pull-downs on the PHY strap pins.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "REXT Resistor"	Confirm proper REXT resistor (6.49 kΩ, 1.0%) with a 100 µF capacitor in parallel.		
	Section 8.2, "Other Considerations"	• Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. • Incorporate sufficient power plane bulk capacitors (4.7-22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002702B (09-28-18)	Section 4.2, "Magnetics Connection" and Section 6.1, "RMII Interface"	Updated the sections.
	Section 5.1, "External Clock Connections for RMII Mode"	Added a note under Figure 5-1.
	Section 6.1, "RMII Interface"	Removed the old figure and replaced it with Table 6-1.
DS00002702A (05-09-18)	All	Initial release.

NOTES:

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