PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarifications

PIC16(L)F18455/56

The PIC16(L)F18455/56 devices that you have received conform functionally to the current device data sheet (DS40002038**D**), except for the anomalies described in this document. The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below. The errata described in this document will be addressed in future revisions of the PIC16(L)F18455/56 silicon.

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of the *'Silicon Issue Summary'* table apply to the current silicon revision (A1).

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a. For MPLAB IDE 8, select ***Programmer*** > ***Reconnect***.
   b. For MPLAB X IDE, select ***Window*** > ***Dashboard*** and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A0	A1
PIC16F18455	0x30D7	0x2000	0x2001
PIC16LF18455	0x30D8	0x2000	0x2001
PIC16F18456	0x30D9	0x2000	0x2001
PIC16LF18456	0x30DA	0x2000	0x2001

Note: Refer to the **Device/Revision ID** section in the current *"PIC16(L)F184XX Memory Programming Specification"* (DS40001970) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A0	A1
Analog-to-Digital Converter With Computation (ADC^2)	ADC^2 Burst Average mode	1.1.1	ADC^2 Burst Average mode while in "Non-Continuous Double Sample" mode may not operate as intended.	X	-
	Double Sample Conversion	1.1.2	An unexpected acquisition time is added between the first and second conversions.	X	X
I^{2}C	Start and Stop Interrupt Functions	1.2.1	A race condition can cause the Start and/or Stop flags to be set when I^{2}C is enabled.	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.3.1	Low-Voltage programming is not possible when V_{DD} is below BORV while BOR is enabled.	X	X
NVM	WRERR bit Operation	1.4.1	NVMERR bit is set by device Reset after being cleared by software.	X	-
Program Flash Memory (PFM)	PFM Endurance	1.5.1	The PFM endurance is lower than specified.	X	X
	Back to Back Writes	1.5.2	Repetitive writes may cause write/erase failures.	X	-
Capture/Compare/PWM (CCP)	PWM mode	1.6.1	Duty cycle values are incorrect.	X	-
Signal Measurement Timer (SMT)	Reset Bit	1.7.1	Module stops working if RST is set while prescaler setting is not zero.	X	X
Universal Asynchronous Receiver Transmitter (UART)	Synchronous Mode Transmissions	1.8.1	Loss of second byte written in TXREG.	X	-
	Transmit mode	1.8.2	Double byte transmit.	X	-
Windowed Watchdog Timer	Window Operation	1.9.1	Window feature of the WWDT does not operate correctly in DOZE mode.	X	-

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (ADMD = `0b011` in the ADCON2 register) while enabling noncontinuous operation and double-sampling (ADCONT = `0` in the ADCON0 register and ADDSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around

When operating the ADCC in Burst Average mode with double-sampling, enable continuous module operation (ADCONT = `1` in the ADCON0 register) and set the Stop-on-Interrupt bit (the ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in noncontinuous Burst Average mode can be operated with a single ADC conversion (ADDSEN = `0` in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A0	A1
X	

1.1.2 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = `1`) with no Precharge time (ADPRE = `0`) and no Acquisition time (ADACQ = `0`), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around
Method 1:

Disable Double Sample Conversion (DSEN = `0`) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A0	A1
X	

1.2 Module: Inter-Integrated Circuit (I^2C)

1.2.1 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles (F_{OSC}/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
SSPxCON3bits.SCIE = 0;          // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;          // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;         // Enable I2C
Delay();                        // Wait for 250 ns + 6 instruction cycles (FOSC/4)
PIRxbits.SSPxIF = 0;            // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;          // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;          // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A0	A1
X	X

1.3 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.3.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A0	A1
X	X

1.4 Module: Nonvolatile Memory (NVM)

1.4.1 WRERR Bit Operation

When a Reset is issued while an NVM high voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A0	A1
X	

1.5 Module: Program Flash Memory (PFM)

1.5.1 Endurance of PFM is Lower than Specified

The minimum value for the Program Flash Memory (PFM) endurance specification called out as parameter number MEM30 is 1K cycles.

Work around

None.

Affected Silicon Revisions

A0	A1
X	X

1.5.2 PFM Back to Back Writes

When repetitive writes to non-volatile memory (Program Flash Memory) are performed, it could result in write/erase failures at some locations. The issue is due to latent timing in the non-volatile memory controller which can cause the write instruction to fail under certain conditions.

Work around

To avoid the issue, the customer needs to wait an additional 100 us after the NVMCON1.WR bit has been set, allowing for the last word to be loaded into the latch. This delay is added only when the NVMCON1.LWLO bit is cleared in the software.

```
if(i == (WRITE_FLASH_BLOCKSIZE-1))
        {
            // Start Flash program memory write
            NVMCON1bits.LWLO = 0;
        }
         NVMCON2 = 0x55;
        NVMCON2 = 0xAA;
        NVMCON1bits.WR = 1;
         if (NVMCON1bits.LWLO==0)
        {
        __delay_us(100);
        }
        NOP();
        NOP();

    writeAddr++;
    }
```

Note: The __delay_us() function uses a #define macro definition. For the intrinsic __delay_us() function to work correctly, the value of the _XTAL_FREQ must be clearly defined. This macro is defined in the device_config.h file if the code is generated using MCC. The value of XTAL_FREQ is equal to the system clock frequency.

Affected Silicon Revisions

A0	A1
X	

1.6 Module: Pulse-Width Modulation (PWM)

1.6.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = `0` (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around

None.

Affected Silicon Revisions

A0	A1
X	

1.7 Module: Signal Measurement Timer (SMT)

1.7.1 Reset Bit

If the SMT clock prescaler is set to any value other than `'00'`, setting the RST bit will cause the module to stop working. The RST bit will remain at the value `'1'`, the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work around

Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = `00`).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = `00`.

Affected Silicon Revisions

A0	A1
X	X

1.8 Module: Universal Asynchronous Receiver Transmitter (UART)

1.8.1 Synchronous Mode Transmissions

In synchronous mode, if the TXREG is loaded with a new byte while the EUSART is shifting out the 8th bit of the previous byte, then only one bit of the new byte is shifted out. After this bit is shifted out, the transmission stops and the data is lost. If using 9-bit transmission, then this occurs on the 9th bit.

Work around

Write to the TXREG earlier in the transmission or wait for the TXIF flag bit to be set before writing a second byte.

Affected Silicon Revisions

A0	A1
X	

1.8.2 Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

Method 1:

Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2:

Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

Affected Silicon Revisions

A0	A1
X	

1.9 Module: Windowed Watchdog Timer (WWDT)

1.9.1 Window Operation in Doze Mode

When enabling the Windowed operation mode in Doze mode, a window violation error is issued even though the window is open and armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed operation mode in any mode other than Doze. If disabling the Doze mode is not an option, use the WWDT module without enabling the window.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to the Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A0	A1
X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002038**D**):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Thermal Characteristics

In Table **39-6 Thermal Characteristics** of the **Electrical Specifications** chapter, the Thermal Resistance Junction to Ambient (θ_{JA}) and Thermal Resistance Junction to Case (θ_{JC}) are not specified for the 28-pin VQFN (4x4 mm) package type. The table below has been amended to include the missing specifications, and the corresponding parameters (TH01 and TH02) will be updated in the next revision of the datasheet.

Table 2-1.

Standard Operating Conditions (unless otherwise stated) **Operating temperature -40°C ≤ TA ≤ +125°C**					
Param No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	55	°C/W	28-pin SPDIP package
			74	°C/W	28-pin SOIC package
			67.1	°C/W	28-pin SSOP package
			36.2	°C/W	28-pin VQFN 4x4 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	36	°C/W	28-pin SPDIP package
			19	°C/W	28-pin SOIC package
			23.9	°C/W	28-pin SSOP package
			41.9	°C/W	28-pin VQFN 4x4 mm package
TH03	T_{JMAX}	Maximum Junction Temperature	—	°C	$T_{JMAX} = T_{AMAX} + (PD_{MAX} \times \theta_{JA})$(2)
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} x V_{DD}$(1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O}=\Sigma(I_{OL}*V_{OL})+\Sigma(I_{OH}*(V_{DD}-V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX} (T_J-T_A)/\theta_{JA}$(2)

Notes:
1. I_{DD} is current to run the chip alone without driving any load on the output pins.
2. T_A = Ambient Temperature, T_J = Junction Temperature.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
D	03/2024	Added data sheet clarification 2.1.
C	09/2023	Added A1 Silicon Errata Items. Added Silicon Errata issues 1.1.2, 1.2.1, 1.3.1, 1.4.1, 1.5.2, 1.6.1, 1.7.1, 1.8.1 and 1.9.1. Minor format corrections to maintain consistency with the format of other errata documents.
B	11/2020	Updated Electrical Spec. Silicon Issue 1.2.2 and added 1.2.3 silicon issue; Other minor corrections.
A	11/2018	Initial document release.

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