
LAN9252 TX Shift Compensation

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INTRODUCTION

The LAN9252 is a 2/3-port EtherCAT[®] slave controller with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. The LAN9252 supports HP Auto-MDIX, allowing the use of direct connect or cross-over LAN cables. 100BASE-FX is supported via an external fiber transceiver.

The LAN9252 can operate in various modes like Microcontroller, Expansion, or Digital I/O mode. When operated in SPI or Quad SPI mode (Expansion mode), a third networking port can be enabled to provide an additional MII port. This port can be connected to an external PHY, to enable star or tree network topologies, or to another LAN9252 creating a 4-port solution. This port can be configured for the upstream or downstream direction. This manual details about the manual TX shift compensation required in the expansion mode.

This document includes the following topic:

- [TX Shift Compensation on page 2](#)

TX SHIFT COMPENSATION

The EtherCAT Core does not directly use the PHY transmit clock; however, proper timing must be ensured. To aid in this, the EtherCAT Core has the TX shift feature enabled. This feature can delay the generation of the transmit signals from the EtherCAT Core by 0ns, 10ns, 20ns or 30ns. This value can be automatic or manually set using tx_shift_strap [1:0].

Internal PHY TX Shift

For connection to the internal PHYs, automatic TX shift compensation is used. The PHY's TX_CLK is connected and its rising edge detected. The rising edge aligns the phase of the shift counter and when this counter matches the MII_TX_SHIFT input, the MII_TX_ENA and MII_TX_DATA signals are output to the PHY as if they were clocked by the TX_CLK.

External PHY TX Shift

For connection to the external PHY (chip_mode_strap [1:0] set as "10"- 3-port downstream mode or "11"- 3-port upstream mode), manual TX shift compensation is to be used. An external PHY is connected to the MII port and 25 MHz O/P (MII_CLK25) is provided to be used as the reference clock for the PHY. The clock source of Ethernet PHYs and ESC can be the same quartz or separate quartz oscillator. The TXD<3.0>, TXEN from the MII of EtherCAT Slave can be delayed with respect to the CLK25 output by using TX shift compensation. TX_CLK is usually not connected unless automatic TX Shift compensation is used, because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC for TX_CLK phase shift compensation so that they align properly as if they were driven by the PHY's TX_CLK.

Depending upon the timing relationship between the 25 MHz reference clock and the PHYs TX_CLK, a setting of MII_TX_SHIFT is chosen to provide proper setup and hold time to the PHY.

The TX_CLK signals of the PHYs must have a fixed relation to the clock input of the PHYs with a tolerance of ± 5 ns since TX FIFO is not incorporated. During operation the phase relation cannot change since the PHYs and the ESC have to share the same clock source. The phase offset is compensated inside the ESC manually by TX_SHIFT [1:0] - MII Transmit Timing Shift Strap configuration.

TX shift compensation can be achieved by adding delays for MII_TX_ENA/MII_TX_DATA.

Such delays can be added using the TX shift feature and applying MII_TX_SHIFT [1:0].

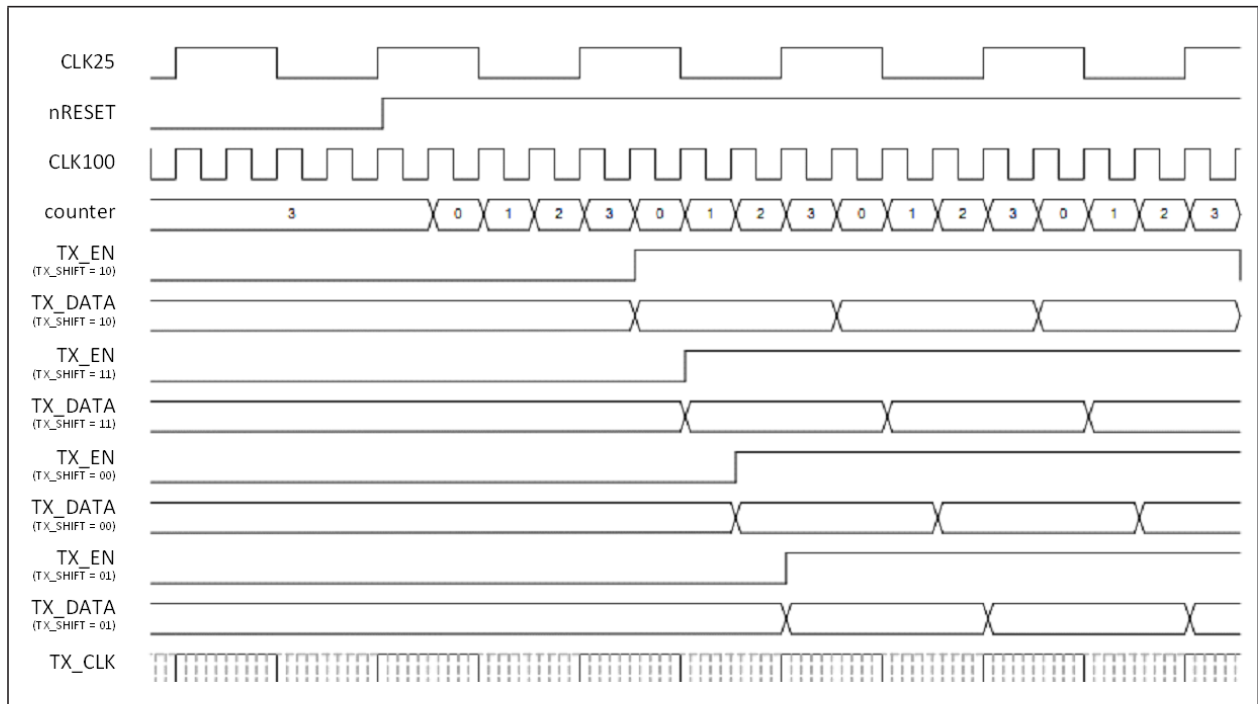
MII_TX_SHIFT [1:0] determine the delay in multiples of 10ns for each port.

TABLE 1: EXTERNAL PHY TX SHIFT

TX_SHIFT1	TX_SHIFT0	MII TX Timing Shift
0	0	20 ns
0	1	30 ns
1	0	00 ns
1	1	10 ns

The timing diagrams in [Figure 1](#) illustrate how the set up and hold times are provided.

FIGURE 1: EXTERNAL PHY TX SHIFT TIMING DIAGRAM



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002008A (08-31-16)	TABLE 1: "External PHY TX Shift"	Corrected table headings: "TX_SHIFT0", "TX_SHIFT1".
	FIGURE 1: "External PHY TX Shift Timing Diagram"	Corrected TX_SHIFT values in figure.
DS00002008A, Sept. 2015	Initial release.	

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