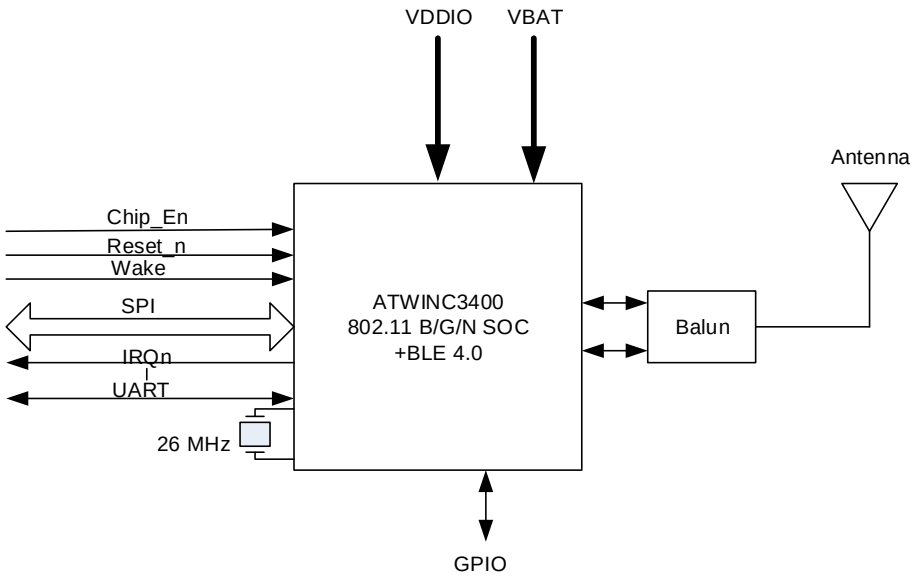
# ATWINC3400

## IEEE 802.11 b/g/n + BLE4.0 Combo SoC for IoT Applications - Hardware Design Guidelines

## USER GUIDE




**Block Diagram**

## Introduction

This document details the hardware design guidelines for a customer to design the ATWINC3400 IC onto their board.

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# 1 Reference Schematic

## 1.1 Schematic

Figure 1-1 shows the reference schematic for a system using the ATWINC3400. Note that there are several 0Ω resistors (R1-R12) shown in series with signals to the chip. These are place holders in case filtering of these lines is necessary due to high frequency in band (2.4GHz) noise on these lines, which can get into the RF path and degrade receiver sensitivity. If the signals coming from the host MCU are noise free, then these placeholders are not required and can be removed.

**Figure 1-1. Reference Schematic**

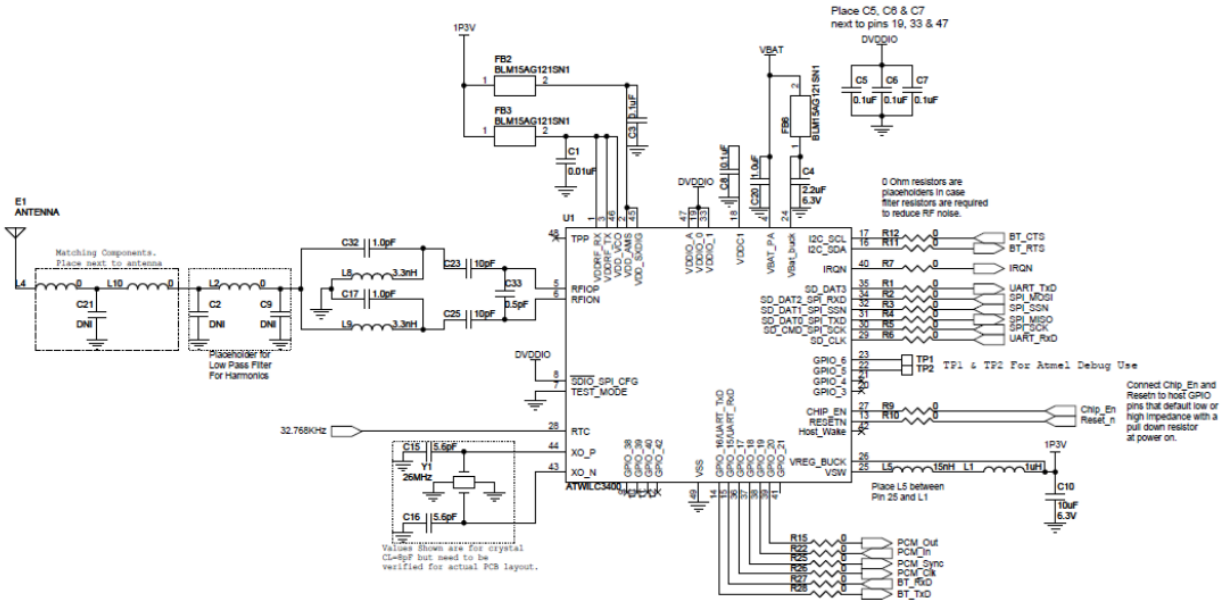



**Figure 1-2. Bill of Materials**

Atmel WiFi Combo Chip Revised: June 25, 2015
ATWINC3400 Revision: 1.0

Bill Of Materials

| Item | Qty | Reference | Value | Description | Manufacturer | Part Number | Footprint |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 0.01uF | CAP,CER,0.01uF,20%,X5R,0402,6.3V | Panasonic | ECJ-0EB0J103M | 0402 |
| 2 | 2 | C2,C9 | DNI | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125C | Murata | 500RGRM0335C1ER50BA0 | 0201 |
| 3 | 5 | C3,C5,C6,C7,C8 | 0.1uF | CAP,CER,0.1uF,10%,X5R,0402,10V | AVX | 0402ZD104KAT2A | 0402 |
| 4 | 1 | C4 | 2.2uF | CAP,CER,2.2uF,10%,X5R,0402,6.3V | TDK | C1005X5R0J225K | 0402 |
| 5 | 1 | C10 | 10uF | CAP,CER,10uF,10%,X5R,0402,6.3V,-55-85C | TDK | C1005X5R0J106K | 0402 |
| 6 | 2 | C15,C16 | 5.6pF | CAP,CER,5.6pF,0.5pF,NPO,0201,25V,-55-125C | TDK | C0603C0G1E5R6D030BA | 0201 |
| 7 | 2 | C17,C32 | 1.0pF | CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125C | Murata | GRM0335C1E1R0BA01J | 0201 |
| 8 | 1 | C20 | 1.0uF | CAP,CER,1.0uF,20%,X5R,0402,6.3V | Panasonic | ECJ-0EB0J105M | 0402 |
| 9 | 1 | C21 | DNI | CAP,CER,10pF,5%,NPO,0402,50V | Murata | GRM1555C1H100J | 0402 |
| 10 | 2 | C23,C25 | 10pF | CAP,CER,10pF,0.5pF,NPO,0201,25V,-55-125C | TDK | C0603C0G1E100D030BA | 0201 |
| 11 | 1 | C33 | 0.5pF | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125C | Murata | 500RGRM0335C1ER50BA01D0750R5AV4T | 0201 |
| 12 | 1 | E1 | ANTENNA | | | | |
| 13 | 3 | FB2,FB3,FB6 | BLM15AG121SN1 | FERRITE,120 OHM @100MHz,0402 | Murata | BLM15AG121SN1 | 0402 |
| 14 | 1 | L1 | 1uH | POWER INDUCTOR,1uH,20%,940mA,0.125ohms,0603,shielded,-40-85c | Murata | LQM18PN1R0MFRL | 0603 |
| 15 | 1 | L2 | 0 | Inductor,2.0nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C | Taiyo Yuden | HKQ060352N0C-T | 0201 |
| 16 | 2 | L4,L10 | 0 | Inductor,9.1nH,5%,Q=8@100MHz,0402 | Taiyo Yuden | HK10059N1J-T | 0402 |
| 17 | 1 | L5 | 15nH | INDUCTOR,Multilayer,15nH,5%,350mA,Q=8@100MHz,0402 | Murata | LQG15H515NJ02D | 0402 |
| 18 | 2 | L8,L9 | 3.3nH | Inductor,3.3nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C | Taiyo Yuden | HKQ060353N3C-T | 0201 |
| 19 | 17 | R1,R2,R3,R4,R5,R6,R7,R9, R10,R11,R12,R15,R22,R25, R26,R27,R28 | 0 | RESISTOR,Thick Film,0 ohm,0402 | Panasonic | ERJ-2GE0R00X | 0402 |
| 20 | 2 | TP1,TP2 | Non Component | Test Point,Surface Mount,0.030"sq. | | 30X30_SM_TEST_POINT | |
| 21 | 1 | U1 | ATWINC3400 | IC, SOC, WiFi Combo, 48QFN | Atmel | ATWINC3400 | 48QFN |
| 22 | 1 | Y1 | 26MHz | CRYSTAL,26MHz,CL=8pF,20ppm temp.,-40C-85C,ESR=80 max,2.5x2.0mm | Taitien | A10183-X-001-3 | 2.5x2.0mm |

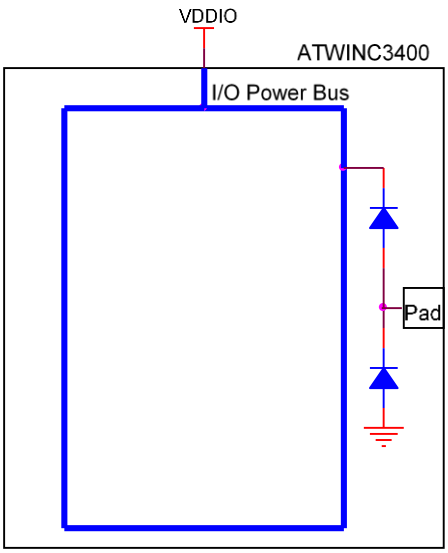
# 2 Notes on Interfacing to the ATWINC3400

## 2.1 Programmable Pull-up Resistors

The ATWINC3400 provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused chip pin on the ATWINC3400 should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC3400 is in the low-power sleep state, current will flow from the VDDIO supply through the pull-up resistors and increase the current consumption of the chip. Since the value of the pull-up resistor is approximately 100kΩ, the current through any pull-up resistor driven low will be VDDIO/100kΩ. For VDDIO = 3.3V, the current through each pull-up resistor driven low would be approximately 3.3V/100kΩ = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

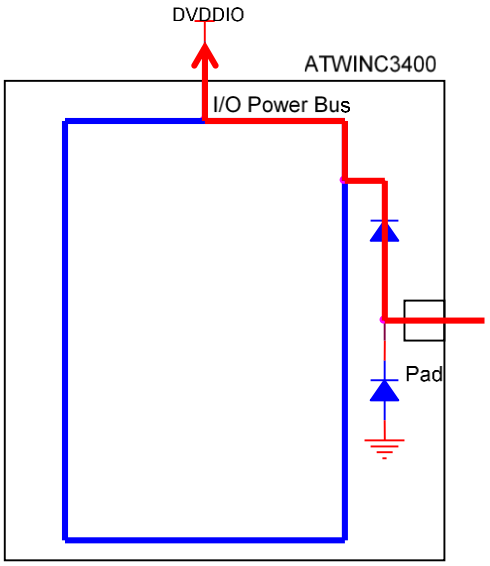
See the ATWINC3400 Programming Guide for information on enabling/disabling the programmable pull-up resistors.

**Figure 2-1. ATWINC3400 Pad ESD Structure**




This shows why it is important that any time Chip_En to the chip is low, all pins interfacing to the chip must not be driven or pulled high. They should either be set to a low level or high impedance state. This means that if any external pull-up resistors are attached to any pins they should be disconnected from the supply when Chip_En is low.

**Figure 2-2. Current Path through ESD Diode**




## 2.2 Restrictions for Power States

When no power is supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

## 2.3 Power-up/down Sequence

The power-up/down sequence for ATWINC3400A is shown in Figure 2-3. The timing parameters are provided in Table 2-1.

**Figure 2-3. Power Up/Down Sequence**

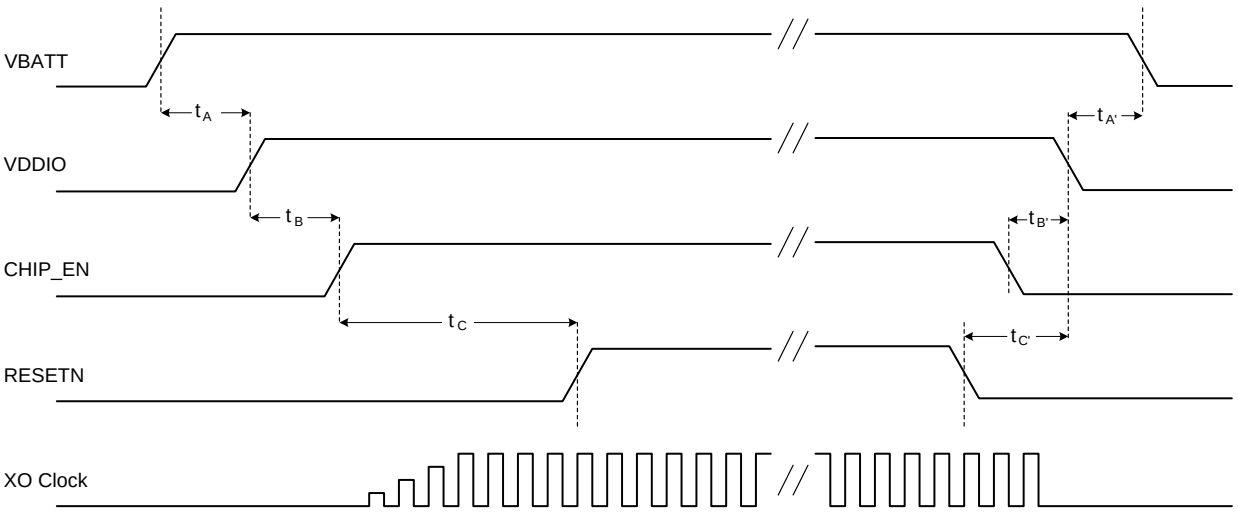


**Table 2-1. Power-up/down Sequence Timing**

| Parameter | Min. | Max. | Unit | Description | Notes |
|---|---|---|---|---|---|
| tA | 0 | | ms | VBATT rise to VDDIO rise | VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT. |
| tB | 0 | | ms | VDDIO rise to CHIP_EN rise | CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating. |
| tC | 5 | | ms | CHIP_EN rise to RESETN rise | This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating. |
| tA' | 0 | | ms | VDDIO fall to VBATT fall | VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO. |
| tB' | 0 | | ms | CHIP_EN fall to VDDIO fall | VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously. |
| tC' | 0 | | ms | RESETN fall to VDDIO fall | VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously. |

## 2.4 Digital I/O Pin Behavior during Power-up Sequences

Table 2-2 represents digital I/O pin states corresponding to device power modes.

**Table 2-2. Digital I/O Pin Behavior in Different Device States**

| Device state | VDDIO | CHIP_EN | RESETN | Output driver | Input driver | Pull-up/down resistor (96kΩ) |
|---|---|---|---|---|---|---|
| Power Down:<br>core supply off | High | Low | Low | Disabled (Hi-Z) | Disabled | Disabled |
| Power-On Reset:<br>core supply on, hard reset on | High | High | Low | Disabled (Hi-Z) | Disabled | Enabled |
| Power-On Default:<br>core supply on, device out of reset but not programmed yet | High | High | High | Disabled (Hi-Z) | Enabled | Enabled |
| On Sleep/<br>On Transmit/<br>On Receive:<br>core supply on, device programmed by firmware | High | High | High | Programmed by firmware for each pin: Enabled or Disabled | Opposite of output driver state | Programmed by firmware for each pin: Enabled or Disabled |

# 3 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4 – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the chip.

## 3.1 Power and Ground

Dedicate one layer as a ground plane. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to insure the lowest possible inductance. The power pins of the ATWINC3400 should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have its own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

## 3.2 RF Traces and Components

The RF traces that go from the ATWINC3400 to the balun must be 50Ω differential controlled impedance. These are pins 5 and 6 of the ATWINC3400. The route from the balun to the antenna connector must be a 50Ω controlled impedance trace. These controlled impedance traces must reference a ground plane on a lower layer. To achieve 50Ω impedance, a typical design might be 20 mil traces referenced to a ground plane on an inner layer which is 10.7 mils below the traces. This must be adjusted depending on the dielectric and copper weight used. No other traces must route through the RF area on layers between the RF traces and the ground reference plane. In fact, try not to route any other traces in the RF area on any layer. This ground reference plane must extend entirely under the tuner.

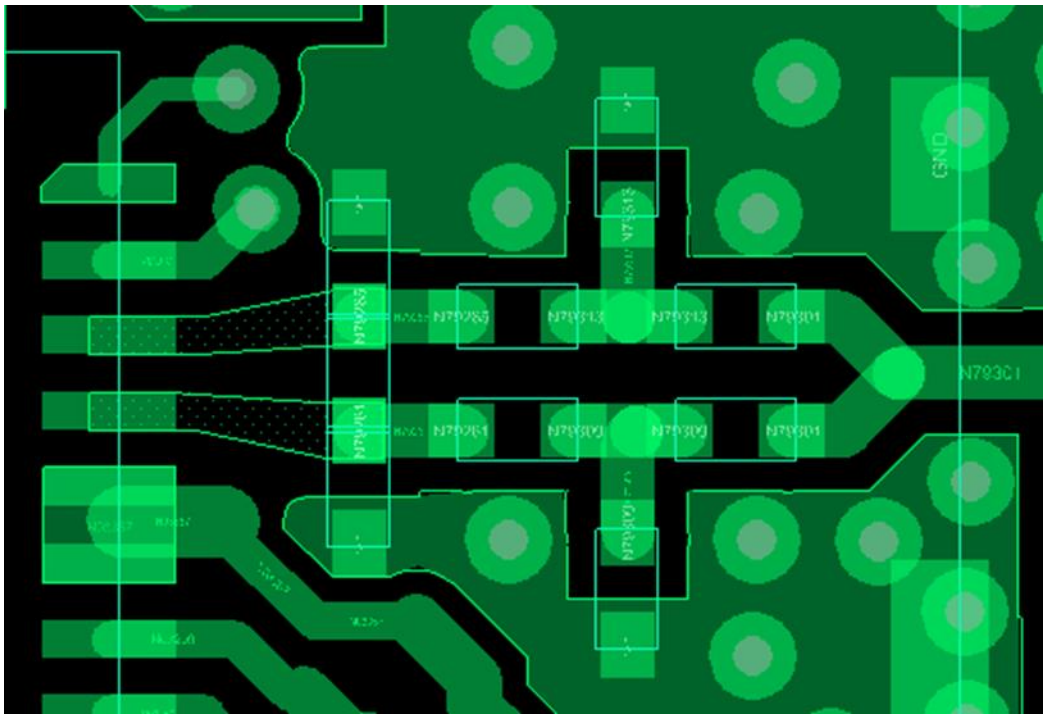
Be sure to add as many ground vias as possible, tying all ground layers together (ground stitching) all along the RF traces and throughout the area where the RF traces are routed. Add at least two ground vias for every ground pad around the RF components. Place ground vias all along the RF traces on either side.

Tie the center ground pad of the ATWINC3400 to the inner ground layer using a grid of nine vias. The ground path going from the ground pad down to the ground plane must be absolutely as low impedance as possible.

Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled in with ground copper.

Be sure to place the matching components and balun as close to the RFIOP and RFION pins as possible (these are named C33, C23, C25, C17, C32, L8, and L9 in the reference schematic). Figure 3-1 shows the placement and routing of these components. Note that they are placed as close as possible to the ATWINC3400's pins 5 and 6. The components used for this design are 0201. Note that the width of the route matches the width of the component pads. This will avoid impedance discontinuities which would occur if there is a large mismatch in trace width versus the component pad size.

**Figure 3-1. Placement and Routing of Balun and Matching Components**




Be sure the route from the antenna to the ATWINC3400 is as short as possible and is completely isolated from all other signals on the board. No signals should route under this trace on any layer of the board. Make sure that all digital signals that may be toggling while the ATWINC3400 active are placed as far away from the antenna as possible. No connectors which have digital signals going to them should be near the antenna. All digital components and switching regulators on the board should be shielded so they do not radiate noise that is picked up by the antenna.

In summary, make sure anything that switches is shielded and kept away from the antenna, the ATWINC3400 or the route from the ATWINC3400 to the antenna.

## 3.3 Sensitive Routes

### 3.3.1 Signals

The following signals are very sensitive to noise and you must take care to keep them as short as possible and keep them isolated from all other signals by routing them far away from other traces or using ground to shield them. Be sure that they are also isolated from noisy traces on the layers above them and below them:

XO_N

XO_P

RFIOP

RFION

### 3.3.2 Supplies

The following power supply pins for the ATWINC3400 are sensitive to noise and care should be taken to isolate the routes to these pins from other noisy signals both on the same layer as the route and on layers above and below. Use ground between these sensitive signals to isolate them from other signals. It is important that the decoupling capacitors for these supplies are placed as close to the ATWINC3400 pin as

possible. This is necessary to reduce the trace inductance between the capacitor and ATWINC3400 power pin to an absolute minimum:

VDDRF_RX (pin 1)

VDDRF_TX (pin 3)

VDD_AMS (pin 2)

VDD_SXDIG (pin 45)

VDD_VCO (pin 46)

Additionally, while the VDDC (pin 18) and VBAT_BUCK (pin 24) supplies are not sensitive to picking up noise, they are noise generating supplies. Therefore, be sure to keep the decoupling capacitors for these supply pins as close as possible to the VDDC and VBAT_BUCK pins and make sure that the routes for these supplies stay far away from sensitive pins and supplies.

## 3.4 Additional Suggestions

Make sure that traces route directly through the pads of all filter capacitors and not by way of a stub route.

The following routes are extremely critical and should be routed first. C) is a power route and should be a heavy copper route. These routes must not have anything above, below, or to the side of them except ground. They must be as short as possible. Make sure that the filter capacitor for these pins is placed right next to the pin.

A. The 50Ω differential pair from ATWINC3400 pins 5 and 6 to the balun. Be sure this route is as short as possible and that both routes of the differential pair are matched in length.
B. The 50Ω unbalanced route from the balun to the antenna.
C. The routes to the XO_P and XO_N pins (pins 43 and 44). These must be isolated with ground above, below, and to the sides of the routes.
D. The route from ATWINC3400 pin 25 (VSW) to the 15nH inductor (L5) must be as short and wide as possible. Make sure this inductor is placed right next to pin 25. The route from the other side of this inductor to the 1.0µH inductor (L1) must also be as short and heavy as possible. Then the route from L1 to the 10µF capacitor (C10) and to pin 26 must also be as short and heavy as possible.
E. The loop created from ATWINC3400 pin 25 through the inductors, the capacitor, and back to pin 26 must be as small as possible.
F. Make sure the ground return path from the 10µF capacitor connected to pin 26 back to the ground pad of the ATWINC3400 is as short and wide as possible. This is critical. The ground return path must have extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATWINC3400 ground pad will result in incorrect operation of the on chip switching regulator.

Be sure to place the power supply decoupling capacitors so that there is a capacitor very close to each power supply pin of the device. This requires making the copper as short and wide as possible – use copper fills for the power supply routing from the pins to the filter capacitors, not narrow traces.

# 4 Interferers

One of the biggest problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also make sure that no traces route underneath the RF portion of the ATWINC3400 and that no traces route underneath any of the RF traces from the antenna to the ATWINC3400 input. This applies to all

layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

# 5 Thermal Considerations

Table 5-1 lists the thermal resistance from junction to ambient ($\Theta_{JA}$) and from junction to case ($\Theta_{JC}$) for 6x6 48L QFN.

**Table 5-1. Thermal Resistance from Junction to Ambient**

| Package | $\Theta_{JA}$ | $\Theta_{JC}$ |
|---|---|---|
| 5x5mm 40L QFN | 29.5ºC/W | 3.7ºC/W |

Junction-to-ambient thermal resistance $\Theta_{JA}$ is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment near the package. The generated heat on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces. $\Theta_{JA}$ reported here assumes the package is mounted on a board with two signal layers and two internal planes (2s2p).

# 6 External Interfaces

## 6.1 General

The Digital Pad Characteristics are given in Table 6-1.

**Table 6-1. Digital Pad Characteristics**

| Symbol | Characteristics | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $VDDIO_L$ (2) | I/O Supply Voltage Low Range | 1.62 | 1.80 | 2.00 | V |
| $VDDIO_M$ (2) | I/O Supply Voltage Mid-Range | 2.00 | 2.50 | 3.00 | V |
| $VDDIO_H$ (2) | I/O Supply Voltage High Range | 3.00 | 3.30 | 3.60 | V |
| VBATT (3) | Battery Supply Voltage | 2.5 (4) | 3.6 | 4.2 | V |
| | Operating Temperature | -40 | | 85 | ºC |

Notes:
1. Refer to the datasheet for details of power connections.
2. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO_0, and VDDIO_1.
3. Battery supply voltage is applied to following pins: VDDBATT_PPA/PA and VBATT_BUCK.
4. Device is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.

**Table 6-2. VDDIO Conditions**

| VDDIO condition | Characteristics | Min. | Max. | Unit |
|---|---|---|---|---|
| $VDDIO_L$ | Input Low Voltage $V_{IL}$ | -0.30 | 0.60 | V |
| | Input High Voltage $V_{IH}$ | VDDIO-0.60 | VDDIO+0.30 | V |
| | Output Low Voltage $V_{OL}$ | | 0.45 | V |
| | Output High Voltage $V_{OH}$ | VDDIO-0.50 | | V |
| | $I^2C$ Pad Drive Strength (1) | 4 | | mA |
| | All other Digital Pad Drive Strength | 2 | | mA |
| $VDDIO_M$ | Input Low Voltage $V_{IL}$ | -0.30 | 0.63 | V |
| | Input High Voltage $V_{IH}$ | VDDIO-0.60 | VDDIO+0.30 | V |
| | Output Low Voltage $V_{OL}$ | | 0.45 | V |
| | Output High Voltage $V_{OH}$ | VDDIO-0.50 | | V |
| | $I^2C$ Pad Drive Strength (1) | 8 | | mA |
| | All other Digital Pad Drive Strength | 4 | | mA |
| $VDDIO_H$ | Input Low Voltage $V_{IL}$ | -0.30 | 0.65 | V |
| | Input High Voltage $V_{IH}$ | VDDIO-0.60 | VDDIO+0.30 (up to 3.60) | V |
| | Output Low Voltage $V_{OL}$ | | 0.45 | V |
| | Output High Voltage $V_{OH}$ | VDDIO-0.50 | | V |
| | $I^2C$ Pad Drive Strength (1) | 12 | | mA |
| | All other Digital Pad Drive Strength | 6 | | mA |
| All | Output Loading | | 20 | pF |

| VDDIO condition | Characteristics | Min. | Max. | Unit |
|---|---|---|---|---|
| All | Digital Input Load | | 6 | pF |

Note: 1. $I^2C$ Pad Drive Strength applies to the following pins: I2C_SDA, I2C_SCL.

## 6.2 SPI Interface

### 6.2.1 Overview

ATWINC3400 has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 6-3. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 8 (SPI_CFG) is tied to VDDIO.

**Table 6-3. SPI Interface Pin Mapping**

| Pin # | SPI Function |
|---|---|
| 8 | CFG: Must be tied to VDDIO for ATWINC3400 |
| 32 | SSN: Active Low Slave Select |
| 34 | MOSI (RXD): Serial Data Receive |
| 30 | SCK: Serial Clock |
| 31 | MISO (TXD): Serial Data Transmit |

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC3400 have internal programmable pull-up resistors. These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWINC3400 is in the low-power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the chip.

### 6.2.2 SPI Timing

The SPI timing is provided in Figure 6-1 and Table 6-4.

**Figure 6-1. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)**

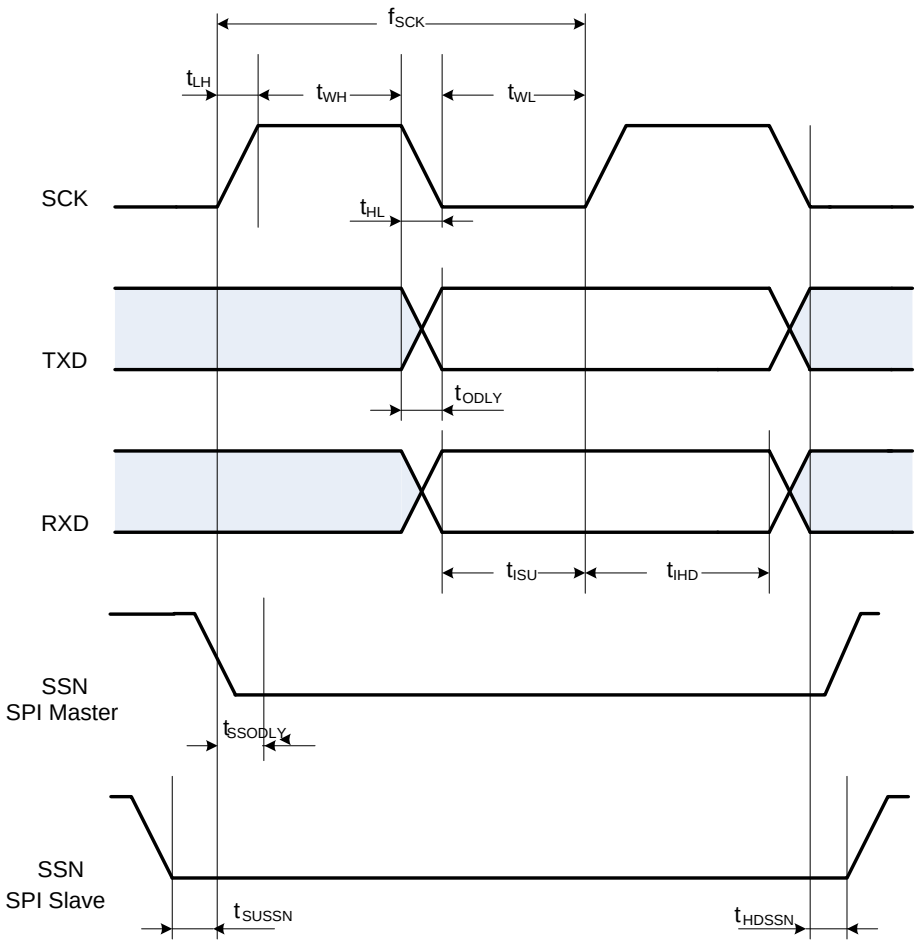



**Table 6-4. SPI Slave Timing Parameters**

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Clock Input Frequency | $f_{SCK}$ | | 48 | MHz | |
| Clock Low Pulse Width | $t_{WL}$ | 5 | | ns | |
| Clock High Pulse Width | $t_{WH}$ | 5 | | ns | |
| Clock Rise Time | $t_{LH}$ | | 5 | ns | |
| Clock Fall Time | $t_{HL}$ | | 5 | ns | |
| Input Setup Time | $t_{ISU}$ | 5 | | ns | |
| Input Hold Time | $t_{IHD}$ | 5 | | ns | |
| Output Delay | $t_{ODLY}$ | 0 | 20 | ns | |
| Slave Select Setup Time | $T_{SUSSN}$ | 5 | | ns | |
| Slave Select Hold Time | $t_{HDSSN}$ | 5 | | ns | |

### 6.2.3 SPI PCB Trace Constraints

In general, the SPI PCB trace layout must ensure that the total capacitance (trace and load of other pin) on the SPI lines (SPI_RXD, SPI_SSN, SPI_TXD, and SPI_SCK) are less than the maximum pin capacitance of 20pF (see Section 6.1). As this is heavily dependent on the board type and lithography, no single constraint of trace length can be given. It is, however, preferable to minimize the trace length as much as possible. For further guidance, consult your Atmel® FAE. Be sure to have all information on the application PCB layout design rules.

## 6.3 UART Interface

The ATWINC3400 has a Universal Asynchronous Receiver/Transmitter (UART) interface available on pins 14 and 15. It can be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where ATWINC3400 operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

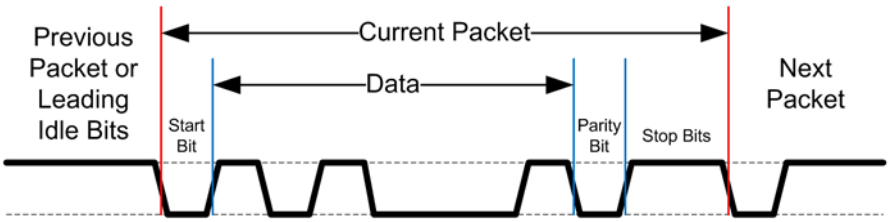
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz / 8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well as the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 6-2. This example shows 7-bit data (0x45), odd parity, and two stop bits.

See the ATWINC3400 Programming Guide for information on configuring the UART.

**Figure 6-2. Example of UART RX or TX Packet**



# 7 Antenna

Make sure to choose an antenna that covers the proper frequency band, 2.400GHz to 2.500GHz. Talk to the antenna vendor and make sure he understands the full frequency range that must be covered by the antenna.

Make sure the antenna is designed for a 50Ω system.

Make sure the PCB pad that the antenna is connected to is properly designed for 50Ω impedance. This is extremely important. The antenna vendor must specify the pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad. Also, since the ground reference plane for the 50Ω trace going from the antenna pad to the ATWINC3400 will probably be on a different layer than the ground reference for the antenna pad, make sure the pad design has a proper transition from the pad to the 50Ω trace.

Make sure that the antenna matching components are placed as close to the antenna pad as possible. The antenna cannot be properly matched if the matching components are far away from the antenna.

# 8 FCC, TELEC, and ETSI Compliance

The reference design provided is compliant with FCC, TELEC, and ETSI regulations. No calibrations are needed by the device maker if the 26MHz crystal used meets the 802.11 requirements (±20ppm). For crystals variations outside this range, consult your Atmel FAE.

# 9 Reference Documentation and Support

## 9.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

Table 9-1 shows a list of documents available on Atmel web or integrated into development tools.

**Table 9-1. Reference Documentation**

| Title | Content |
|---|---|
| Datasheet | |
| Design Files Package | User Guide, Schematic, PCB layout, Gerber, BOM and System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD. |
| Platform Getting started Guide | How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines |
| HW Design Guide | This document |
| SW Design Guide | Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing. |
| SW Programmer guide | Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note |

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/ or contact the nearest Atmel field representative.

# 10 ATMEL EVALUATION BOARD/KIT IMPORTANT NOTICE AND DISCLAIMER

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ATMEL CORPORATION
1600 Technology Drive
San Jose, CA 95110
USA

# 11 Revision History

| Doc Rev. | Date | Comments |
|---|---|---|
| 42564A | 01/2016 | Initial document release. |

**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**