AN3310

Connecting SDR and DDR Memories to SAM9X60

Scope

The SAM9X60 is a high-performance, ultra-low power ARM926EJ-S CPU-based embedded microprocessor (MPU) running up to 600 MHz, with support for multiple memories such as SDRAM, LP-SDRAM, LP-DDR, DDR2, and QSPI and e.MMC Flash. The device integrates powerful peripherals for connectivity and user interface applications, and offers security functions (tamper detection, secure boot program, secure key storage, etc.), TRNG, as well as high-performance crypto accelerators for AES and SHA.

This application note is intended to help the developer design a system based on the SAM9X60 using an external memory by providing examples. Refer to References for board design example files.

Abbreviation List

- SDRAM – Synchronous Dynamic Random-Access Memory
- SDR – Single Data Rate
- DDR – Double Data Rate
- LP – Low Power
- PCB – Printed Circuit Board

References

The following references are available on https://www.microchip.com/wwwproducts/en/SAM9X60.

Type	Name	Literature No.
Data sheet	SAM9X60	DS60001579
Errata	SAM9X60 Device Silicon Errata and Data Sheet Clarification	DS80000846
Application note	SAM9X60 Hardware Design Considerations	DS00003311
Board design example files	SAM9X60 board design example files	–

© 2019 Microchip Technology Inc.

Table of Contents

1. External Bus Interface (EBI) Overview

The External Bus Interface (EBI) is designed to ensure the successful data transfer between several external devices and the embedded SAM9X60 memory controller.

The static memory, MPDDR, SDRAM and ECC controllers are featured external memory controllers on the EBI. These controllers are capable of handling several types of external memory and peripheral devices, such as SRAM, PROM, EPROM, EEPROM, Flash and (DDR2/LP-DDR/SDR/LP-SDR) SDRAM. The EBI operates with 1.8V or 3.3V power supplies (VDDIOM and VDDNF).

Before connecting a memory to the EBI, refer to table “EBI Pins and External Device Connections”, in chapter “External Bus Interface (EBI)” of the SAM9X60 data sheet for the correct connections between the EBI controller pins and the interfaced device pins.

Note: For DDR2, addresses A0, A1 and A12 are not used on the controller side. Addresses A2 to A11 are connected to A0 to A9 on the memory side, signal SDA10 is connected to A10, addresses A13 to A15 are connected to the last three addresses on the memory side and A16 to A18 are connected to BA0 to BA2.

Choose the DDR_CAL value depending on the memory used:

- 20kΩ for LP-SDR, LP-DDR and DDR2 SDRAM types
- 16.9kΩ for SDR SDRAM

Then, connect the DDR_VREF pin to the correct voltage:

- VDDIOM/2 for DDR2 and LP-DDR SDRAM types
- GND for SDR and LP-SDR SDRAM types

For more information, refer to section “DDR/SDR I/O Calibration and DDR Voltage Reference”, in chapter “Memories” of the SAM9X60 data sheet.

2. Hardware Implementation Examples

This section shows hardware design examples implementing all supported memory types.

Extra examples can be found in section “Implementation Examples”, in chapter “External Bus Interface (EBI)” of the SAM9X60 data sheet.

Each subsection features schematics describing how to connect the MPU to the related memory device, the resulting layout and the configuration settings corresponding to each type of memory.

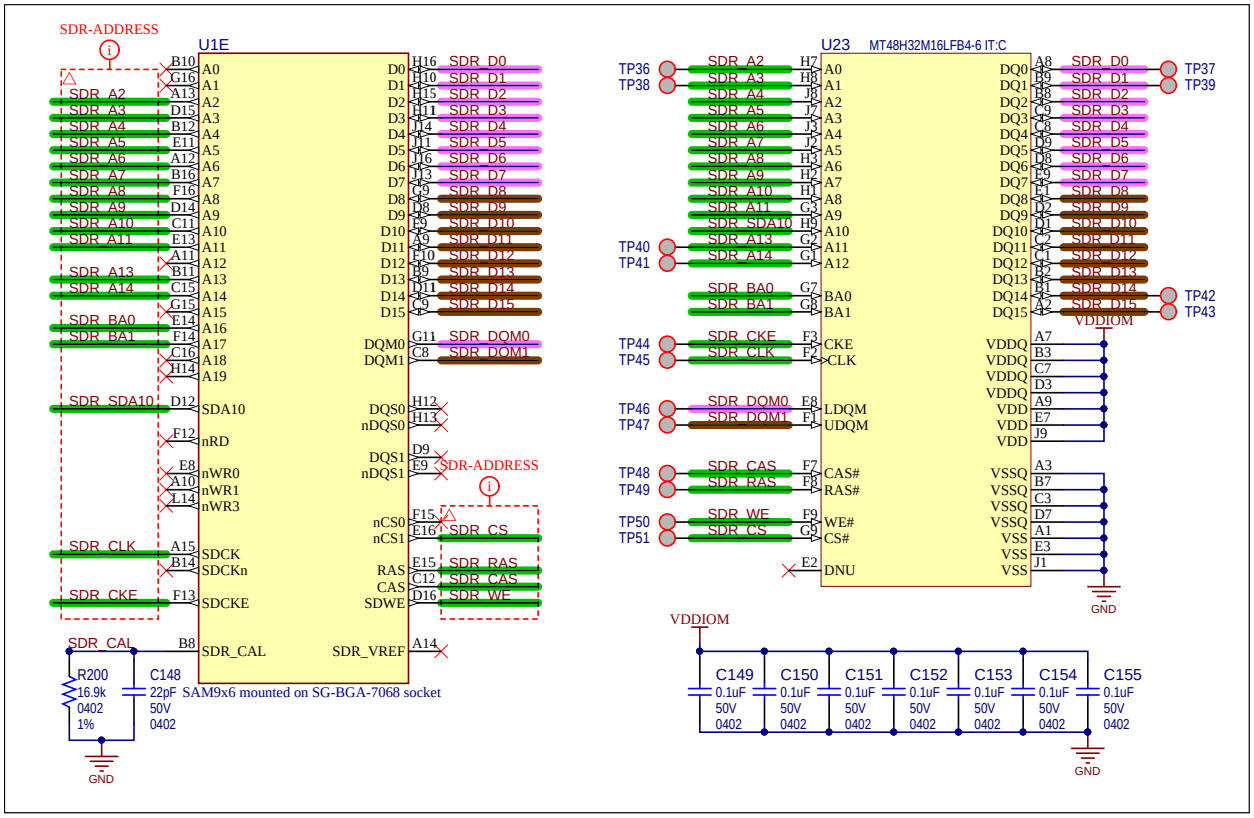
2.1 SDR and LP-SDR SDRAMs on 6-Layer PCB Layout

Because SDR and LP-SDR SDRAMs have the same pinout, only one implementation example, applicable to both, is presented.

Care must be taken when choosing the voltage value for the VDDIOM supply, as SDR memories need 3.3V while LP-SDR memories are powered at 1.8V.

2.1.1 Schematic

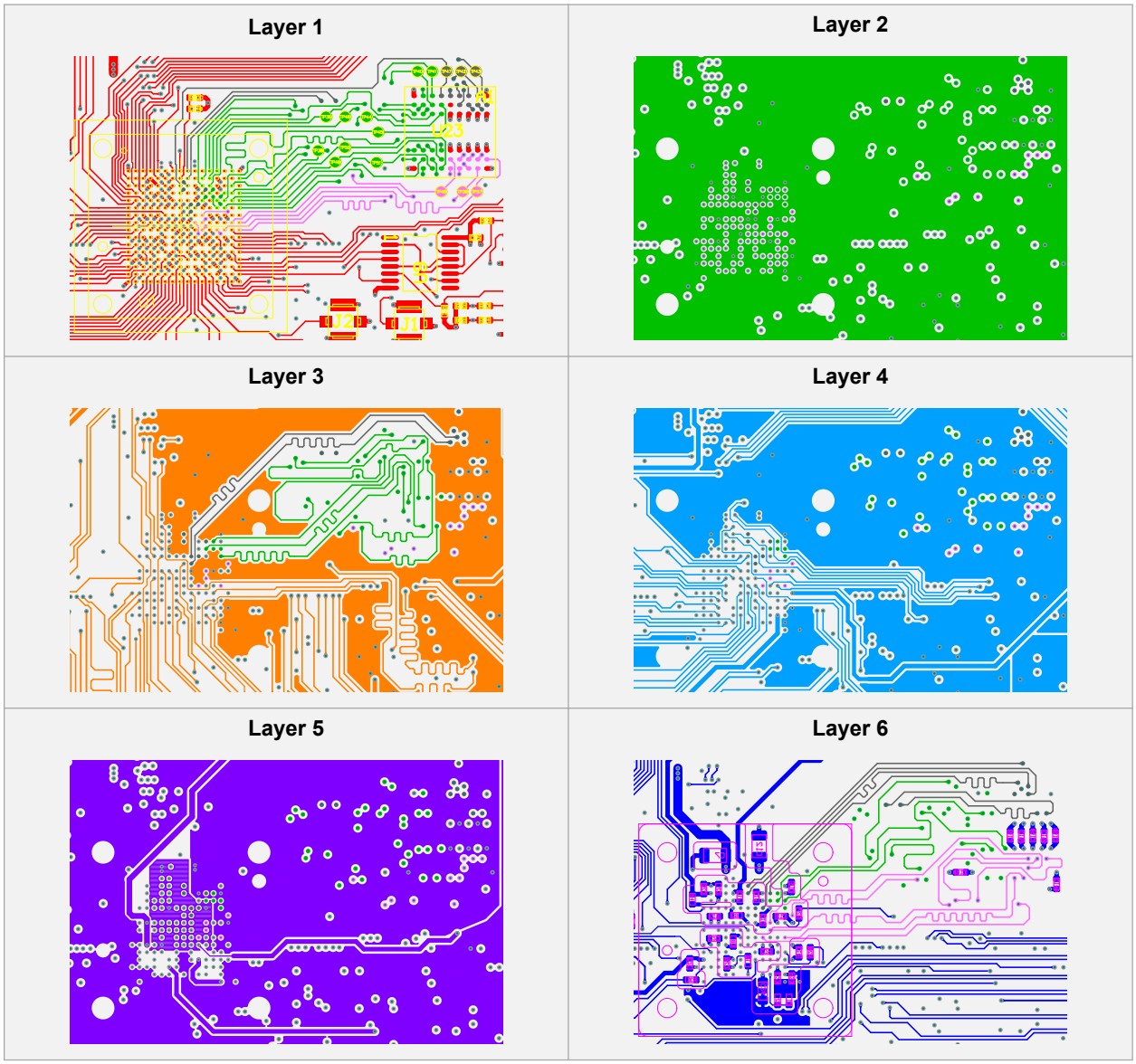
Figure 2-1. LP-SDR Implementation on 6-Layer PCB Layout



2.1.2 Layout

The following figure shows a 6-layer implementation validated on one of the internal engineering boards.

Figure 2-2. LP-SDR and SDR SDRAM 6-Layer PCB Layout Example

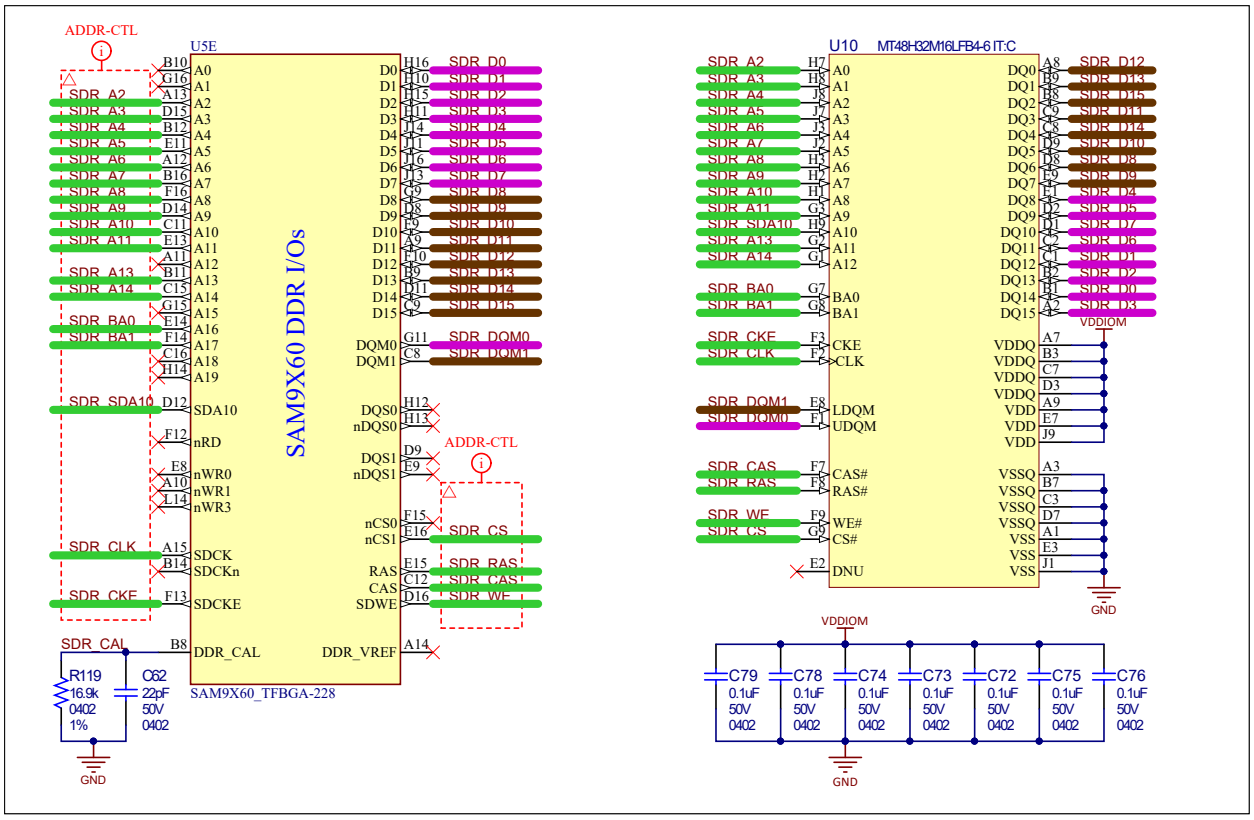


Note: Test points were added to this project to enable signal probing to validate the controller. However, a design can work successfully without them. The connection between the MPU and the memory is then shorter.

2.2 SDR and LP-SDR SDRAMs on 4-Layer PCB Layout

2.2.1 Schematic

Figure 2-3. LP-SDR Implementation on 4-Layer PCB Layout

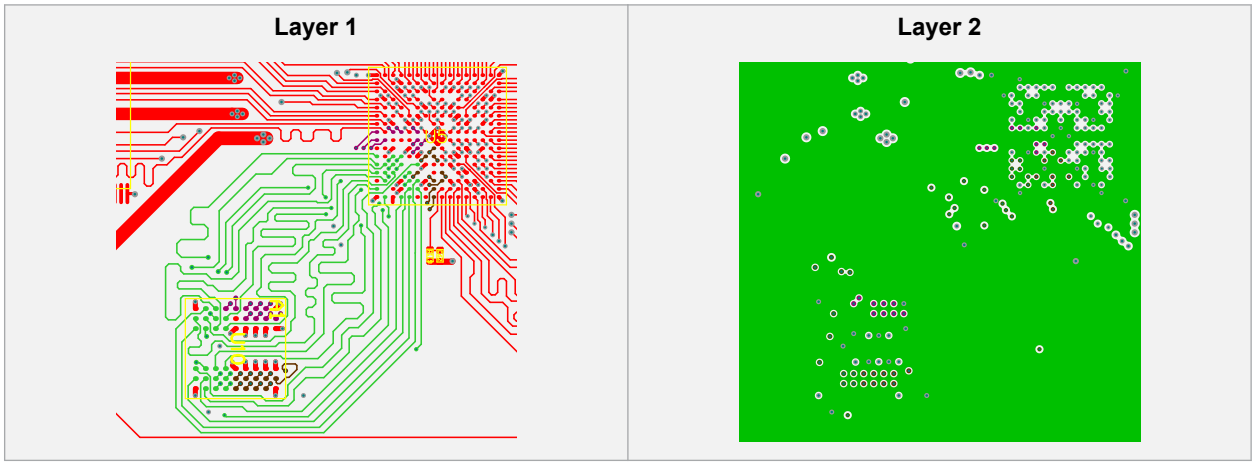


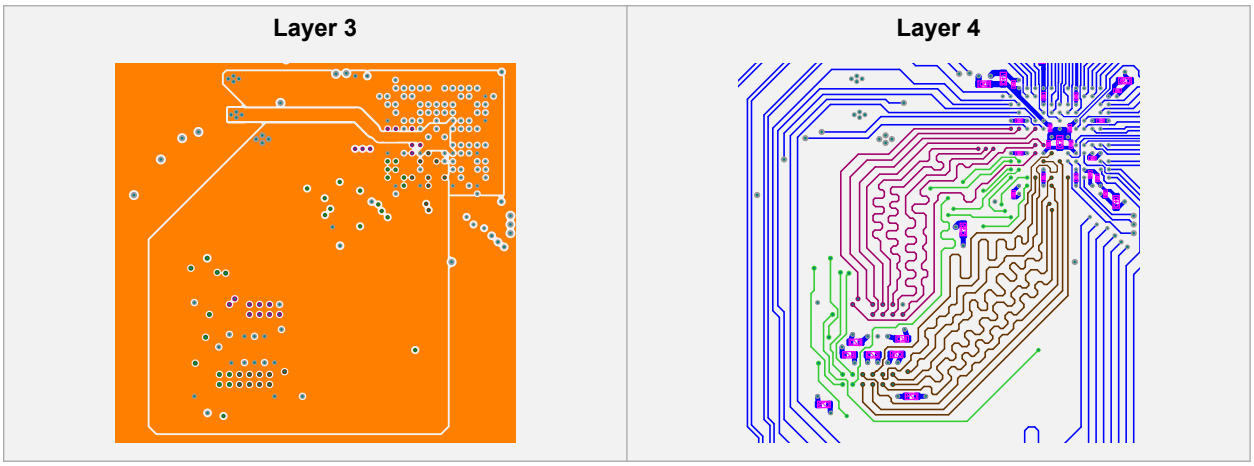
The 4-layer example shows that the data bits are connected differently between the MPU and the memory. A technique called “bit swapping” was used to clean the layout. See 4.1 Bit and Byte Swapping.

2.2.2 Layout

A 4-layer implementation is shown below. This “experimental” design, not meant to be manufactured, shows that devices can be connected on four layers.

Figure 2-4. LP-SDR and SDR SDRAM 4-Layer PCB Layout Example

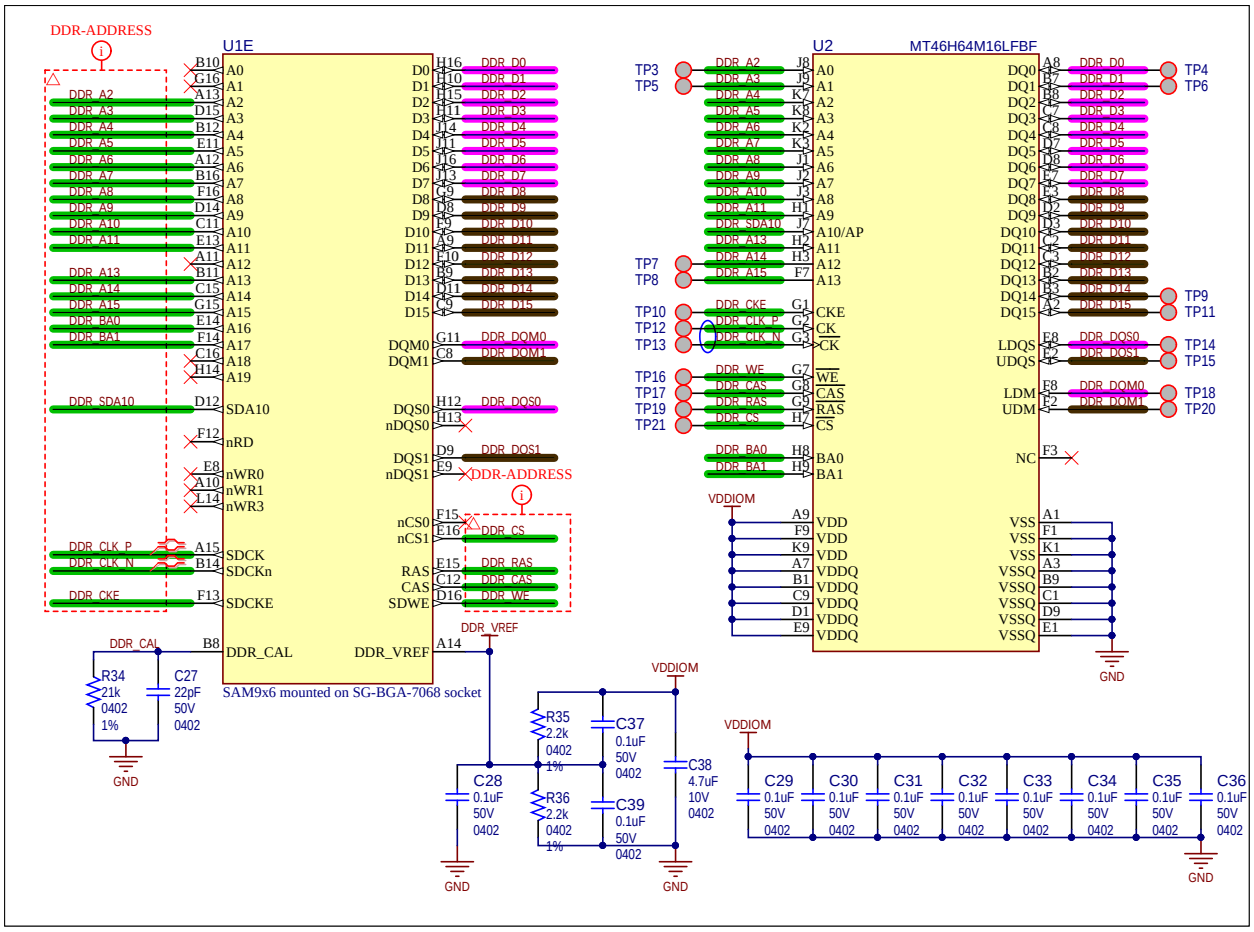




2.3 LP-DDR SDRAM on 6-Layer PCB Layout

2.3.1 Schematic

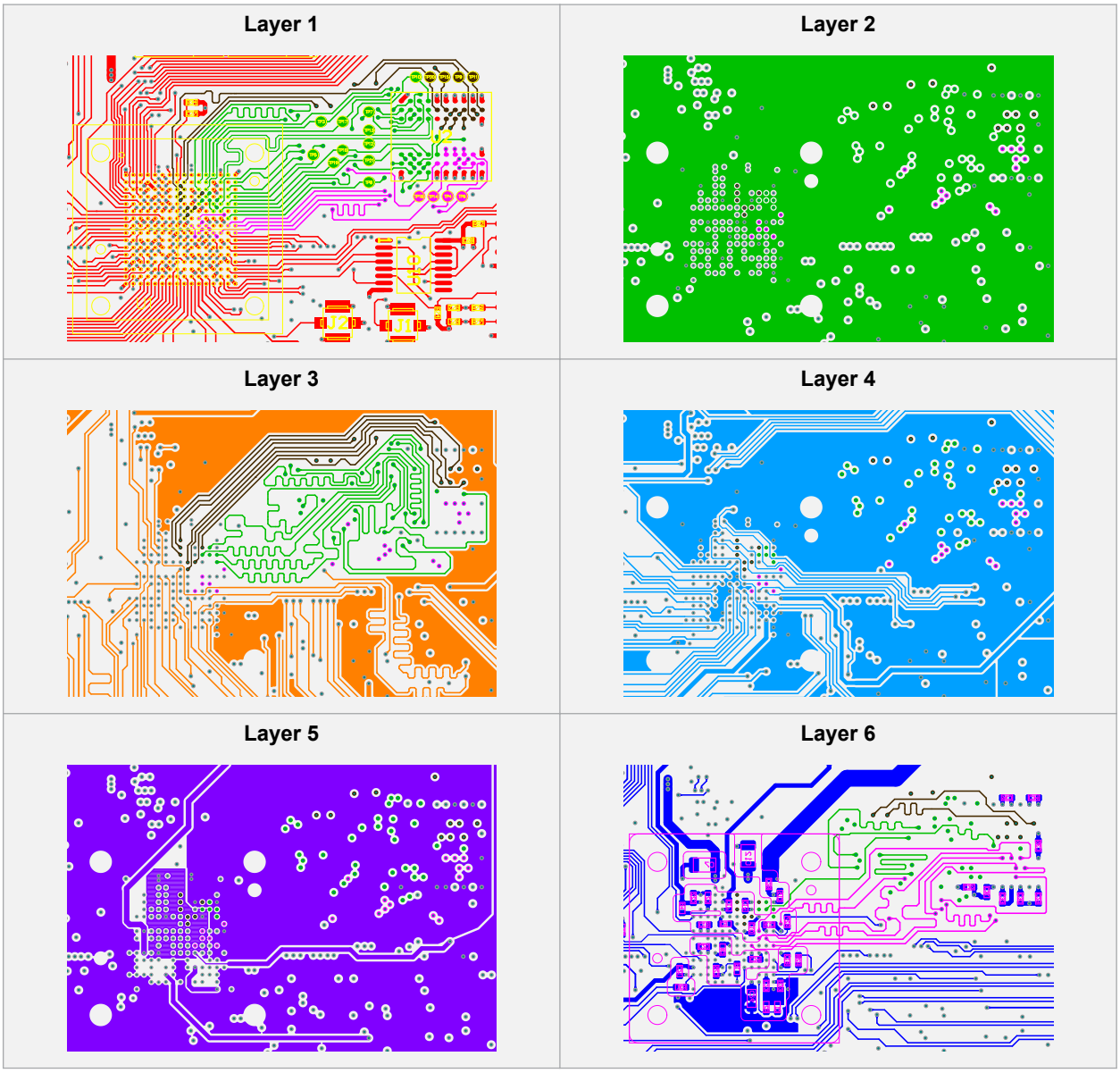
Figure 2-5. LP-DDR Implementation on 6-Layer PCB Layout



2.3.2 Layout

The following figure shows a 6-layer implementation validated on one of the internal engineering boards.

Figure 2-6. LP-DDR SDRAM 6-Layer PCB Layout Example

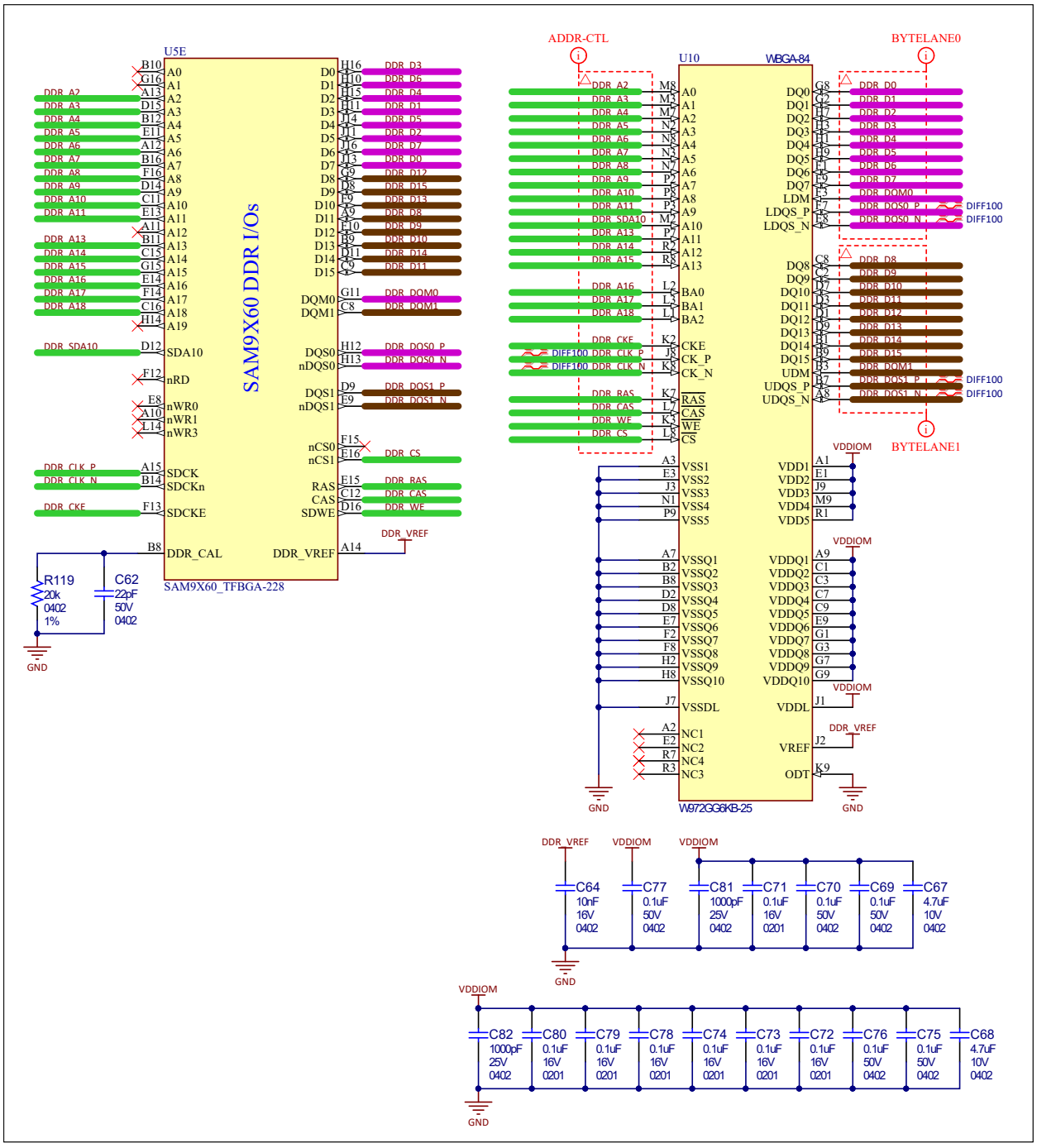


Note: Test points were added to this project to enable signal probing to validate the controller. However, a design can work successfully without them. The connection between the MPU and the memory is then shorter.

2.4 DDR2 SDRAM on 4-Layer PCB Layout

2.4.1 Schematic

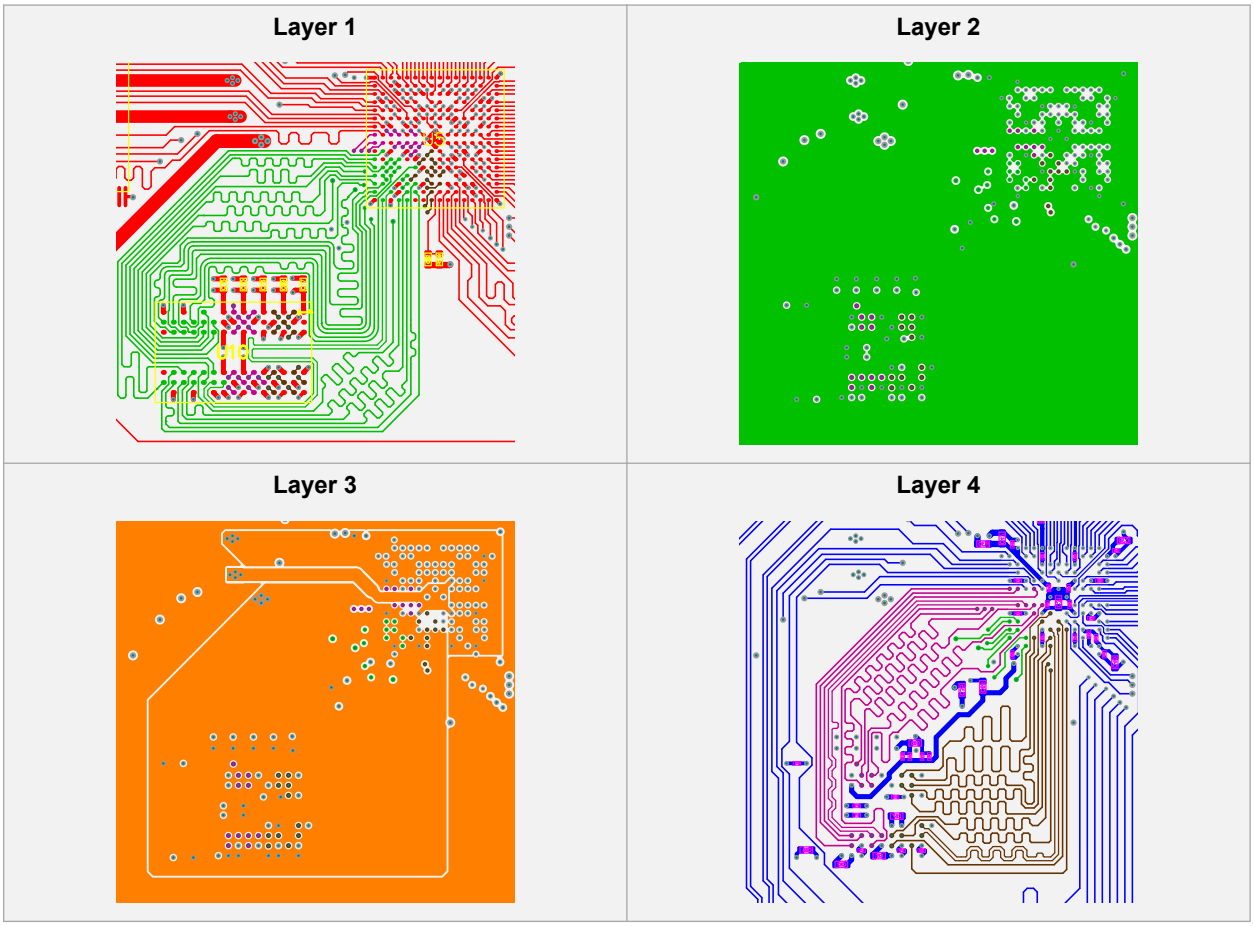
Figure 2-7. DDR2 Implementation



2.4.2 Layout

The following figure shows a 4-layer implementation validated on the SAM9X60-EK evaluation kit. The design files are available for download from the Microchip website. See References.

Figure 2-8. DDR2 SDRAM 4-Layer PCB Layout Example

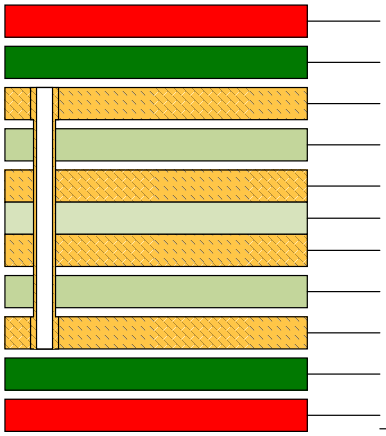


2.5 Stack-Up Recommendations for 4- and 6-Layer PCBs

For all the PCB examples presented above, we recommend the following layer stack-up.

Figure 2-9. 4-Layer Board PCB Stacking

4 Layer Board Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.020mm	Solder Resist	Solder Mask	GTS
Copper	L1 - Top Layer	0.035mm		Signal	GTL
Prepreg		0.090mm		Dielectric	
Copper	L2 - GND	0.035mm		Signal	G1
Core		1.200mm	FR-4	Dielectric	
Copper	L3 - PWR	0.035mm		Signal	G2
Prepreg		0.090mm		Dielectric	
Copper	L4 - Bottom Layer	0.035mm		Signal	GBL
Surface Material	Bottom Solder	0.020mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

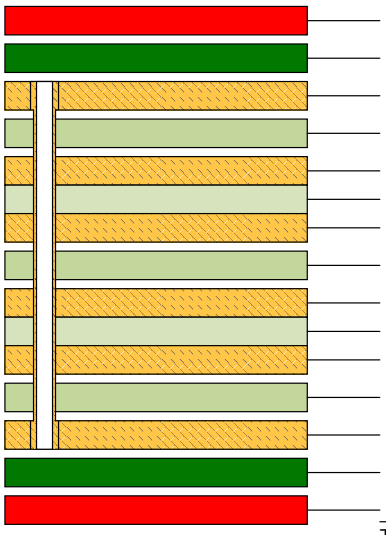
Total thickness: 1.560 mm ± 10%

PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L4	L3	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L4	L3	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L4	L3	125	

Figure 2-10. 6-Layer Board PCB Stacking

6 Layer Board Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.020mm	Solder Resist	Solder Mask	GTS
Copper	L1 - TOP	0.053mm		Signal	GTL
Prepreg		0.090mm	Prepreg	Dielectric	
Copper	L2 - GND	0.036mm		Signal	G1
Core		0.100mm	FR-4	Dielectric	
Copper	L3 - SIG	0.036mm		Signal	G2
Prepreg		0.950mm	Prepreg	Dielectric	
Copper	L4 - SIG	0.036mm		Signal	G3
Core		0.100mm	FR-4	Dielectric	
Copper	L5 - VCC	0.036mm		Signal	G4
Prepreg		0.090mm	Prepreg	Dielectric	
Copper	L6 - BOT	0.053mm		Signal	GBL
Surface Material	Bottom Solder	0.020mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.6 mm ± 10%

PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 15%	L1	L2	135	200
DIFF	90Ω	± 15%	L6	L5	135	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L6	L5	100	200
DIFF	100Ω	± 10%	L3	L2	100	200
DIFF	100Ω	± 10%	L4	L5	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L6	L5	125	
SE	50Ω	± 10%	L3	L2	125	
SE	50Ω	± 10%	L4	L5	125	

3. Software Implementation Considerations

For every SDRAM type, a specific initialization sequence must be performed after system power-up. The required steps are a sequence of electrical patterns executed by software by the microprocessor and applied to the memory device through the embedded DRAM controller (“MPDDRC”) or the SDRAM controller (“SDRAMC”). Refer to chapters “AHB Multiport DDR-SDRAM Controller (MPDDRC)” and “SDRAM Controller (SDRAMC)” of the SAM9X60 data sheet for more information.

The tables in the following subsections describe each initialization step and the actions required, the registers involved in that action, and the settings (values) to write in the register fields, for each type of memory device. After the last step in the initialization sequence, the SDRAM device is fully functional.

Software support is provided with drivers and examples in the form of a software package.

Table footnotes are located in section 3.5 Table Notes.

3.1 SDR SDRAM Initialization

A detailed description of how to initialize the SDR and LP-SDR SDRAMs is provided in section “SDRAM Device Initialization”, in chapter “SDRAM Controller (SDRAMC)” of the SAM9X60 data sheet.

The table below provides the values that must be written in the register fields in the specified order.

Table 3-1. SDR SDRAM Initialization Steps

Step	Action	Register	Setting
0	Configure matrix for SDRAM.	SFR_CCFG_EBICSA	DDR_MP_EN = 1 NFD0_ON_D16 = 1 EBI_CS1A = 1
1	Program SDR SDRAM features. **Note:** These settings apply to the MT48LC16M16 SDR SDRAM; for other devices, refer to the relevant data sheets.	SDRAMC_CR	NC[1:0] = 1 (9 bits) NR[1:0] = 2 (13 bits) NB = 1 (4 banks) CAS[1:0] = 3 (3-cycle) DBW = 1 (16 bits) TWR[3:0] = 12 ns(1) TRC_TRFC[3:0] = 60 ns(1) TRP[3:0] = 18 ns(1) TRCD[3:0] = 18 ns(1) TRAS[3:0] = 42 ns(1) TXSR[3:0] = 67 ns(1)
1’	Set UNAL bit and TMRD value. **Note:** TMRD depends on the memory used.	SDRAMC_CFR1	UNAL = 1 TMRD[3:0] = 2 (2 cycles)
3	Select the SDRAM memory device type.	SDRAMC_MDR	MD[1:0] = 0 (SDRAM) SHIFT_SAMPLING[1:0] = 3
4	200 µs delay(2)	–	–
5	Issue a NOP command(5).	SDRAMC_MR	MODE[2:0] = 1
6	Issue an ALLBANKS_PRECHARGE command.(5)	SDRAMC_MR	MODE[2:0] = 2

.....continued			
Step	**Action**	**Register**	**Setting**
7	Provide 8 autorefresh (CBR) cycles.(5)	SDRAMC_MR	MODE[2:0] = 4
8	Issue a Mode Register Set (MRS) cycle.(4)	SDRAMC_MR	MODE[2:0] = 3
10	Provide a Normal Mode command(5).	SDRAMC_MR	MODE[2:0] = 0
11	Write the refresh rate in the COUNT field.	SDRAMC_TR	COUNT = T_{refi}/T_{ck}

3.2 LP-SDR SDRAM Initialization

A detailed description of how to initialize the SDR and LP-SDR SDRAMs is provided in section “SDRAM Device Initialization”, in chapter “SDRAM Controller (SDRAMC)” of the SAM9X60 data sheet.

The table below provides the values that must be written in the register fields in the specified order.

Table 3-2. LP-SDR SDRAM Initialization Steps

Step	Action	Register	Setting
0	Configure matrix for SDRAM.	SFR_CCFG_EBICSA	DDR_MP_EN = 1 NFD0_ON_D16 = 1 EBI_CS1A = 1
1	Program LP-SDR SDRAM features. **Note:** These settings apply to the MT48H32M16 LP-SDR SDRAM; for other devices, refer to the relevant data sheets.	SDRAMC_CR	NC[1:0] = 2 (10 bits) NR[1:0] = 2 (13 bits) NB = 1 (4 banks) CAS[1:0] = 3 (3-cycle) DBW = 1 (16 bits) TWR[3:0] = 15 ns(1) TRC_TRFC[3:0] = 72 ns(1) TRP[3:0] = 18 ns(1) TRCD[3:0] = 18 ns(1) TRAS[3:0] = 42 ns(1) TXSR[3:0] = 120 ns(1)
1’	Set UNAL bit and TMRD value. **Note:** TMRD depends on the memory used.	SDRAMC_CFR1	UNAL = 1 TMRD[3:0] = 2 (2 cycles)
2	Configure features for LP-SDR.	SDRAMC_LPR	LPCB[1:0] = 1 PASR[2:0] = 0 TCSR[1:0] = 0 DS[1:0] = 2 TIMEOUT[1:0] =2
3	Select the SDRAM memory device type.	SDRAMC_MDR	MD[1:0] = 1 (LP-SDRAM) SHIFT_SAMPLING[1:0] = 3
4	200 µs delay(2)	–	–

.....continued			
Step	**Action**	**Register**	**Setting**
5	Issue a NOP command.(5)	SDRAMC_MR	MODE[2:0] = 1
6	Issue an ALLBANKS_PRECHARGE command.(5)	SDRAMC_MR	MODE[2:0] = 2
7	Provide 8 autorefresh (CBR) cycles.(5)	SDRAMC_MR	MODE[2:0] = 4
8	Issue a Mode Register Set (MRS) cycle.(4)	SDRAMC_MR	MODE[2:0] = 3
9	Issue an EMRS cycle(3) for LP-SDR.	SDRAMC_MR	MODE[2:0] = 5
10	Provide a Normal Mode command.(5)	SDRAMC_MR	MODE[2:0] = 0
11	Write the refresh rate in the COUNT field.	SDRAMC_TR	MODE[2:0] = T_{refi}/T_{ck}

3.3 LP-DDR SDRAM Initialization

A detailed description of how to initialize the LP-DDR SDRAM is provided in section “Low-power DDR1-SDRAM Initialization”, in chapter “AHB Multiport DDR-SDRAM Controller (MPDDRC)” of the SAM9X60 data sheet.

The table below provides the values that must be written in the register fields in the specified order.

Table 3-3. LP-DDR SDRAM Initialization Steps

Step	Action	Register	Setting
0	Configure matrix for SDRAM.	SFR_CCFG_EBICSA	DDR_MP_EN = 1 NFD0_ON_D16 = 1 EBI_CS1A = 1
1	Program the memory device type.	MPDDRC_MD	MD = 3 (for LPDDR1) DBW = 1 (16 bits)
2	Disable NDQS.	MPDDRC_CR	NDQS = 1 (disabled)
3	Program the shift sampling value.	MPDDRC_RD_DATA_PATH	SHIFT_SAMPLING[1:0] = 1

.....continued

Step	Action	Register	Setting
4	Program LP-DDR SDRAM features. **Note:** These settings apply to the MT46H64M16 LPDDR SDRAM; for other devices, refer to the relevant data sheets.	MPDDRC_CR	NC[1:0] = 2 (10 bits) NR[1:0] = 3 (14 bits) CAS[1:0] = 3 (3-cycle) NB = 0 (4 banks) DECOD = 1 (interleaved)
		MPDDRC_TPR0	TRAS[3:0] = 40 ns(1) TRCD[3:0] = 15 ns(1) TWR[3:0] = 15 ns(1) TRC[3:0] = 55 ns(1) TRP[3:0] = 15 ns(1) TRRD[3:0] = 10 ns(1) TWTR[2:0] = 2 (2 cycles) TMRD[3:0] = 2 (2 cycles)
		MPDDRC_TPR1	TRFC[6:0] = 72 ns(1) TXSNR[7:0] = 112.5 ns(1) TXSRD[7:0] = 2 (2 cycles) TXP[3:0] = 2 (2 cycles)
5	Program TCR, PASR and DS.	MPDDRC_LPR	DS[2:0] = 2
6	Issue a NOP command.(4)	MPDDRC_MR	MODE[2:0] = 1
7	200 µs delay(1)	–	–
8	Issue a NOP command.(4)	MPDDRC_MR	MODE[2:0] = 1
9	Issue an ALLBANKS_PRECHARGE command.(4)	MPDDRC_MR	MODE[2:0] = 2
10	Provide two autorefresh (CBR) cycles.(4)	MPDDRC_MR	MODE[2:0] = 4
11	Issue an EMRS cycle.(2)	MPDDRC_MR	MODE[2:0] = 5
12	Issue a Mode Register Set (MRS) cycle.(3)	MPDDRC_MR	MODE[2:0] = 3
13	Provide a Normal Mode command.(4)	MPDDRC_MR	MODE[2:0] = 0
14	Write the refresh rate in the COUNT field.	MPDDRC_RTR	COUNT = T_{refi}/T_{ck}

3.4 DDR2 SDRAM Initialization

A detailed description of how to initialize the DDR2 SDRAM is provided in section “DDR2-SDRAM Initialization”, in chapter “AHB Multiport DDR-SDRAM Controller (MPDDRC)” of the SAM9X60 data sheet.

The table below provides the values that must be written in the register fields in the specified order.

Table 3-4. DDR2 SDRAM Initialization steps

Step	Action	Register	Setting
0	Configure matrix for SDRAM.	SFR_CCFG_EBICSA	DDR_MP_EN = 1 NFD0_ON_D16 = 1 EBI_CS1A = 1
1	Program the memory device type.	MPDDRC_MD	MD = 6 (for DDR2) DBW = 1 (16 bits)
2	Program the shift sampling value.	MPDDRC_RD_DATA_PATH	SHIFT_SAMPLING[1:0] = 1
3	Program DDR2 SDRAM features. **Note:** These settings apply to the W972GG6KB DDR2 SDRAM; for other devices, refer to the relevant data sheets.	MPDDRC_CR	NC[1:0] = 1 (10 bits) NR[1:0] = 3 (14 bits) CAS[1:0] = 3 (3-cycle) NB = 1 (8 banks) DECOD = 1 (interleaved)
		MPDDRC_TPR0	TRAS[3:0] = 45 ns(1) TRCD[3:0] = 12.5 ns(1) TWR[3:0] = 15 ns(1) TRC[3:0] = 57.5 ns(1) TRP[3:0] = 12.5 ns(1) TRRD[3:0] = max (10 ns(1), 2 cycles) TWTR[2:0] = max (8 ns(1), 2 cycles) TMRD[3:0] = 2 (2 cycles)
		MPDDRC_TPR1	TRFC[6:0] = 195 ns(1) TXSNR[7:0] = TRFC + 10 ns(1) TXSRD[7:0] = 200 (cycles) TXP[3:0] = 2 (cycles)
		MPDDRC_TPR2	TXARD[3:0] = 2 (cycles) TXARDS[3:0] = 8 (cycles) TRPA[3:0] = TRP + 1 cycle TRTP[2:0] = max (8 ns(1), 4 cycles) TFAW[3:0] = 45 ns(1)
4	Issue a NOP command.(4)	MPDDRC_MR	MODE = 1
5	200 µs delay(1)	–	–
6	Issue a NOP command.(4)	MPDDRC_MR	MODE = 1
7	Issue an ALLBANKS_PRECHARGE command(4)	MPDDRC_MR	MODE = 2
8	Issue an EMRS2 cycle.(2)	MPDDRC_MR	MODE = 5
9	Issue an EMRS3 cycle(2)	MPDDRC_MR	MODE = 5
10	Issue an EMRS1 cycle.(2)	MPDDRC_MR	MODE = 5

.....continued

Step	Action	Register	Setting
11	200 cycles delay(1)	-	-
12	Write a '1' to the DLL bit.	MPDDRC_CR	DLL = 1
13	Issue a Mode Register Set (MRS) cycle. (3)	MPDDRC_MR	MODE = 3
14	Issue an ALLBANKS_PRECHARGE command.(4)	MPDDRC_MR	MODE = 2
15	Provide two autorefresh (CBR) cycles.(4)	MPDDRC_MR	MODE = 4
16	Write a '0' to the DLL bit	MPDDRC_CR	DLL = 0
17	Issue a Mode Register Set (MRS) cycle. (3)	MPDDRC_MR	MODE = 3
18	Configure the OCD field to 7.	MPDDRC_CR	OCD = 7
19	Issue an EMRS1 cycle.(2)	MPDDRC_MR	MODE = 5
20	Configure the OCD field to 0	MPDDRC_CR	OCD = 0
21	Issue an EMRS1 cycle.(2)	MPDDRC_MR	MODE = 5
22	Provide a Normal Mode command.(4)	MPDDRC_MR	MODE = 0
23	Write the refresh rate in the COUNT field.	MPDDRC_RTR	COUNT = T_{refi}/T_{ck}

3.5 Table Notes

1. Must be converted to cycles depending on the system clock.
   - The formula is: (time[ns] * clock[MHz] + 999) / 1000
2. To issue a delay:
   - Disable interrupts.
   - Compute a deadline = ROUND_INT_DIV((timer_channel_freq/1000)*count, 1000), where count is the delay in µs.
   - Start a timer and wait for the timer to reach the deadline.
   - Enable interrupts.
3. To issue an Extended Mode Register Set (EMRS) cycle, after setting the MODE field to 5, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Then, perform a write access to the DDR2 SDRAM device so that the BA[1:0] signals are as follows:
   - BA[1] is set to 0, BA[0] is set to 1 for EMRS1;
   - BA[1] is set to 1, BA[0] is set to 0 for EMRS2;
   - BA[1] is set to 1, BA[0] is set to 1 for EMRS3.

   The address at which the write access is issued to acknowledge the command needs to be calculated so that the BA[1:0] signals are in the right state for an EMRS cycle.
4. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to acknowledge the command so that BA[2:0] signals are set to 0 (write at BASE_ADDRESS_DDR).
5. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any address to acknowledge the command.

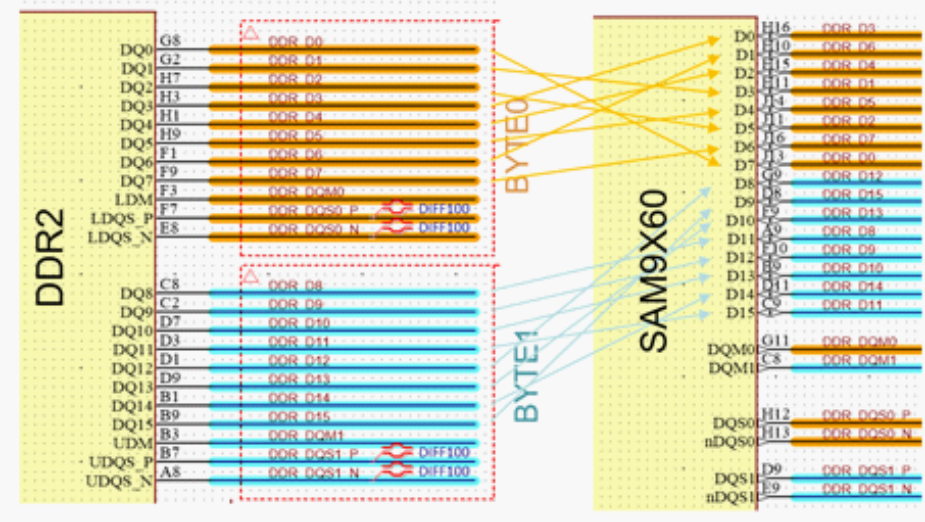
4. Appendix

4.1 Bit and Byte Swapping

DDR2 memories support **bit swapping**, a technique the designer can use to interchange data lines with one another, provided that they correspond to the same byte lane (e.g. any bits inside the D[0..7] lane). This is very useful when trying to optimize a DDR layout routing.

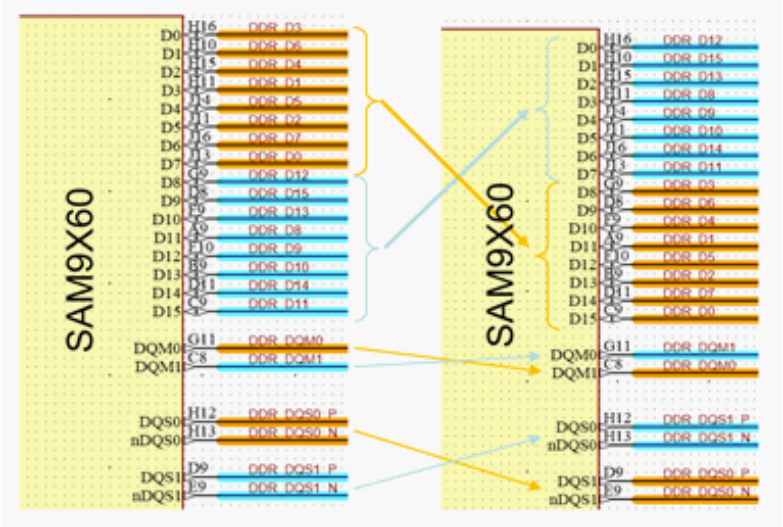
The following figure shows an example of the bit swapping technique implemented in the SAM9X60-EK board design.

Figure 4-1. DDR2 Bit Swapping



Byte swapping is another technique that can be used on DDR2 memories. It allows the designer to swap the data lanes with one another, also for the purpose of optimizing the layout. Remember to also swap the DQMx and DQSx signals corresponding to the swapped byte lanes, as illustrated below.

Figure 4-2. DDR2 Byte Swapping



4.2 Good Practices

The following is a list of suggestions for designing with high-speed signals:

- Use controlled impedance PCB traces that match the specified single-ended (50Ω) and differential (100Ω) impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing required to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs, any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- Route CMOS/TTL and differential signals on different layers, which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Use a minimum of 20 mils spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND), avoiding cross splits or openings in those planes.
- For microstrip or stripline transmission lines, keep the spacing between adjacent signal paths at least twice the line width.
- Keep all traces at least five line widths away from the edge of the board.
- Follow the return path of each signal and keep the width of the return path under each signal path at least as wide, and preferably at least three times as wide, as the signal trace.
- To avoid EMIs, avoid routing switching signals across splits or openings in ground planes. Routing around them is preferable even if it results in longer paths.
- Minimize the loop inductance between the power and ground paths.
- Allocate power and ground planes on adjacent layers with as thin a dielectric as possible to create plane capacitance.
- Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
- Supply voltages must be composed of planes only, not traces. Short connections (≈ 8 mils) are commonly used to attach vias to planes. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance (20 mils trace width).

5. Revision History

5.1 Rev. A - 11/2019

First issue.

The Microchip Website

Microchip provides online support via our website at http://www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to http://www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with

your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-5212-6

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit http://www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: http://www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

© 2019 Microchip Technology Inc.