AN1995

LAN9252 SOC Porting Guidelines

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INTRODUCTION

This document describes the guidelines for creating hardware abstraction layer/PDI driver files for SSC for LAN9252.

This document includes the following topics:

Abbreviations

SPI – Serial peripheral interface

HBI – Hub bus interface

ESC – EtherCAT® core

CSR – Control and status register

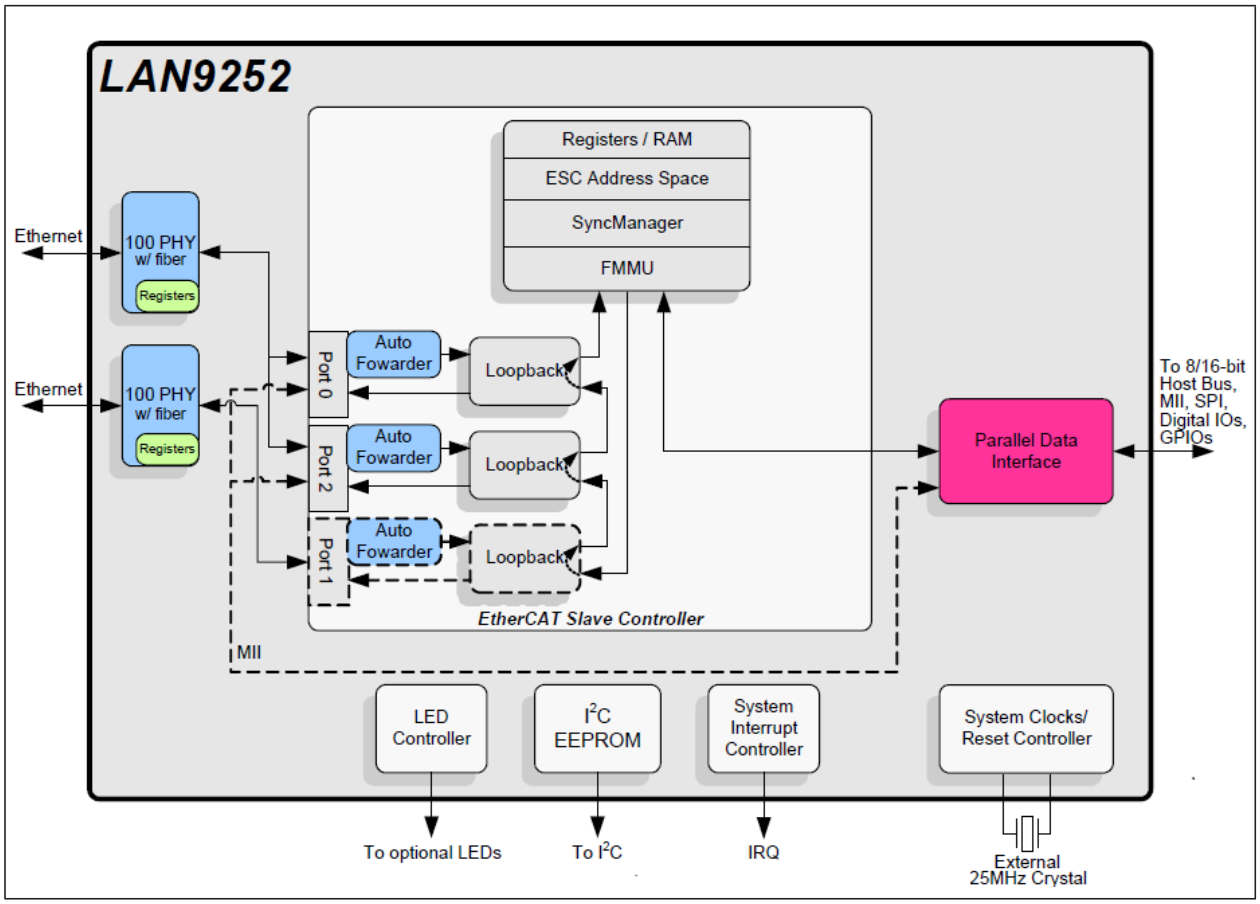
SSC – Slave Stack Code

HAL – Hardware Abstraction Layer

LAN9252 ARCHITECTURE

The LAN9252 can be configured to different modes as per EEPROM configuration. Further details can be found within the LAN9252 data sheet. Figure 1 provides an internal block diagram of the LAN9252. The LAN9252 can operate in Microcontroller, Expansion, or Digital I/O mode, as displayed in Figure 2

FIGURE 1: LAN9252 BLOCK DIAGRAM



Microcontroller Mode

The LAN9252 communicates with the microcontroller through an SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 8- or 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with an 8- or 16-bit external bus.

Alternatively, the device can be accessed via SPI or Quad SPI, while also providing up to 16 inputs or outputs for general purpose usage.

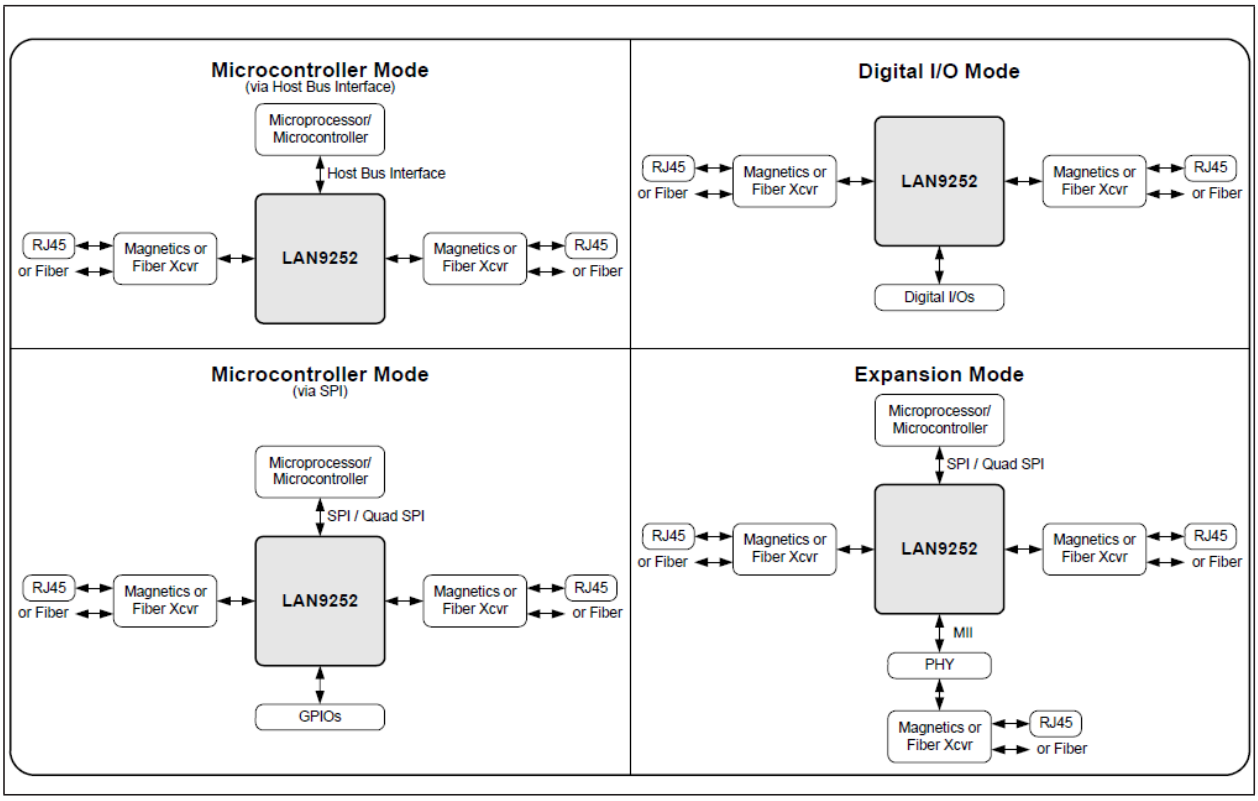
Expansion Mode

While the device is in SPI or Quad SPI mode, a third networking port can be enabled to provide an additional MII port. This port can either be connected to an external PHY, to enable star or tree network topologies, or to another LAN9252 to create a four port solution. This port can be configured for the upstream or downstream direction.

Digital I/O Mode

For simple digital modules without microcontrollers, the LAN9252 can operate in Digital I/O Mode where 16 digital signals can be controlled or monitored by the EtherCAT master. Six control signals are also provided.

FIGURE 2: LAN9252 MODES

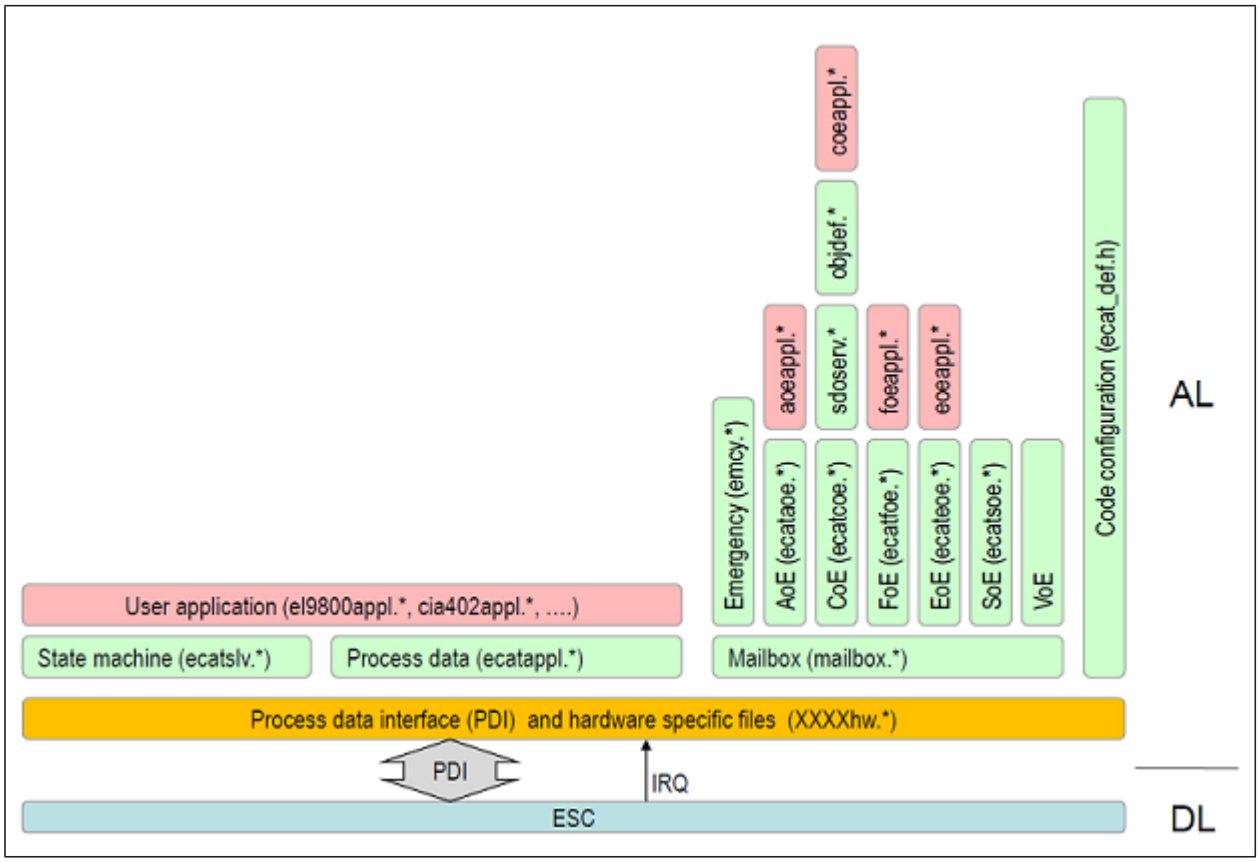


SSC is applicable in Microcontroller mode and expansion mode where Microprocessor/Microcontroller interface (PDI) is available.

BECKHOFF'S SSC ARCHITECTURE

Figure 3 illustrates the Beckhoff SSC Architecture. The SSC code can be downloaded from the EtherCAT Technology Group website: https://www.ethercat.org/. For integrating SSC code with LAN9252, Hardware Abstraction Layer (PDI-XXXXhw.*) to access ESC has to be defined.

FIGURE 3: BECKHOFF'S SSC ARCHITECTURE



LAN9252 HARDWARE ABSTRACTION LAYER

These are the function to be defined in XXXXhw.* to access the SSC.

1. UINT8 HW_Init(void);
2. void HW_Release(void);
3. UINT16 HW_GetALEventRegister(void);
4. UINT16 HW_GetALEventRegister_Isr(void);
5. void HW_ResetALEventMask(UINT16 intMask);
6. void HW_SetALEventMask(UINT16 intMask);
7. void HW_EscRead(MEM_ADDR * pData, UINT16 Address, UINT16 Len);
8. void HW_EscReadIsr(MEM_ADDR *pData, UINT16 Address, UINT16 Len);
9. void HW_EscWrite(MEM_ADDR *pData, UINT16 Address, UINT16 Len);
10. void HW_EscWriteIsr(MEM_ADDR *pData, UINT16 Address, UINT16 Len);
11. void HW_DisableSyncManChannel(UINT8 channel);
12. void HW_EnableSyncManChannel(UINT8 channel);
13. TSYNCMAN ESCMEM *HW_GetSyncMan(UINT8 channel);
14. Interrupts for IRQ, SYNC0 and SYNC1
15. Timer Interrupt.

GUIDELINES FOR PORTING LAN9252-PIC32_SDK_VX.X TO OTHER SOCS

LAN9252 Hardware Initialization

1. EtherCAT core register read/write.
2. Protection of CSR registers.

SOCs can access LAN9252 using different types Process Data Interfaces (PDI) like HBI, SPI or SQI.

The hardware and software details for various PDI are defined in AN1907 “Microchip LAN9252 Migration from Beckhoff ET1100”.

ESC Register Read/Write

There are two types of registers available in the LAN9252:

1. Directly accessible registers.

FIGURE 4: DIRECTLY ACCESSIBLE REGISTERS

Address	Register Name (Symbol)
000h-01Ch	EtherCAT Process RAM Read Data FIFO (ECAT_PRAM_RD_DATA)
020h-03Ch	EtherCAT Process RAM Write Data FIFO (ECAT_PRAM_WR_DATA)
050h	Chip ID and Revision (ID_REV)
054h	Interrupt Configuration Register (IRQ_CFG)
058h	Interrupt Status Register (INT_STS)
05Ch	Interrupt Enable Register (INT_EN)
064h	Byte Order Test Register (BYTE_TEST)
074h	Hardware Configuration Register (HW_CFG)
084h	Power Management Control Register (PMT_CTRL)
08Ch	General Purpose Timer Configuration Register (GPT_CFG)
090h	General Purpose Timer Count Register (GPT_CNT)
09Ch	Free Running 25MHz Counter Register (FREE_RUN)
Reset Register	
1F8h	Reset Control Register (RESET_CTL)
EtherCAT Registers	
300h	EtherCAT CSR Interface Data Register (ECAT_CSR_DATA)
304h	EtherCAT CSR Interface Command Register (ECAT_CSR_CMD)
308h	EtherCAT Process RAM Read Address and Length Register (ECAT_PRAM_RD_ADDR_LEN)
30Ch	EtherCAT Process RAM Read Command Register (ECAT_PRAM_RD_CMD)
310h	EtherCAT Process RAM Write Address and Length Register (ECAT_PRAM_WR_ADDR_LEN)
314h	EtherCAT Process RAM Write Command Register (ECAT_PRAM_WR_CMD)

2. Indirectly accessible registers – All EtherCAT core registers

Using EtherCAT CSR Interface Command Register (ECAT_CSR_CMD) and EtherCAT CSR Interface Data Register (ECAT_CSR_DATA) to perform read and write operations with the EtherCAT Core registers and Process Data RAM Access.

The indirectly accessible EtherCAT Core CSRs are accessed at address 0h through 0FFFh and via EtherCAT Core CSR Registers (Indirectly Addressable).

The EtherCAT Core Process Data RAM can be accessed indirectly via the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA) and EtherCAT CSR Interface Command Register (ECAT_CSR_CMD), starting at 1000h.

Refer LAN9252 datasheet for more detailed description.

ESC READ

To perform a read of an individual EtherCAT Core register, the read cycle must be initiated by performing a single write to the EtherCAT CSR Interface Command Register (ECAT_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR) field set to the desired register address, the Read/Write (R_nW) bit set, and the CSR Size (CSR_SIZE) field set to the desired size.

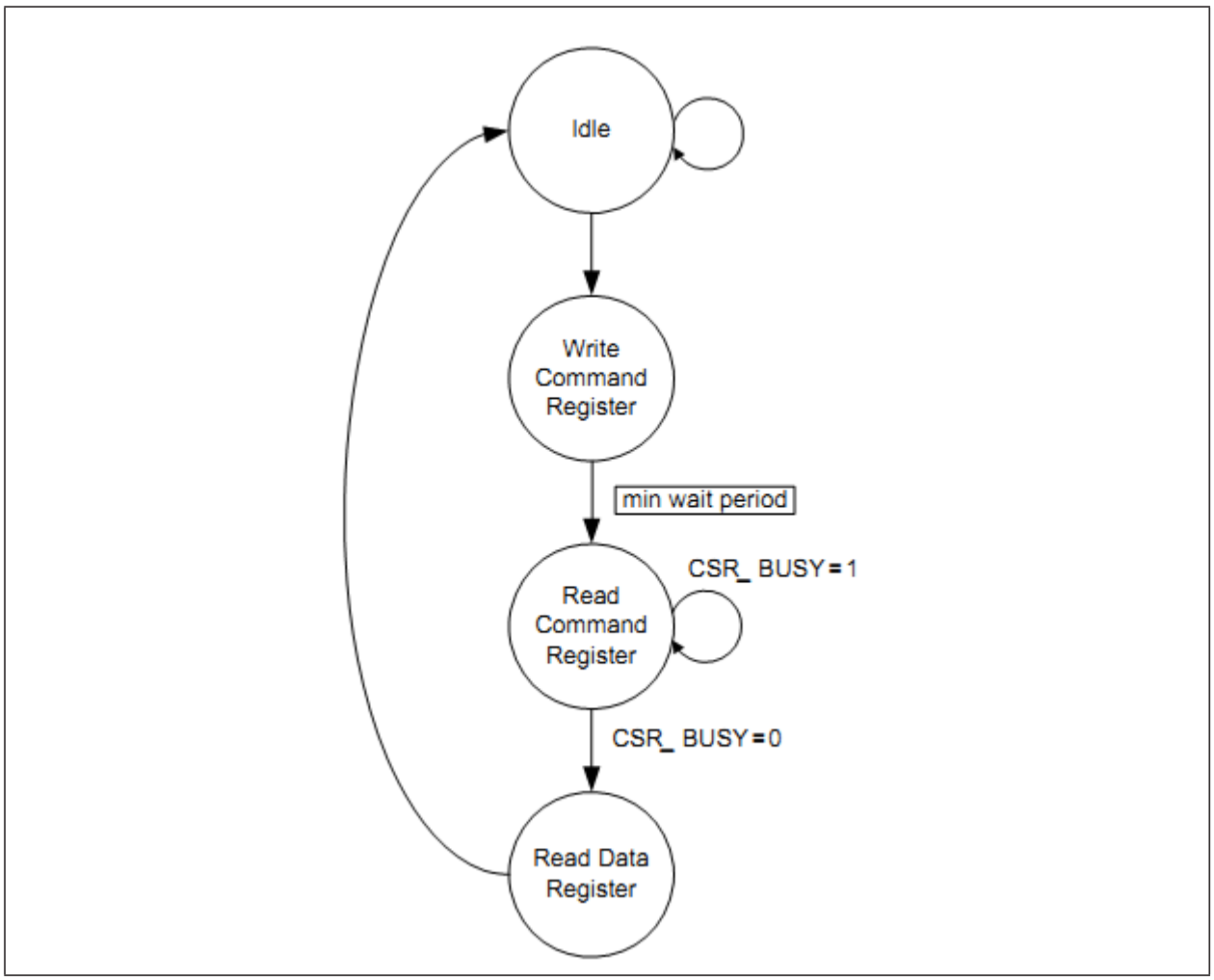
Valid data is available for reading when the CSR Busy (CSR_BUSY) bit is cleared, indicating that the data can be read from the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA).

Valid data is always aligned into the lowest bits of the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA).

For example, Read 0x1000 register with length 4:

- Write 0xc0041000 Register address 0x0304 (ECAT_CSR_CMD)
- Wait for Busy bit(CSR_BUSY) to clear
- Read 0x0300(ECAT_CSR_DATA) register for data

FIGURE 5: CSR READ



ESC WRITE REGISTER

To perform a read of an individual EtherCAT Core register, the read cycle must be initiated by performing a single write to the EtherCAT CSR Interface Command Register (ECAT_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR) field set to the desired register address, the Read/Write (R_nW) bit set and the CSR Size (CSR_SIZE) field set to the desired size.

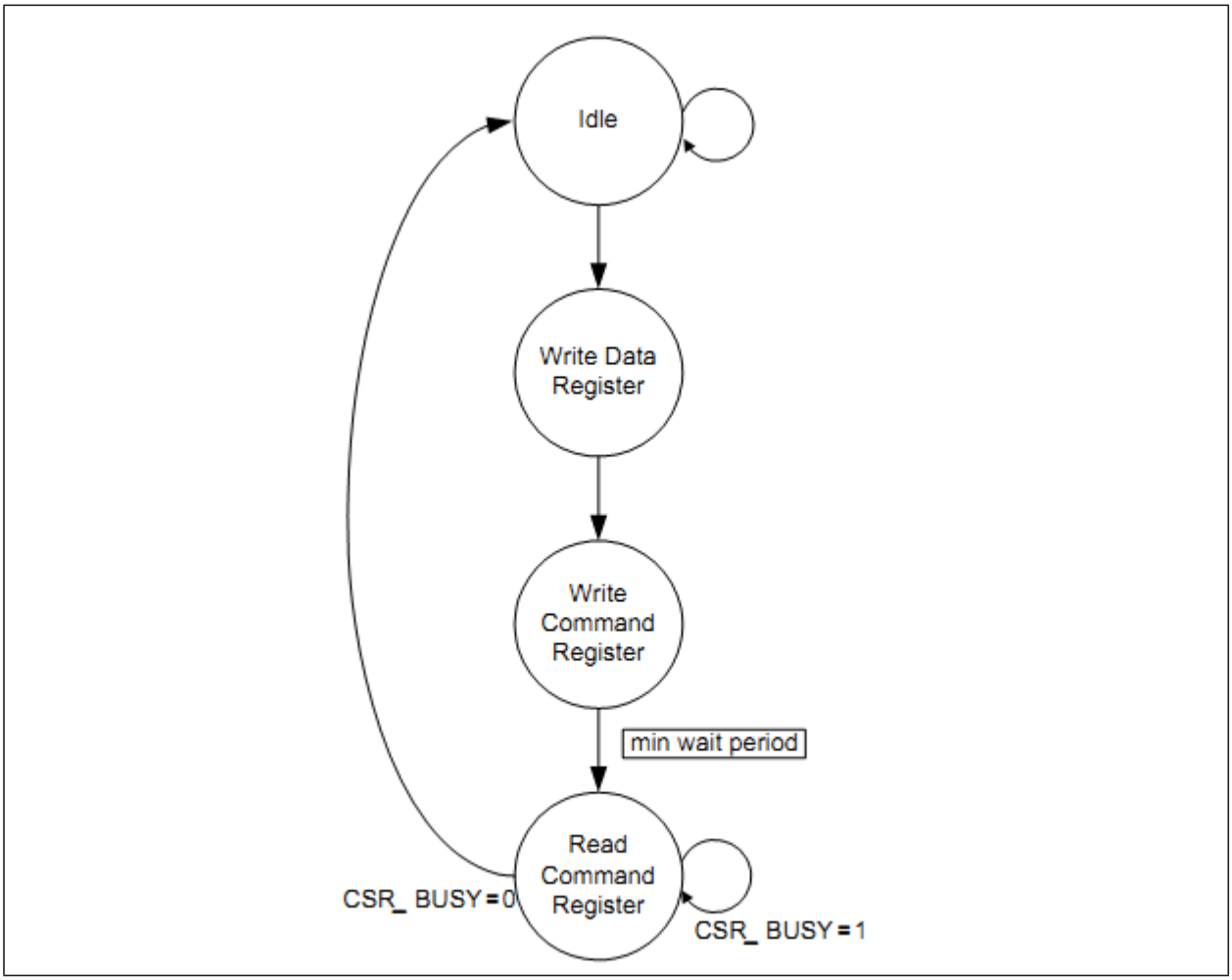
To perform a write to an individual EtherCAT Core register, the desired data must first be written into the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA). Valid data is always aligned into the lowest bits of the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA). The write cycle is initiated by performing a single write to the EtherCAT CSR Interface Command Register (ECAT_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR)field set to the desired register address, the Read/Write (R_nW) bit cleared and the CSR Size (CSR_-SIZE) field set to the desired size. The completion of the write cycle is indicated by the clearing of the CSR Busy (CSR_BUSY) bit.

Below figure illustrates the process required to perform a EtherCAT Core CSR write. Minimum wait periods are required where noted, as specified in the LAN9252 data sheet, under Table 5-2 “Read After Write Timing Rules.”

For example, Write 4 bytes in 0x1000 Register Address:

- Write Data to be written in the register 0x0300
- Write 0x80041000 in 0x0304 Register
- Wait for Bust bit clear to complete write operation

FIGURE 6: CSR WRITE



The host interfaces that are disabled during the reset state/power on, the BYTE_TEST register (0x64) can be used to determine when the device has exited the reset state. So, polling the register BYTE_TEST can be used to determine whether LAN9252 is in READY state. For more details check BYTE_TEST register in the datasheet.

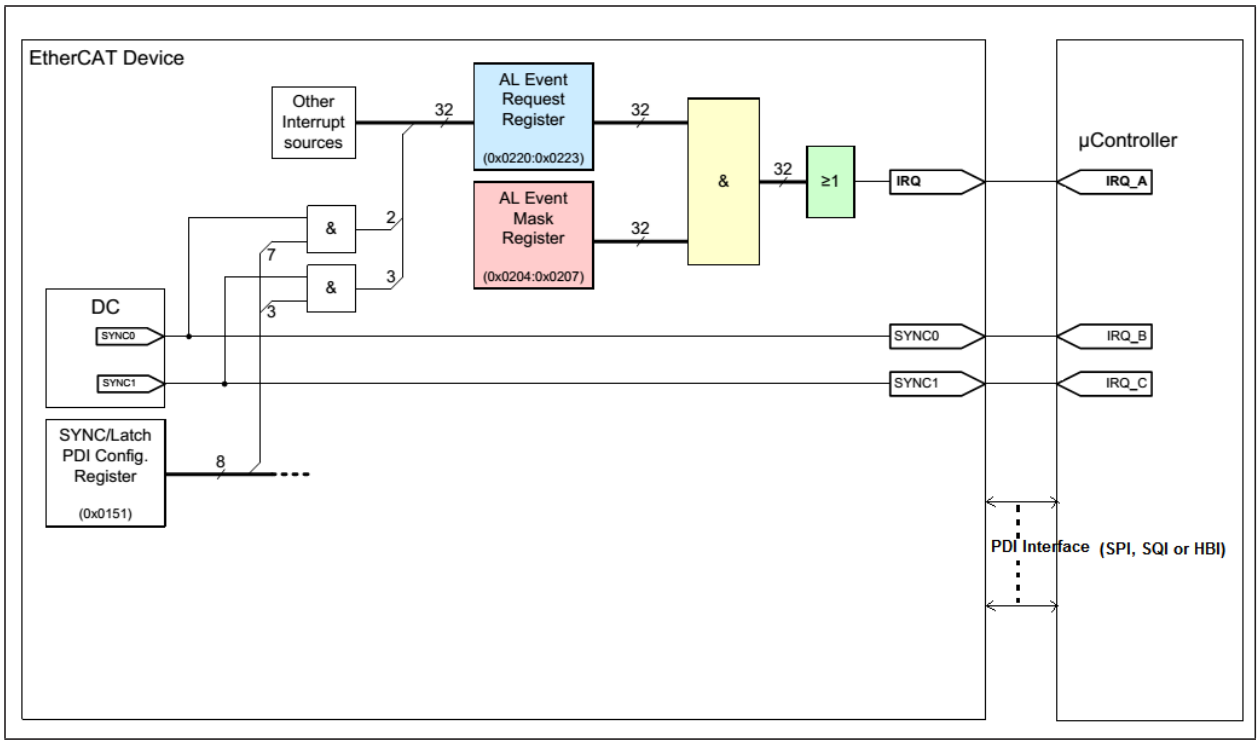
Interrupts

All interrupts have to be configured during hardware initialization.

PDI INTERRUPT

The programmable system interrupts are generated internally by the various device sub-modules and can be configured to generate a single external host interrupt via the IRQ interrupt output pin. The programmable nature of the host interrupt provides the user with the ability to optimize performance dependent upon the application requirements. The IRQ interrupt buffer type, polarity and de-assertion interval are modifiable. The IRQ interrupt can be configured as an open-drain output to facilitate the sharing of interrupts with other devices. All internal interrupts are mask able and capable of triggering the IRQ interrupt.

FIGURE 7: PDI INTERRUPT



If the application running on the SOC requires AL Event Interrupt, then the IRQ line should be connected to microcontroller input interrupt. The configuration of IRQ can be done using INTERRUPT CONFIGURATION REGISTER (IRQ_CFG) - 0x54 and INTERRUPT ENABLE REGISTER (INT_EN) - 0x5C. For more details, see the LAN9252 datasheet.

DC - SYNC0 AND SYNC1

If the application running on the SOC requires Distributed clock, then SYNC0 and SYNC1 should be connected to the microcontroller's interrupts lines. Refer to LAN9252 datasheet for configuration of SYNC0 and SYNC1.

TIMER

SSC has a variable which will count every millisecond, which can be implemented either timer interrupt or polling method. The interrupt/polling mode can be selected in the SSC Tool before creating the slave stack code.

SSC will access EtherCAT core registers from both interrupt context and polling mode. So, the ECAT_CSR_CMD and ECAT_CSR_DATA registers hast be protected against simultaneous access which can corrupt the state machine inside the slave stack code.

For example, while reading 0x120 register, if an interrupt comes after updating 0x120 into the ECAT_CSR_CMD, then any ESC access (read/write) due to ISR routine will overwrite the ECAT_CSR_CMD register to some other content (for example, 0x220), then read data from ECAT_CSR_DATA register should be some other register data.

This can be avoided by disabling the interrupt routine while accessing any EtherCAT core register. However, any missed interrupts due to interrupt routine disable should be checked and handled in the polling mode by checking the interrupt line in between every CSR read and write operations. It is handled in LAN9252 SDK1.0 by checking the interrupt line (GPIO) after reading/writing EtherCAT core register.

The LAN9252 SDK 1.0 is compatible for PIC32MX512L. If the any other SOCs are using, then 9252_HW.C, 9252_HW.h, main.c and SPI/HBI drivers have to be modified.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
Rev. A, Sept. 2015	Initial release.	

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ISBN: 978-1-63277-770-6

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