AN4785

LAN8831 Register Definitions

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1.0 INTRODUCTION

The LAN8831 Register Definitions application note provides a description of all customer-facing registers within the LAN8831 device and is meant for clarification of functionality during design and debugging.

2.0 SECTIONS

This application note covers the following sections:

- Section 4.0, Register Maps
- Section 5.0, Register Definitions

3.0 REFERENCES

Consult the following documents for details on the specific parts referred to in this application note. The first three references include high-level descriptions intended for software design and configuration:

- *LAN8831 Data Sheet*
- *LAN8831 Hardware Design Checklist*
- *AN4746 KSZ9031MNX to LAN8831 Migration Guide*
- *AN4744 KSZ9131MNX to LAN8831 Migration Guide*

3.1 Register Nomenclature

Table 1 describes the register bit attributes used throughout this document.

TABLE 1: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents are cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents is self-cleared after the being set. Writes of zero have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After a read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read, the bit will remain high regardless of if its cause has been removed.
NASR	**Not Affected by Software Reset.** The state of NASR bits does not change on assertion of a software Reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

4.0 REGISTER MAPS

The register space within the LAN8831 consists of two distinct areas.

- Standard Registers (Direct register access)
- MDIO Manageable Device (MMD) Registers (Indirect register access)

The LAN8831 supports the following standard registers. These registers are accessed through the SMI (MDIO/MDC) interface.

TABLE 2: STANDARD REGISTERS

Index (in decimal)	Index (in hex)	Register Name
IEEE-Defined Registers		
0	0	Basic Control Register
1	1	Basic Status Register
2	2	Device Identifier 1 Register
3	3	Device Identifier 2 Register
4	4	Auto-Negotiation Advertisement Register
5	5	Auto-Negotiation Link Partner Base Page Ability Register
6	6	Auto-Negotiation Expansion Register
7	7	Auto-Negotiation Next Page TX Register
8	8	Auto-Negotiation Next Page RX Register
9	9	Auto-Negotiation Master Slave Control Register
10	Ah	Auto-Negotiation Master Slave Status Register
11-12	Bh-Ch	RESERVED
13	Dh	MMD Access Control Register
14	Eh	MMD Access Address/Data Register
15	Fh	Extended Status Register
Vendor-Specific Registers		
16	10h	RESERVED
17	11h	PCS Loopback Swap/Polarity Control Register
18	12h	LinkMD Cable Diagnostic Register
19	13h	Digital PMA/PCS Status Register
20	14h	RESERVED
21	15h	RXER Counter Register
22	16h	LED Mode Select Register
23	17h	LED Behavior Register
24	18h	RESERVED
25	19h	Output Control Register
26	1Ah	KSZ9031 LED Mode Register
27	1Bh	Interrupt Status Register
28	1Ch	Auto-MDI/MDI-X Register
29	1Dh	Software Power Down Control Register
30	1Eh	External Loopback Register
31	1Fh	Control Register

The device supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers.

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
1	225	E1h	Mean Slicer Error Register
	226	E2h	DCQ Mean Square Error Register
	227	E3h	DCQ Mean Square Error Worst Case Register
	228	E4h	DCQ SQI Register
	229	E5h	DCQ Peak MSE Register
	230	E6h	DCQ Control Register
	231	E7h	DCQ Configuration Register
	232-238	E8h-EEh	DCQ SQI Table Registers
2	0	0h	Common Control Register
	1	1h	Strap Status Register
	2	2h	Operation Mode Strap Override Register
	3	3h	Operation Mode Strap Register
	4	4h	Clock Invert and Control Signal Pad Skew Register
	5	5h	RGMII RX Data Pad Skew Register
	6	6h	RGMII TX Data Pad Skew Register
	7	7h	RESERVED
	8	8	Clock Pad Skew Register
	9	9	Self-Test Packet Count LO Register
	10	Ah	Self-Test Packet Count HI Register
	11	Bh	Self-Test Status Register
	12	Ch	Self-Test Frame Count Enable Register
	13	Dh	Self-Test PGEN Enable Register
	14	Eh	Self-Test Enable Register
	15	Fh	RESERVED
	16	10h	Wake-On-LAN Control Register
	17	11h	Wake-On-LAN-MAC-LO Register
	18	12h	Wake-On-LAN-MAC-MI Register
	19	13h	Wake-On-LAN-MAC-HI Register
	20	14h	Customized-Pkt-0-CRC-LO Register
	21	15h	Customized-Pkt-0-CRC-HI Register
	22	16h	Customized-Pkt-1-CRC-LO Register
	23	17h	Customized-Pkt-1-CRC-HI Register
	24	18h	Customized-Pkt-2-CRC-LO Register
	25	19h	Customized-Pkt-2-CRC-HI Register
	26	1Ah	Customized-Pkt-3-CRC-LO Register
	27	1Bh	Customized-Pkt-3-CRC-HI Register
	28	1Ch	Customized-Pkt-0-MASK_LL Register
	29	1Dh	Customized-Pkt-0-MASK_LH Register
	30	1Eh	Customized-Pkt-0-MASK_HL Register
	31	1Fh	Customized-Pkt-0-MASK_HH Register
	32	20h	Customized-Pkt-1-MASK_LL Register
	33	21h	Customized-Pkt-1-MASK_LH Register

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	34	22h	Customized-Pkt-1-MASK_HL Register
	35	23h	Customized-Pkt-1-MASK_HH Register
	36	24h	Customized-Pkt-2-MASK_LL Register
	37	25h	Customized-Pkt-2-MASK_LH Register
	38	26h	Customized-Pkt-2-MASK_HL Register
	39	27h	Customized-Pkt-2-MASK_HH Register
	40	28h	Customized-Pkt-3-MASK_LL Register
	41	29h	Customized-Pkt-3-MASK_LH Register
	42	2Ah	Customized-Pkt-3-MASK_HL Register
	43	2Bh	Customized-Pkt-3-MASK_HH Register
	44	2Ch	Wake-on-LAN Control Status Register
	45	2Dh	Wake-on-LAN Custom Packet Receive Status Register
	46	2Eh	Wake-on-LAN Magic Packet Receive Status Register
	47	2Fh	Wake-on-LAN Data Module Status Register
	48	30h	Customized Pkt-0 Received CRC-L Register
	49	31h	Customized Pkt-0 Received CRC-H Register
	50	32h	Customized Pkt-1 Received CRC-L Register
	51	33h	Customized Pkt-1 Received CRC-H Register
	52	34h	Customized Pkt-2 Received CRC-L Register
	53	35h	Customized Pkt-2 Received CRC-H Register
	54	36h	Customized Pkt-3 Received CRC-L Register
	55	37h	Customized Pkt-3 Received CRC-H Register
	56-59	38h-3B	RESERVED
	60	3Ch	Self-Test Correct Count LO Register
	61	3Dh	Self-Test Correct Count HI Register
	62	3Eh	Self-Test Error Count LO Register
	63	3Fh	Self-Test Error Count HI Register
	64-75	40h-4Bh	RESERVED
	76	4Ch	RX DLL Control Register
	77	4Dh	TX DLL Control Register
	78-89	4Eh-59h	RESERVED
	90	5Ah	1000M Fast Link Down Enable Register
	91-110	5Bh-6Eh	RESERVED
	111	6Fh	Driving Strength, Fast Link Down, S2P RX PCS Select Setting Register
	112-127	70h-7Fh	RESERVED
	128	80h	General Purpose IO Enable Register (GPIO_EN)
	129	81h	General Purpose IO Direction Register (GPIO_DIR)
	130	82h	General Purpose IO Buffer Type Register (GPIO_BUF)
	131	83h	General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1)
	132	84h	General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2)
	133	85h	General Purpose IO Data Register (GPIO_DATA)
	134	86h	General Purpose IO Interrupt Status Register (GPIO_INT_STS)
	135	87h	General Purpose IO Interrupt Enable Register (GPIO_INT_EN)
	136	88h	General Purpose IO Interrupt Polarity Register (GPIO_INT_POL)
	137-255	89h-FFh	RESERVED

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
3	0	0h	PCS Control 1 Register
	1	1h	PCS Status 1 Register
	2-7	2h-7h	RESERVED
	8	8h	EEE Quiet Timer Register
	9	9h	EEE Update Timer Register
	10	Ah	EEE Link-Fail Timer Register
	11	Bh	EEE Post-Update Timer Register
	12	Ch	EEE WaitWQ Timer Register
	13	Dh	EEE Wake Timer Register
	14	Eh	EEE WakeTX Timer Register
	15	Fh	EEE WakeMz Timer Register
	16-19	10h-13h	RESERVED
	20	14h	EEE Control and Capability Register
	21	15h	RESERVED
	22	16h	EEE Wake Error Counter Register
	23	17h	RESERVED
	24	18h	EEE 100 Timer-0 Register
	25	19h	EEE 100 Timer-1 Register
	26	1Ah	EEE 100 Timer-2 Register
	27	1Bh	EEE 100 Timer-3 Register
7	60	3Ch	EEE Advertisement Register
	61	3Dh	EEE Link Partner Ability Register
	62	3Eh	EEE Link Partner Ability Override Register
	63	3Fh	EEE Message Code Register
28 (1Ch)	1	1h	XTAL Control Register
	2-8	2h-8h	RESERVED
	9	9h	AFED Control Register
	10-13	Ah-Dh	RESERVED
	14	Eh	LDO Control Register
	15-35	Fh-23h	RESERVED
	36	24h	EDPD Control Register
	37	25h	EMITX Control Register
	38-52	26h-34h	EMITX Coefficient Registers

5.0 REGISTER DEFINITIONS

Register Definitions are divided into the following sections:

- Section 5.1, "Standard Registers"
- Section 5.2, "MDIO Manageable Device (MMD) Registers"

5.1 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0 to 15 (Fh)) are defined according to the IEEE specification, while the remaining 16 registers (Registers 16 (10h) to 31 (1Fh)) are defined specific to the PHY vendor.

5.1.1 BASIC CONTROL REGISTER

Index (In Decimal): 0 Size: 16 bits

This read/write register is used to configure the PHY.

Bits	Description	Type	Default
15	**PHY Soft Reset (RESET)** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software reset.	R/W1S/ SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions are not sent to network. Instead, they are looped back into the PHY. 0 = Loopback mode disabled (normal operation) 1 = Loopback mode enabled	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	0b
12	**Auto-Negotiation Enable** This bit enables/disables Auto-Negotiation. 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1] and Duplex Mode bits of this register)	R/W	1b
11	**Power Down** This bit controls the power down mode of the PHY. 0 = Normal operation 1 = General power down mode	R/W	0b

Bits	Description	Type	Default
10	**Isolate (PHY_ISO)** This bit controls the isolation of the PHY from the MII interface. 0 = Non-Isolated (Normal operation) 1 = Isolated	R/W	0b
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. This bit is self clearing. 1 = Auto-Negotiation restarted	R/W1S/ SC	0b
8	**Duplex Mode** This bit is used to set the duplex. 0 = Half Duplex 1 = Full Duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	1b
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in loopback mode. 0 = Collision test mode disabled 1 = Collision test mode enabled	R/W	0b
6	**Speed Select[1]** See description for Speed Select[0] for details.	R/W	1b
5:0	**RESERVED**	R/W	—

5.1.2 BASIC STATUS REGISTER

Index (In Decimal): 1 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. 0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0b
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. 0 = PHY not able to perform 100BASE-X full duplex 1 = PHY able to perform 100BASE-X full duplex	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. 0 = PHY not able to perform 100BASE-X half duplex 1 = PHY able to perform 100BASE-X half duplex	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. 0 = PHY not able to perform 10BASE-T full duplex 1 = PHY able to perform 10BASE-T full duplex	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. 0 = PHY not able to perform 10BASE-T half duplex 1 = PHY able to perform 10BASE-T half duplex	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. 0 = PHY not able to perform 100BASE-T2 full duplex 1 = PHY able to perform 100BASE-T2 full duplex	RO	0b
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. 0 = PHY not able to perform 100BASE-T2 half duplex 1 = PHY able to perform 100BASE-T2 half duplex	RO	0b
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). 0 = No extended status information in Register 15 1 = Extended status information in Register 15	RO	1b

Bits	Description	Type	Default
7	**Unidirectional Ability** This bit indicates whether the PHY is able to transmit regardless of whether the PHY has determined that a valid link has been established. 0 = Can only transmit when a valid link has been established 1 = Can transmit regardless	RO	0b
6	**MF Preamble Suppression** This bit indicates whether the PHY accepts management frames with the preamble suppressed. 0 = Management frames with preamble suppressed not accepted 1 = Management frames with preamble suppressed accepted	RO	1b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. 0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0b
3	**Auto-Negotiation Ability** This bit indicates the PHY's Auto-Negotiation ability. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	RO	1b
2	**Link Status** This bit indicates the status of the link. 0 = Link is down 1 = Link is up	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. 0 = No jabber condition detected 1 = Jabber condition detected	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. 0 = Basic register set capabilities only 1 = Extended register set capabilities	RO	1b

5.1.3 DEVICE IDENTIFIER 1 REGISTER

Index (In Decimal): 2 Size: 16 bits

This register contains the MSB of the Organizationally Unique Identifier (OUI) for the PHY. The LSB of the PHY OUI is contained in the Device Identifier 2 Register.

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022h

5.1.4 DEVICE IDENTIFIER 2 REGISTER

Index (In Decimal): 3 Size: 16 bits

This register contains the LSB of the Organizationally Unique Identifier (OUI) for the PHY. The MSB of the PHY OUI is contained in the Device Identifier 1 Register.

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	000101b
9:4	**Model Number** Six-bit manufacturer's model number.	RO	100101b
3:0	**Revision Number** Four-bit manufacturer's revision number.	RO	Note 5-1

Note 5-1 The default value of the Revision Number field varies dependent on the silicon revision number.

Note: The hexadecimal equivalent of this register is 165xh.

5.1.5 AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Index (In Decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the PHY and is used in the Auto-Negotiation process with the link partner.

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. 0 = Remote fault indication not advertised 1 = Remote fault indication advertised	R/W	0b
12	**Extended Next Page** **Note:** This bit should be written as 0.	RO	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner advertised 1 = Asymmetric PAUSE toward link partner advertised	R/W	1b
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. 0 = No Symmetric PAUSE toward link partner advertised 1 = Symmetric PAUSE toward link partner advertised	R/W	1b
9	**100BASE-T4** 0 = no T4 ability 1 = T4 able **Note:** The device does not support this mode and this bit should always be written as a 0.	RO	0
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not advertised 1 = 100BASE-X full duplex ability advertised	R/W	Note 5-2
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not advertised 1 = 100BASE-X half duplex ability advertised	R/W	Note 5-2

Bits	Description	Type	Default
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not advertised 1 = 10BASE-T full duplex ability advertised	R/W	Note 5-2
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not advertised 1 = 10BASE-T half duplex ability advertised	R/W	Note 5-2
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	R/W	00001b

Note 5-2 Set by the MODE[3:0] strapping pins.

5.1.6 AUTO-NEGOTIATION LINK PARTNER BASE PAGE ABILITY REGISTER

Index (In Decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15	**Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	RO	0b
12	**Extended Next Page** 0 = Link partner PHY does not advertise extended next page capability 1 = Link partner PHY advertises extended next page capability	RO	0b
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner 1 = Asymmetric PAUSE toward link partner	RO	0b

Bits	Description	Type	Default
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. 0 = No Symmetric PAUSE toward link partner 1 = Symmetric PAUSE toward link partner	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. 0 = 100BASE-T4 ability not supported 1 = 100BASE-T4 ability supported	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not supported 1 = 100BASE-X full duplex ability supported	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not supported 1 = 100BASE-X half duplex ability supported	RO	0b
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not supported 1 = 10BASE-T full duplex ability supported	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not supported 1 = 10BASE-T half duplex ability supported	RO	0b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	RO	00000b

5.1.7 AUTO-NEGOTIATION EXPANSION REGISTER

Index (In Decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**Receive Next Page Location Able** 0 = Received next page storage location is not specified by bit 6.5 1 = Received next page storage location is specified by bit 6.5	RO	1b
5	**Received Next Page Storage Location** 0 = Link partner next pages are stored in the Auto-Negotiation Link Partner Base Page Ability Register (PHY register 5) 1 = Link partner next pages are stored in the Auto-Negotiation Next Page RX Register (PHY register 8)	RO	1b
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. 0 = A fault hasn't been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. 0 = Link partner does not contain next page capability 1 = Link partner contains next page capability	RO	0b
2	**Next Page Able** This bit indicates whether the local device has next page ability. 0 = Local device does not contain next page capability 1 = Local device contains next page capability	RO	1b
1	**Page Received** This bit indicates the reception of a new page. 0 = A new page has not been received 1 = A new page has been received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-Negotiation ability of the link partner. 0 = Link partner is not Auto-Negotiation able 1 = Link partner is Auto-Negotiation able	RO	0b

5.1.8 AUTO-NEGOTIATION NEXT PAGE TX REGISTER

Index (In Decimal): 7 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Message Page** 0 = Unformatted page 1 = Message page	R/W	1b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	R/W	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	R/W	000 0000 0001b

5.1.9 AUTO-NEGOTIATION NEXT PAGE RX REGISTER

Index (In Decimal): 8 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0
13	**Message Page** 0 = Unformatted page 1 = Message page	RO	0b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	RO	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RO	000 0000 0000b

5.1.10 AUTO-NEGOTIATION MASTER SLAVE CONTROL REGISTER

Index (In Decimal): 9 Size: 16 bits

Bits	Description	Type	Default
15:13	**Test Mode** IEEE 802.3 clause 40.6.1.1.2 transmitter test mode. 000 = Normal mode 001 = Test Mode 1 - Transmit waveform test 010 = Test Mode 2 - Transmit jitter test in Master mode 011 = Test Mode 3 - Transmit jitter test in Slave mode 100 = Test Mode 4 - Transmitter distortion test 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000b
12	**Master/Slave Manual Configuration Enable** 0 = disable MASTER-SLAVE manual configuration value 1 = enable MASTER-SLAVE manual configuration value	R/W	0b
11	**Master/Slave Manual Configuration Value** Active only when the Master/Slave Manual Configuration Enable bit of this register is 1. 0 = Configure PHY as slave 1 = Configure PHY as master	R/W	0b
10	**Port Type** 0 = single-port device 1 = multi-port device	R/W	0b
9	**1000BASE-T Full Duplex** 0 = advertise PHY is not 1000BASE-T full duplex capable 1 = advertise PHY is 1000BASE-T full duplex capable	R/W	1b
8	**1000BASE-T Half Duplex** 0 = advertise PHY is not 1000BASE-T half duplex capable 1 = advertise PHY is 1000BASE-T half duplex capable **Note:** The device does not support this mode and this bit should always be written as a 0.	R/W	0b
7:0	**RESERVED**	RO	—

5.1.11 AUTO-NEGOTIATION MASTER SLAVE STATUS REGISTER

Index (In Decimal): 10 Size: 16 bits

Bits	Description	Type	Default
15	**Master/Slave Configuration Fault** 0 = No MASTER-SLAVE configuration fault detected 1 = MASTER-SLAVE configuration fault detected	RO/LH	0b
14	**Master/Slave Configuration Resolution** 0 = Local PHY configuration resolved to SLAVE 1 = Local PHY configuration resolved to MASTER	RO	0b
13	**Local 1000BASE-T Receiver Status** 0 = Local Receiver not OK 1 = Local Receiver OK	RO	0b
12	**Remote (Link Partner) Receiver Status** 0 = Remote Receiver not OK 1 = Remote Receiver OK	RO	0b
11	**Link Partner Advertised 1000BASE-T Full Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex	RO	0b
10	**Link Partner Advertised 1000BASE-T Half Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex	RO	0b
9:8	**RESERVED**	RO	—
7:0	**1000BASE-T Idle Error Count** Cumulative count of the errors detected when the receiver is receiving idles. **Note:** This counter halts at a value of 0xFF.	RO/RC	00h

5.1.12 MMD ACCESS CONTROL REGISTER

Index (In Decimal): 13 Size: 16 bits

Bits	Description	Type	Default
15:14	**MMD Function** This field is used to select the desired MMD function: 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	—
4:0	**MMD Device Address (DEVAD)** This field is used to select the desired MMD device address.	R/W	00000b

5.1.13 MMD ACCESS ADDRESS/DATA REGISTER

Index (In Decimal): 14 Size: 16 bits

Bits	Description	Type	Default
15:0	**MMD Register Address/Data** If the MMD Function field of the MMD Access Control Register is “00”, this field is used to indicate the MMD register address to read/write of the device specified in the MMD Device Address (DEVAD) field. Otherwise, this register is used to read/write data from/to the previously specified MMD address.	R/W	0000h

5.1.14 EXTENDED STATUS REGISTER

Index (In Decimal): 15 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**1000BASE-X Full Duplex** This bit displays the status of 1000BASE-X full duplex compatibility. 0 = PHY not able to perform 1000BASE-X full duplex 1 = PHY able to perform 1000BASE-X full duplex	RO	0b
14	**1000BASE-X Half Duplex** This bit displays the status of 1000BASE-X half duplex compatibility. 0 = PHY not able to perform 1000BASE-X half duplex 1 = PHY able to perform 1000BASE-X half duplex	RO	0b
13	**1000BASE-T Full Duplex** This bit displays the status of 1000BASE-T full duplex compatibility. 0 = PHY not able to perform 1000BASE-T full duplex 1 = PHY able to perform 1000BASE-T full duplex	RO	1b
12	**1000BASE-T Half Duplex** This bit displays the status of 1000BASE-T half duplex compatibility. 0 = PHY not able to perform 1000BASE-T half duplex 1 = PHY able to perform 1000BASE-T half duplex	RO	0b
11:0	**RESERVED**	RO	—

5.1.15 PCS LOOPBACK SWAP/POLARITY CONTROL REGISTER

Index (In Decimal): 17 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**Remote Loopback** 1 = Enable remote loopback 0 = Disable remote loopback	R/W	0b
7:6	**mr_led_sel** See Table 5-13 in the *LAN8831 Data Sheet*.	R/W	11b
5:3	**RESERVED**	RO	—
2	**10BASE-T Preamble Enable** 1 = Enable 10BASE-T Preamble for Loopback 0 = Disable 10BASE-T Preamble for Loopback	R/W	0b

Bits	Description	Type	Default
1:0	**RESERVED**	RO	—

5.1.16 LINKMD CABLE DIAGNOSTIC REGISTER

Index (In Decimal): 18 Size: 16 bits

Bits	Description	Type	Default
15	**Cable Diagnostics Test Enable (VCT_EN)** Writing a 1 enables the test. This bit is self-cleared when the test is complete. Writing a 0 will disable the test. Reading a 0 indicates the cable diagnostic test is completed and the status information is valid. Reading a 1 indicates the cable diagnostic test is in progress and the status information is NOT valid.	R/W/SC	0b
14	**Cable Diagnostic Disable Transmitter (VCT_DIS_TX)** [0] = The transmitter is enabled to start cable diagnostic. [1] = The transmitter is disabled and cable diagnostic is on hold to break down the link.	R/W	0b
13:12	**Cable Diagnostics Test Pair (VCT_PAIR[1:0])** This field defines which channel to be tested. 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D	R/W	00b
11:10	**RESERVED**	R/W	00b
9:8	**Cable Diagnostics Status (VCT_ST[1:0])** Valid only when VCT_EN = 0. 00 = Normal, no fault has been detected 01 = Open Fault has been detected 10 = Short Fault has been detected 11 = Cable diagnostic test failed	RO	00b

Bits	Description	Type	Default
7:0	**Cable Diagnostics Data or Threshold (VCT_DATA[7:0])** This is the data of cable diagnostics. Valid only when VCT_EN = 0. (1) If cable is normal, i.e., VCT_ST = 00, VCT_DATA don't care. (2) If cable is open or short, i.e., VCT_ST = 01 or 10, the distance to fault is approximately 0.8 * (VCT_DATA - 22) (Meters) (3) If cable diagnostics failed, i.e., VCT_ST = 11, Bit[7] = 1 means invalid reflected pulse width, i.e. equal or greater than 152ns, equal or less than 48ns. Bit[6] = 1 means cable has signal for too long time during WAIT state. It's unusual and for debug only. Bit[5] = 1 means mask100 detected and no silent time window can be found for diagnostics. It means high frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. Bit[4] = 1 means signals faster than NLP and FLP exists and no silent time window can be found for diagnostics. It's unusual and for debug only. Bit[3:2] = number of low pulses detected. If more than 3, stay at 3. Bit[1:0] = number of high pulses detected. If more than 3, stay at 3.	RO	00h

5.1.17 DIGITAL PMA/PCS STATUS REGISTER

Index (In Decimal): 19 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**1000BT link status** 1000 BT link status 1 = link status OK 0 = link status not OK	RO	0b
0	**100BT link status** 100 BT link status 1 = link status OK 0 = link status not OK	RO	0b

5.1.18 RXER COUNTER REGISTER

Index (In Decimal): 21 Size: 16 bits

Bits	Description	Type	Default
15:0	**RXER Counter** RX Error counter for the RX_ER signal **Note:** This counter halts at a value of 0xFFFF.	RC	0000h

5.1.19 LED MODE SELECT REGISTER

Index (In Decimal): 22 Size: 16 bits

This register selects the operating mode of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15:12	**LED4 Configuration** This field configures the LED4 pin function. Refer to Table 4 for definitions.	R/W	1000b
11:8	**LED3 Configuration** This field configures the LED3 pin function. Refer to Table 4 for definitions.	R/W	0000b
7:4	**LED2 Configuration** This field configures the LED2 pin function. Refer to Table 4 for definitions.	R/W	0010b
3:0	**LED1 Configuration** This field configures the LED1 pin function. Refer to Table 4 for definitions.	R/W	0001b

TABLE 4: LED MODE AND FUNCTION SUMMARY

Mode	Name	Description
0	Link/Activity	1 (led off) = No link in any speed on any media interface. 0 (led on) = Valid link at any speed on any media interface. Blink or pulse stretch (led turns off) = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 (led off) = No link at 1000BASE-T. 0 (led on) = Valid link at 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 1000BASE-T with activity present.
2	Link100/Activity	1 (led off) = No link at 100BASE-TX. 0 (led on) = Valid link at 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX with activity present.
3	Link10/Activity	1 (led off) = No link at 10BASE-T. 0 (led on) = Valid link at 10BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T with activity present.
4	Link100/1000/Activity	1 (led off) = No link at 100BASE-TX or 1000BASE-T. 0 (led on) = Valid link at 100BASE-TX or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX or 1000BASE-T, with activity present.
5	Link10/1000/Activity	1 (led off) = No link at 10BASE-T or 1000BASE-T. 0 (led on) = Valid link at 10BASE-T or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 1000BASE-T, with activity present.

TABLE 4: LED MODE AND FUNCTION SUMMARY (CONTINUED)

Mode	Name	Description
6	Link10/100/Activity	1 (led off) = No link at 10BASE-T or 100BASE-TX. 0 (led on) = Valid link at 10BASE-T or 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 100BASE-TX, with activity present.
7	RESERVED	RESERVED
8	Duplex/Collision	1 (led off) = Link established in half-duplex mode, or no link established. 0 (led on) = Link established in full-duplex mode. Blink or pulse stretch (led turns on) = Link established in half-duplex mode but collisions are present.
9	Collision	1 (led off) = No collisions detected. Blink or pulse stretch (led turns on) = Collision detected.
10	Activity	1 (led off) = No activity present. Blink or pulse stretch (led turns on) = Activity present. (becomes TX activity present if the LED Activity Output Select bit in the LED Behavior Register is set to 1.)
11	RESERVED	RESERVED
12	Auto-Negotiation Fault	1 (led off) = No Auto-Negotiation fault present. 0 (led on) = Auto-Negotiation fault occurred.
13	RESERVED	RESERVED
14	Force LED Off	1 (led off) = De-asserts the LED.
15	Force LED On	0 (led on) = Asserts the LED.

5.1.20 LED BEHAVIOR REGISTER

Index (In Decimal): 23 Size: 16 bits

This register selects the operating parameters of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15	**RESERVED**	R/W	—
14	**LED Activity Output Select**	R/W	0b
13	**RESERVED**	R/W	—
12	**LED Pulsing Enable**	R/W	1b
11:10	**LED Blink / Pulse-Stretch Rate** 00 = 2.5 Hz Blink Rate / 400 ms pulse-stretch 01 = 5 Hz Blink Rate / 200 ms pulse-stretch 10 = 10 Hz Blink Rate / 100 ms pulse-stretch 11 = 20 Hz Blink Rate / 50 ms pulse-stretch	R/W	00b
9	**RESERVED**	R/W	—
8:5	**LED Pulse Stretch Enables** Configures LED4 (bit 8), LED3 (bit 7), LED2 (bit 6) and LED1 (bit 5) to either pulse-stretch when 1, or blink when 0.	R/W	0000b

Bits	Description	Type	Default
4	**RESERVED**	R/W	—
1:0	**LED Combination Disables** Configures LED4 (bit 3), LED3 (bit 2), LED2 (bit 1) and LED1 (bit 0) to either combine link/activity and duplex/collision when 0, or disable combination, providing link-only and duplex-only when 1.	R/W	0000b

5.1.21 OUTPUT CONTROL REGISTER

Index (In Decimal): 25 Size: 16 bits

This register selects the output buffer type and polarity of the INT_N, MDIO and LED pins.

Bits	Description	Type	Default
15	**MDIO Buffer Type** When set to a 0, the MDIO output is open-drain When set to a 1, the MDIO output is push-pull	R/W	0b
14	**INT Buffer Type** When set to a 0, the INT_N output is open-drain When set to a 1, the INT_N output is push-pull **Note:** If the buffer type is set to open-drain, INT_N is always active low.	R/W	0b
13:8	**LED Buffer Type** When set to a 0, the LED pins are open-drain or open-source When set to a 1, the LED pins are push-pull **Bit 8 is for LED1, bit 9 for LED2, etc.**	R/W	000000b
7	**PME Polarity** When set to a 0, the PME_N pin is active low When set to a 1, the PME_N pin is active high	R/W	0b
6	**RESERVED**	R/W	—
5:0	**LED Polarity** When set to a 0, the LED pins are active low When set to a 1, the LED pins are active high Bit 0 is for LED1, bit 1 is for LED2, etc.	RO	Note 1

Note 1: Set by the inverse of the LEDPOL configuration straps.

5.1.22 KSZ9031 LED MODE REGISTER

Index (In Decimal): 26 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	R/W	—
14	**KSZ9031 LED Mode** 1 = KSZ9031 LED mode 0 = Extended LED mode **Note:** For normal LED operation, this bit should always be written as a 1.	R/W	1b
13:0	**RESERVED**	R/W	—

5.1.23 INTERRUPT STATUS REGISTER

Index (In Decimal): 27 Size: 16 bits

Reading this register clears the RC interrupt sources. RO sources must be cleared at their lower level register.

Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	—
11	**Energy Not Detected Interrupt** 1 = “Energy not detected” interrupt 0 = No “energy not detected” interrupt This bit is set when the EDPD Low Power bit in the EDPD Control Register changes from 1 to 0.	RC	0b
10	**Energy Detected Interrupt** 1 = “Energy detected” interrupt 0 = No “energy detected” interrupt This bit is set when the EDPD Low Power bit in the EDPD Control Register changes from 0 to 1.	RC	0b
9	**RESERVED**	RO	—
8	**GPIO Interrupt** Indicates an interrupt generated from the GPIOs. This bit is set whenever any enabled bits in the General Purpose I/O Interrupt Status Register (GPIO_INT_STS) are set. **Note:** The sources for these interrupts are level. The interrupt persists until the bits in the GPIO controller are cleared or disabled. 1 = GPIO interrupt 0 = No GPIO interrupt	RO	0b

Bits	Description	Type	Default
7	**Jabber Interrupt** 1 = Jabber interrupt 0 = No jabber interrupt	RC	0b
6	**Receive Error Interrupt** 1 = Receive error interrupt 0 = No receive error interrupt	RC	0b
5	**Page Receive Interrupt** 1 = Page receive interrupt 0 = No page receive interrupt	RC	0b
4	**Parallel Detect Fault Interrupt** 1 = Parallel detection fault interrupt 0 = No parallel detection fault interrupt	RC	0b
3	**Link Partner Acknowledge Interrupt** 1 = Link partner acknowledge interrupt 0 = No link partner acknowledge interrupt	RC	0b
2	**Link Down Interrupt** 1 = Link down interrupt 0 = No link down interrupt	RC	0b
1	**ADC FIFO Error Interrupt** 1 = ADC FIFO Error interrupt 0 = No ADC FIFO Error interrupt	RC	0b
0	**Link Up Interrupt** 1 = Link up interrupt 0 = No link up interrupt	RC	0b

5.1.24 AUTO-MDI/MDI-X REGISTER

Index (In Decimal): 28 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7	**MDI Set** When the Swap-Off bit of this register is asserted (1), 1 = PHY is set to operate in MDI mode 0 = PHY is set to operate in MDI-X mode	R/W	0b
6	**Swap-Off** 1 = Disable Auto-MDI/MDI-X function 0 = Enable Auto-MDI/MDI-X function	R/W	0b
5:0	**RESERVED**	RO	—

5.1.25 SOFTWARE POWER DOWN CONTROL REGISTER

Index (In Decimal): 29 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	—
11	**spd_clock_gate_override** 0 = internal clocks are gated during the Software Power Down (SPD) mode. 1 = internal clock gating is overridden during the SPD mode.	R/W	0b
10	**spd_pll_disable** 0 = PLL is enabled during the Software Power Down (SPD) mode. 1 = PLL is disabled during the SPD mode.	R/W	0b
9:8	**RESERVED**	R/W	—
7	**IO_DC_test_en** 1 = enable IO test	R/W	0b
6	**VOH** 1 = “VDD” to output IO 0 = “GND” to IO	R/W	0b

5.1.26 EXTERNAL LOOPBACK REGISTER

Index (In Decimal): 30 Size: 16 bits

Bits	Description	Type	Default
15:4	**RESERVED**	R/W	—
3	**Ext_lpbk** External loopback enable	R/W	0b
2:0	**RESERVED**	R/W	—

5.1.27 CONTROL REGISTER

Index (In Decimal): 31 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Interrupt Polarity Invert** 1 = invert 0 = normal	R/W	0b
13:10	**RESERVED**	RO	—
9	**Enable Jabber** 1 = Enable jabber counter 0 = Disable	R/W	1b
8	**Enable SQE Test** 1 = Enable SQE test 0 = Disable	R/W	1b
7	**RESERVED**	RO	—
6	**Speed status 1000T** Indicates speed is 1000T	RO	0b
5	**Speed status 100TX** Indicates speed is 100TX	RO	0b
4	**Speed status 10BT** Indicates speed is 10BT	RO	0b
3	**Duplex status** Indicates duplex status	RO	0b
2	**1000BASE-T Mater/Slave status** 1 = Indicates 1000BASE-T Master mode 0 = Indicates 1000BASE-T Slave mode	RO	0b
1	**Software Reset** 1 = Reset PHY except all registers 0 = Disable reset	W1S/RC	0b
0	**Link Status Check Fail** 1 = Fail 0 = Not Failing	RC	0b

5.2 MDIO Manageable Device (MMD) Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. This device, however, uses only a small fraction of the available registers. See Table 3 for a list of supported MMD device addresses and their associated register addresses. These registers are accessed through the SMI (MDIO/MDC) interface.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- MMD Access Control Register
- MMD Access Address/Data Register

Example: MMD Register Write

Write MMD - Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0010h // Set address register = 10h.
3. Write the MMD Access Control Register with 4002h // Select data register for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

Example: MMD Register Read

Read MMD - Device Address 3h, Register 14h EEE Control and Capability.

1. Write the MMD Access Control Register with 0003h // Select address register for MMD – Device Address 3h.
2. Write the MMD Access Address/Data Register with 0014h // Set address register = 14h.
3. Write the MMD Access Control Register with 4003h // Select data register for MMD – Device Address 3h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 3h, Register 14h.

It is also possible to automatically increment the register address for reads and/or writes

Example: MMD Register Writes with Post Increment

Write MMD - Device Address 2h, Register 11h – 13h = 0123_4567_89ABh for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h or C002h // Select data register with post increment for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0123h // Write value 0123h to MMD – Device Address 2h, Register 11h.
5. Write the MMD Access Address/Data Register with 4567h // Write value 4567h to MMD – Device Address 2h, Register 12h.
6. Write the MMD Access Address/Data Register with 89ABh // Write value 89ABh to MMD – Device Address 2h, Register 13h.

Example: MMD Register Reads with Post Increment

Read MMD - Device Address 2h, Register 11h – 13h for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h // Select data register with post increment for MMD – Device Address 2h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 11h.
5. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 12h.
6. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 13h.

5.2.1 MEAN SLICER ERROR REGISTER

Index (In Decimal): 1.225 Size: 16 bits

Bits	Description	Type	Default
15:0	**Mean Slicer Error** This field provides the current mean error value. Either absolute or square mode values can be provided. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0000h

5.2.2 DCQ MEAN SQUARE ERROR REGISTER

Index (In Decimal): 1.226 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**MSE Value Valid** This field provides the mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Value** This field provides the current mean square error value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

5.2.3 DCQ MEAN SQUARE ERROR WORST CASE REGISTER

Index (In Decimal): 1.227 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**MSE Worst Case Value Valid** This field provides the worst case mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Worst Case Value** This field provides the worst case mean square error value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

5.2.4 DCQ SQI REGISTER

Index (In Decimal): 1.228 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:5	**SQI Worst Case** This field indicates the worst case SQI value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
4	**RESERVED**	RO	—

Bits	Description	Type	Default
3:1	**SQI** This field indicates the current SQI value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
0	**RESERVED**	RO	—

5.2.5 DCQ PEAK MSE REGISTER

Index (In Decimal): 1.229 Size: 16 bits

Bits	Description	Type	Default
15:8	**Peak MSE Worst Case** This field indicates the worst case peak MSE value since the last time the channel was captured for reading. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h
7:0	**Peak MSE Value** This field provides the current peak MSE value. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h

5.2.6 DCQ CONTROL REGISTER

Index (In Decimal): 1.230 Size: 16 bits

Bits	Description	Type	Default
15	**DCQ Read Capture** When this bit is set the DCQ values are captured.	R/W/SC	0b
14:2	**RESERVED**	R/W	—
1:0	**DCQ Channel Number** This field specifies which channel's (wire pair) values are captured into the DCQ registers. 00 = Channel A 01 = Channel B 10 = Channel C 11 = Channel D **Note:** Channel A is used for both 100BASE-TX and 1000BASE-T. Channels B-D are only used for 1000BASE-T.	R/W	00b

5.2.7 DCQ CONFIGURATION REGISTER

Index (In Decimal): 1.231 Size: 16 bits

Bits	Description	Type	Default
15:14	**scale613** Scaling factor for SQI method 5 (TC1 peak MSE).	R/W	00b
13:10	**sqi_kp3** LPF bandwidth control.for SQI method 5 (TC1 peak MSE).	R/W	101b
9:8	**scale611** Scaling factor for SQI methods 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	00b
7	**sqi_reset** When set the SQI logic is reset. **Note:** This bit does not self-clear.	R/W	0b
6	**sqi_squ_mode_en** 0 = Absolute mode 1 = Square mode	R/W	1b
5	**sqi_enable** When set SQI measurements are enabled.	R/W	1b
4:0	**sqi_kp** LPF bandwidth control.for SQI methods 2 (non TC1 LPF mean), 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	0Dh

5.2.8 DCQ SQI TABLE REGISTERS

Index (In Decimal): 1.232-238 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**SQI_VALUE** Lookup table utilized for implement of SQI method 4 (TC1 SQI). These registers set the thresholds to map the error value to a SQI level.	R/W	Table 5

TABLE 5: SQI VALUE DEFAULTS

Register	Default (Hexadecimal)
SQI_TBL1.SQI_VALUE	A3h
SQI_TBL2.SQI_VALUE	82h
SQI_TBL3.SQI_VALUE	67h
SQI_TBL4.SQI_VALUE	52h
SQI_TBL5.SQI_VALUE	41h
SQI_TBL6.SQI_VALUE	34h
SQI_TBL7.SQI_VALUE	29h

5.2.9 COMMON CONTROL REGISTER

Index (In Decimal): 2.0 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Single LED** 1 = Individual-LED mode 0 = Tri-color-LED mode By default, this bit reflects the value of the LED_MODE strapping pin. If written as a 1, the value of the LED_MODE strapping pin is overridden and Single-LED mode is selected.	R/W	Note 5-3
3:2	**RESERVED**	R/W	—
1	**clk125 Enable** A 1 enables the 125 MHz clock output onto the CLK125_NDO pin.	R/W	Note 5-4
0	**All-PHYAD Enable** When this bit is set, the PHY will respond to PHY address 0 as well as it's assigned PHY address.	R/W	Note 5-5

Note 5-3 Set by the LED_MODE strapping pin.

Note 5-4 Set by the CLK125_EN strapping pin.

Note 5-5 Set by the inverse of the ALLPHYAD strapping pin.

5.2.10 STRAP STATUS REGISTER

Index (In Decimal): 2.1 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**LEDPOLx Strap-In Status** Strap status of LED polarities 0 = Active low 1 = Active high	RO	Note 5-6
7	**LED_MODE Strap-In Status** 1 = Individual LED mode 0 = Tri-color LED mode	RO	Note 5-7
6	**RESERVED**	RO	—
5	**CLK125_EN Strap-In Status** 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RO	Note 5-8
4:0	**PHYAD[2:0] Strap-In Status** Strap-in value for PHY address **Note:** Bits [4:3] of PHY address are always set to '00'.	RO	Note 5-9

Note 5-6 Set by the inverse of the LEDPOL6 through LEDPOL1 strapping pins.

Note 5-7 Set by the LED_MODE strapping pin.

Note 5-8 Set by the CLK125_EN strapping pin.

Note 5-9 Set by the PHYAD[2:0] strapping pins.

5.2.11 OPERATION MODE STRAP OVERRIDE REGISTER

Index (In Decimal): 2.2 Size: 16 bits

This register may be used to override the value of the MODE[4:0], RGMII_EN, and MAGJACK configuration straps.

Following an update to this register, a PHY Soft Reset (RESET) should be issued into the Basic Control Register in order for the new value to take effect.

APPLICATION NOTE: When setting a new value, it is the user's responsibility to ensure that conflicting assignments are not made.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**MagJack_mode** Forced MagJack mode 1 = Forced MagJack mode	R/W NASR	Note 5-10
13	**1000_FD_slave_mode** Forced 1000BASE-T full duplex slave mode 1 = Forced 1000BT FD slave mode	R/W NASR	Note 5-12
12	**100_HD_mode** Forced 100BASE-TX half duplex mode 1 = Forced 100BT HD mode	R/W NASR	Note 5-12
11	**100_FD_mode** Forced 100BASE-TX full duplex mode 1 = Forced 100BT FD mode	R/W NASR	Note 5-12
10	**1000_FD_master_mode** Forced 1000BASE-T full duplex master mode 1 = Forced 1000BT FD master mode	R/W NASR	Note 5-12
9	**spd_pll_dis_mode** Software Power Down with PLL disabled mode 1 = SPD w/pll disabled mode	R/W NASR	Note 5-12
8	**spd_pll_en_mode** Software Power Down with PLL enabled mode 1 = SPD w/pll enable mode	R/W NASR	Note 5-12
7	**iddq_scan_mode** IDDQ scan mode 1 = IDDQ scan mode	RO NASR	Note 5-12
6:5	**RESERVED**	RO	—
4	**ntree_mode** NAND Tree mode 1 = NAND Tree mode	R/W NASR	Note 5-12
3:2	**RESERVED**	RO	—
1	**gmii_mode** GMII/MII mode 1 = GMII/MII mode	R/W NASR	Note 5-13

Bits	Description	Type	Default
0	**rgmii_mode** RGMII mode 1 = RGMII mode	R/W NASR	Note 5-14

Note 5-10 Set by the MAGJACK strapping pin as indicated by the corresponding but in the Operation Mode Strap Register.

Note 5-11 Writable to a 1 if scan_mode is set and Strap_iddq_scan_mode is clear in the Operation Mode Strap Register.

Note 5-12 Set by the MODE[4:0] strapping pins.

Note 5-13 Set by the inverse of the RGMII_EN strapping pin.

Note 5-14 Set by the RGMII_EN strapping pin.

5.2.12 OPERATION MODE STRAP REGISTER

Index (In Decimal): 2.3 Size: 16 bits

This register indicates the value of the MODE[4:0], RGMII_EN, and MAGJACK configuration straps that were latched into the device at reset.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Strap_magjack_mode** MagJack Strap-In Status 1 = MagJack mode	RO	Note 5-15
13	**Strap_1000_FD_slave_mode** Forced 1000BASE-T full duplex slave Strap-In Status 1 = Forced 1000BT FD slave mode (MODE[4:0]='01101')	RO	Note 5-16
12	**Strap_100_HD_mode** Forced 100BASE-TX half duplex Strap-In Status 1 = Forced 100BT HD mode (MODE[4:0]='01100')	RO	Note 5-16
11	**Strap_100_FD_mode** Forced 100BASE-TX full duplex Strap-In Status 1 = Forced 100BT FD mode (MODE[4:0]='01011')	RO	Note 5-16
10	**Strap_1000_FD_master_mode** Forced 1000BASE-T full duplex master Strap-In Status 1 = Forced 1000BT FD master mode (MODE[4:0]='01010')	RO	Note 5-16
9	**Strap_spd_pll_dis_mode** Software Power Down with PLL disabled Strap-In Status 1 = SPD w/pll disabled mode (MODE[4:0]='01001')	RO	Note 5-16
8	**Strap_spd_pll_en_mode** Software Power Down with PLL enabled Strap-In Status 1 = SPD w/pll enable mode (MODE[4:0]='01000')	RO	Note 5-16
7	**Strap_iddq_scan_mode** IDDQ Scan Strap-In Status 1 = IDDQ scan mode (MODE[4:0]='00111')	RO	Note 5-16
6:5	**RESERVED**	RO	—

Bits	Description	Type	Default
4	**Strap_ntree_mode** NAND Tree Strap-In Status 1 = NAND Tree mode (MODE[4:0]='00100')	RO	Note 5-16
3:2	**RESERVED**	RO	—
1	**Strap_gmii_mode** GMII/MII mode Strap-In status 1 = Strapped to GMII/MII mode	RO	Note 5-17
0	**Strap_rgmii_mode** RGMII mode Strap-In status 1 = Strapped to RGMII mode	RO	Note 5-18

Note 5-15 Set by the MAGJACK strapping pin as indicated by the corresponding but in the Operation Mode Strap Register.

Note 5-16 Set by the MODE[3:0] strapping pins.

Note 5-17 Set by the inverse of the RGMII_EN strapping pin.

Note 5-18 Set by the RGMII_EN strapping pin.

5.2.13 CLOCK INVERT AND CONTROL SIGNAL PAD SKEW REGISTER

Index (In Decimal): 2.4 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	R/W	0h
9	**Inverse GMII RX_CLK Input** 0 = no change 1 = inverse on RX_CLK for GMII	R/W	0b
8	**Inverse RGMII TXC Input** 0 = no change 1 = inverse on TXC for RGMII	R/W	0b
7:4	**RX_DV/RX_CTL Skew** RX_DV/RX_CTL output skew Control (0.1 ns/step)	R/W	7h
3:0	**TX_EN/TX_CTL Skew** TX_EN/TX_CTL input skew Control (0.1 ns/step)	R/W	7h

5.2.14 RGMII RX DATA PAD SKEW REGISTER

Note: This field will also affect the device in GMII mode, therefore the it should not be changed from its default value.

Index (In Decimal): 2.5 Size: 16 bits

Bits	Description	Type	Default
15:12	**RXD3 Pad Skew** RGMII RXD3 output pad skew control (0.1 ns/step)	R/W	7h
11:8	**RXD2 Pad Skew** RGMII RXD2 output pad skew control (0.1 ns/step)	R/W	7h
7:4	**RXD1 Pad Skew** RGMII RXD1 output pad skew control (0.1 ns/step)	R/W	7h
3:0	**RXD0 Pad Skew** RGMII RXD0 output pad skew control (0.1 ns/step)	R/W	7h

5.2.15 RGMII TX DATA PAD SKEW REGISTER

Note: This field will also affect the device in GMII mode, therefore the it should not be changed from its default value.

Index (In Decimal): 2.6 Size: 16 bits

Bits	Description	Type	Default
15:12	**TXD3 Pad Skew** RGMII TXD3 output pad skew control (0.1 ns/step)	R/W	7h
11:8	**TXD2 Pad Skew** RGMII TXD2 output pad skew control (0.1 ns/step)	R/W	7h
7:4	**TXD1 Pad Skew** RGMII TXD1 output pad skew control (0.1 ns/step)	R/W	7h
3:0	**TXD0 Pad Skew** RGMII TXD0 output pad skew control (0.1 ns/step)	R/W	7h

5.2.16 CLOCK PAD SKEW REGISTER

Index (In Decimal): 2.8 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:10	**TX_CLK Pad Input Skew** TX_CLK input Skew Control (0.1ns/step) **Note:**	R/W	07h
9:5	**GTX_CLK/TXC Pad Input Skew** GTX_CLK/TXC input Skew Control (~24 min to ~58 max ps/step)	R/W	07h
4:0	**RX_CLK/RXC Pad Output Skew** RX_CLK/RXC output Skew Control (~24 min to ~58 max ps/step)	R/W	07h

5.2.17 SELF-TEST PACKET COUNT LO REGISTER

Index (In Decimal): 2.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[15:0]**	R/W	0000h

5.2.18 SELF-TEST PACKET COUNT HI REGISTER

Index (In Decimal): 2.10 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[31:16]**	R/W	0001h

5.2.19 SELF-TEST STATUS REGISTER

Index (In Decimal): 2.11 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_done** 0 = Self test running 1 = Self test finished	RO	0b

5.2.20 SELF-TEST FRAME COUNT ENABLE REGISTER

Index (In Decimal): 2.12 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_frame_cnt_en** 0 = disabled 1 = enabled	R/W	0b

5.2.21 SELF-TEST PGEN ENABLE REGISTER

Index (In Decimal): 2.13 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Force_self_test_pgen_en** 0 = packet generator needs to wait for link up to start sending data 1 = packet generator sends data regardless of link status	R/W	0b
3:1	**RESERVED**	RO	—
0	**Self_test_pgen_en** 0 = disabled 1 = enabled	R/W	0b

5.2.22 SELF-TEST ENABLE REGISTER

Index (In Decimal): 2.14 Size: 16 bits

Bits	Description	Type	Default
15	**Self_test_external_clk_sel** **Note:** This bit is not used.	R/W	0b
14:13	**Self_test_packet_type[1:0]** 00 = random data bit 01 = all data bits and SA/DA are 0 10 = all data bits and SA/DA are 1 11 = random	R/W	00b
12:10	**RESERVED**	RO	—
9	**Self_test_clear_counters_on_link_down** 1 = clear counters on link drop 0 = don't clear counters on link drop	R/W	0b
8	**Self_test_CRC_checker_enable** 1 = Enable 0 = Disable	R/W	0b
7:5	**RESERVED**	RO	—
4	**GMII_TX_CRC_check_en** Enables CRC_checker in Tx path (toward line) 0 = disabled 1 = enabled	R/W	0b
3:1	**RESERVED**	RO	—
0	**Self_test_en** 0 = disabled 1 = enabled	R/W	0b

5.2.23 WAKE-ON-LAN CONTROL REGISTER

Index (In Decimal): 2.16 Size: 16 bits

Bits	Description	Type	Default
15:14	**PME Output Select** Controls definition of PME_N signal. 00 = PME 01 = Interrupt 10 = Interrupt ORed with PME 11 = always 0 **Note:** This field controls the PME_N function regardless of the pin to which PME_N is mapped.	R/W	00b
13	**RESERVED**	R/W	—
12	**Enable Energy Not Detected Wake Event** Enables energy not detected as a wake event	R/W	0b
11	**Enable Energy Detected Wake Event** Enables energy detected as a wake event	R/W	0b
7	**Wake-on-LAN Reset (Wol_reset)** Write a 1 then a 0 to reset the WoL module.	R/W	0b
6	**Enable Magic Packet Detection Wake Event** Enables magic packet detection as a wake event	R/W	0b
5:2	**Enable Customized Frame Filter Wake Event** Enables customized frame filters as wake events	R/W	0h
1	**Enable Link Down Wake Event** Enables link down as a wake event	R/W	0b
0	**Enable Link Up Wake Event** Enables link up as a wake event	R/W	0b

5.2.24 WAKE-ON-LAN-MAC-LO REGISTER

Index (In Decimal): 2.17 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-lo** MAC-Address[15:0] of magic packet	R/W	0000h

5.2.25 WAKE-ON-LAN-MAC-MI REGISTER

Index (In Decimal): 2.18 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-mi** MAC-Address[31:16] of magic packet	R/W	0000h

5.2.26 WAKE-ON-LAN-MAC-HI REGISTER

Index (In Decimal): 2.19 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-hi** MAC-Address[47:32] of magic packet	R/W	0000h

5.2.27 CUSTOMIZED-PKT-0-CRC-LO REGISTER

Index (In Decimal): 2.20 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-lo** Customized frame filter 0 CRC[15:0]	R/W	0000h

5.2.28 CUSTOMIZED-PKT-0-CRC-HI REGISTER

Index (In Decimal): 2.21 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-hi** Customized frame filter 0 CRC[31:16]	R/W	0000h

5.2.29 CUSTOMIZED-PKT-1-CRC-LO REGISTER

Index (In Decimal): 2.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-lo** Customized frame filter 1 CRC[15:0]	R/W	0000h

5.2.30 CUSTOMIZED-PKT-1-CRC-HI REGISTER

Index (In Decimal): 2.23 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-hi** Customized frame filter 1 CRC[31:16]	R/W	0000h

5.2.31 CUSTOMIZED-PKT-2-CRC-LO REGISTER

Index (In Decimal): 2.24 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-lo** Customized frame filter 2 CRC[15:0]	R/W	0000h

5.2.32 CUSTOMIZED-PKT-2-CRC-HI REGISTER

Index (In Decimal): 2.25 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-hi** Customized frame filter 2 CRC[31:16]	R/W	0000h

5.2.33 CUSTOMIZED-PKT-3-CRC-LO REGISTER

Index (In Decimal): 2.26 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-lo** Customized frame filter 3 CRC[15:0]	R/W	0000h

5.2.34 CUSTOMIZED-PKT-3-CRC-HI REGISTER

Index (In Decimal): 2.27 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-hi** Customized frame filter 3 CRC[31:16]	R/W	0000h

5.2.35 CUSTOMIZED-PKT-0-MASK_LL REGISTER

Index (In Decimal): 2.28 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-ll** Customized frame filter 0 mask[15:0]	R/W	0000h

5.2.36 CUSTOMIZED-PKT-0-MASK_LH REGISTER

Index (In Decimal): 2.29 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-lh** Customized frame filter 0 mask[31:16]	R/W	0000h

5.2.37 CUSTOMIZED-PKT-0-MASK_HL REGISTER

Index (In Decimal): 2.30 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hl** Customized frame filter 0 mask[47:32]	R/W	0000h

5.2.38 CUSTOMIZED-PKT-0-MASK_HH REGISTER

Index (In Decimal): 2.31 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hh** Customized frame filter 0 mask[63:48]	R/W	0000h

5.2.39 CUSTOMIZED-PKT-1-MASK_LL REGISTER

Index (In Decimal): 2.32 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-ll** Customized frame filter 1 mask[15:0]	R/W	0000h

5.2.40 CUSTOMIZED-PKT-1-MASK_LH REGISTER

Index (In Decimal): 2.33 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-lh** Customized frame filter 1 mask[31:16]	R/W	0000h

5.2.41 CUSTOMIZED-PKT-1-MASK_HL REGISTER

Index (In Decimal): 2.34 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hl** Customized frame filter 1 mask[47:32]	R/W	0000h

5.2.42 CUSTOMIZED-PKT-1-MASK_HH REGISTER

Index (In Decimal): 2.35 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hh** Customized frame filter 1 mask[63:48]	R/W	0000h

5.2.43 CUSTOMIZED-PKT-2-MASK_LL REGISTER

Index (In Decimal): 2.36 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-ll** Customized frame filter 2 mask[15:0]	R/W	0000h

5.2.44 CUSTOMIZED-PKT-2-MASK_LH REGISTER

Index (In Decimal): 2.37 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-lh** Customized frame filter 2 mask[31:16]	R/W	0000h

5.2.45 CUSTOMIZED-PKT-2-MASK_HL REGISTER

Index (In Decimal): 2.38 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hl** Customized frame filter 2 mask[47:32]	R/W	0000h

5.2.46 CUSTOMIZED-PKT-2-MASK_HH REGISTER

Index (In Decimal): 2.39 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hh** Customized frame filter 2 mask[63:48]	R/W	0000h

5.2.47 CUSTOMIZED-PKT-3-MASK_LL REGISTER

Index (In Decimal): 2.40 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-ll** Customized frame filter 3 mask[15:0]	R/W	0000h

5.2.48 CUSTOMIZED-PKT-3-MASK_LH REGISTER

Index (In Decimal): 2.41 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-lh** Customized frame filter 3 mask[31:16]	R/W	0000h

5.2.49 CUSTOMIZED-PKT-3-MASK_HL REGISTER

Index (In Decimal): 2.42 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hl** Customized frame filter 3 mask[47:32]	R/W	0000h

5.2.50 CUSTOMIZED-PKT-3-MASK_HH REGISTER

Index (In Decimal): 2.43 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hh** Customized frame filter 3 mask[63:48]	R/W	0000h

5.2.51 WAKE-ON-LAN CONTROL STATUS REGISTER

Index (In Decimal): 2.44 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_ctrl_status** Wake-on-LAN Control module status	RO	0000h

5.2.52 WAKE-ON-LAN CUSTOM PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.45 Size: 16 bits

Bits	Description	Type	Default
15	**cpkt_pmen** custom packet 0 enabled and custom packet 0 found	RO	0b
14:12	**mismatch code**	RO	000b
11	**good_pkt_crc**	RO	0b
10:7	**crc_match** crc matched bit 10 = custom packet 3 bit 9 = custom packet 2 bit 8 = custom packet 1 bit 7 = custom packet 0	RO	0000b
6:3	**cpkt_found** custom packet found bit 6 = custom packet 3 bit 5 = custom packet 2 bit 4 = custom packet 1 bit 3 = custom packet 0	RO	0000b
2:0	**cpkt_state** custom packet detection state	RO	000b

5.2.53 WAKE-ON-LAN MAGIC PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.46 Size: 16 bits

Bits	Description	Type	Default
15	**mpkt_pmen** magic packet enabled and magic packet found	RO	0b
14:12	**byte count**	RO	000b
11:9	**mismatch code**	RO	000b
8:5	**macda_match_count**	RO	0h
4	**good_pkt_crc**	RO	0b
3	**mpkt_found** magic packet found	RO	0b
2:0	**mpkt_state** magic packet detection state	RO	000b

5.2.54 WAKE-ON-LAN DATA MODULE STATUS REGISTER

Index (In Decimal): 2.47 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_data_status** Wake-on-LAN Data module status	RO	0000h

5.2.55 CUSTOMIZED PKT-0 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.48 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 0	RO	0000h

5.2.56 CUSTOMIZED PKT-0 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.49 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 0	RO	0000h

5.2.57 CUSTOMIZED PKT-1 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.50 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 1	RO	0000h

5.2.58 CUSTOMIZED PKT-1 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.51 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 1	RO	0000h

5.2.59 CUSTOMIZED PKT-2 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.52 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 2	RO	0000h

5.2.60 CUSTOMIZED PKT-2 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.53 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 2	RO	0000h

5.2.61 CUSTOMIZED PKT-3 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.54 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 3	RO	0000h

5.2.62 CUSTOMIZED PKT-3 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.55 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 3	RO	0000h

5.2.63 SELF-TEST CORRECT COUNT LO REGISTER

Index (In Decimal): 2.60 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count HI Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[15:0]**	RO	—

5.2.64 SELF-TEST CORRECT COUNT HI REGISTER

Index (In Decimal): 2.61 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count LO Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[31:16]**	RO	—

5.2.65 SELF-TEST ERROR COUNT LO REGISTER

Index (In Decimal): 2.62 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count HI Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[15:0]**	RO	—

5.2.66 SELF-TEST ERROR COUNT HI REGISTER

Index (In Decimal): 2.63 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count LO Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[31:16]**	RO	—

5.2.67 RX DLL CONTROL REGISTER

Index (In Decimal): 2.76 Size: 16 bits

Bits	Description	Type	Default
15	**rxdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by rxdll_tap_sel.	R/W	0b
14	**bypass rxdll** 1 = RXC DLL delay is not used	R/W	0b
13:7	**rxdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The rxdll_reset bit must be set following a change to this field.	R/W	1Bh
6:0	**rxdll_tap_adj** **Note:** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	1Bh

5.2.68 TX DLL CONTROL REGISTER

Index (In Decimal): 2.77 Size: 16 bits

Bits	Description	Type	Default
15	**txdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by txdll_tap_sel.	R/W	0b
14	**bypass txdll** 1 = TXC DLL delay is not used	R/W	1b
13:7	**txdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The txdll_reset bit must be set following a change to this field.	R/W	1Bh
6:0	**txdll_tap_adj** **Note:** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	1Bh

5.2.69 1000M FAST LINK DOWN ENABLE REGISTER

Index (In Decimal): 2.90 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	R/O	—
8	**1000M Fast Link Down Enable** Enable 1000BT fast link loss time (< 50 µs) onto Link Down Interrupt (PHY Register 27). Also maps Link Down Interrupt onto INT_N interrupt pin.	R/W	0b
7:0	**RESERVED**	R/O	—

5.2.70 DRIVING STRENGTH, FAST LINK DOWN, S2P RX PCS SELECT SETTING REGISTER

Index (In Decimal): 2.111 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	R/W	—
12	**Fast Link Fail Enable** Enable 1000/100 BT fast link loss time (< 15us) into in RGMII in-band status when not operating with EEE	R/W	0b
11:0	**RESERVED**	R/W	—

5.2.71 GENERAL PURPOSE IO ENABLE REGISTER (GPIO_EN)

Index (In Decimal): 2.128 Size: 16 bits

This register enables the GPIO onto its shared pin.

In order for a GPIO to function as an interrupt source, it must be configured as an input.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Enable (GPIO_EN)** When set, the pin functions as a GPIO.	R/W	000h

5.2.72 GENERAL PURPOSE IO DIRECTION REGISTER (GPIO_DIR)

Index (In Decimal): 2.129 Size: 16 bits

This register controls the GPIO direction.

In order for a GPIO to function as an interrupt source, it must be configured as an input.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Direction (GPIO_DIR)** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.	R/W	000h

5.2.73 GENERAL PURPOSE IO BUFFER TYPE REGISTER (GPIO_BUF)

Index (In Decimal): 2.130 Size: 16 bits

This register sets the GPIO output buffer type.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Buffer Type (GPIO_BUF)** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver.	R/W	000h

5.2.74 GENERAL PURPOSE IO DATA SELECT 1 REGISTER (GPIO_DATA_SEL1)

Index (In Decimal): 2.131 Size: 16 bits

This register selects the GPIO output data source value for GPIO 0-4.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:12	**GPIO 4 Data Select (GPIO4_DATA_SEL)** This field selects the output data source for GPIO 4. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
11:9	**GPIO 3 Data Select (GPIO3_DATA_SEL)** This field selects the output data source for GPIO 3. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
8:6	**GPIO 2 Data Select (GPIO2_DATA_SEL)** This field selects the output data source for GPIO 2. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
5:3	**GPIO 1 Data Select (GPIO1_DATA_SEL)** This field selects the output data source for GPIO 1. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
2:0	**GPIO 0 Data Select (GPIO0_DATA_SEL)** This field selects the output data source for GPIO 0. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b

5.2.75 GENERAL PURPOSE IO DATA SELECT 2 REGISTER (GPIO_DATA_SEL2)

Index (In Decimal): 2.132 Size: 16 bits

This register selects the GPIO output data source value for GPIO 5-9.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:12	**GPIO 9 Data Select (GPIO9_DATA_SEL)** This field selects the output data source for GPIO 9. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
11:9	**GPIO 8 Data Select (GPIO8_DATA_SEL)** This field selects the output data source for GPIO 8. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
8:6	**GPIO 7 Data Select (GPIO7_DATA_SEL)** This field selects the output data source for GPIO 7. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
5:3	**GPIO 6 Data Select (GPIO6_DATA_SEL)** This field selects the output data source for GPIO 6. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
2:0	**GPIO 5 Data Select (GPIO5_DATA_SEL)** This field selects the output data source for GPIO 5. 000 : GPIO data register 001 : reserved 010 : reserved 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b

5.2.76 GENERAL PURPOSE IO DATA REGISTER (GPIO_DATA)

Index (In Decimal): 2.133 Size: 16 bits

This register sets or reads the GPIO data value.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Data (GPIO_D)** When enabled as an output, the value written is reflected on the GPIO. When read, the value always reflects the current state of the corresponding GPIO pin, regardless of the value written or the GPIO direction.	R/W	000h

5.2.77 GENERAL PURPOSE IO INTERRUPT STATUS REGISTER (GPIO_INT_STS)

Index (In Decimal): 2.134 Size: 16 bits

This register contains the GPIO interrupt status bits.

Reading this register clears the interrupt status.

Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Interrupt (GPIO_INT)** Interrupts generated from the GPIOs. **Note:** The sources for these interrupts are level sensitive. **Note:** The GPIO inputs must be stable for ~85ns (2 consecutive 25MHz edges) to be recognized.	RC	Note 5-19

Note 5-19 The default depends on the state of the GPIO pin

5.2.78 GENERAL PURPOSE IO INTERRUPT ENABLE REGISTER (GPIO_INT_EN)

Index (In Decimal): 2.135 Size: 16 bits

This register is used to enable the corresponding bits in the General Purpose IO Interrupt Status Register (GPIO_INT_STS) as an interrupt source.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Interrupt Enable (GPIO_INT_EN)** When set, interrupts are enabled from the GPIOs.	R/W	000h

5.2.79 GENERAL PURPOSE IO INTERRUPT POLARITY REGISTER (GPIO_INT_POL)

Index (In Decimal): 2.136 Size: 16 bits

This register configures the interrupt polarity.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**GPIO Interrupt Polarity (GPIO_INT_POL)** When clear, an interrupt is triggered when the GPIO input is low. When set, an interrupt is triggered when the GPIO input is high.	R/W	000h

5.2.80 PCS CONTROL 1 REGISTER

Index (In Decimal): 3.0 Size: 16 bits

Bits	Description	Type	Default
15	**RESET** 1=PCS reset 0=Normal Operation This bit is not used	R/W	0b
14	**Loop Back** 1 = enable loop-back mode 0 = Normal Operation This bit is not used	R/W	0b
13	**RESERVED**	R/W	—
12	**EEE100_idle_sel** 0 = 9031 1 = 8050	R/W	0b
11	**Low power** 1 = low-power-mode 0 = normal operation	R/W	0b
10	**Clock-stop enable** 1 = the PHY may stop the clock during LPI 0 = clock not stoppable	R/W	0b
9:7	**TX FIFO threshold 1000**	R/W	100b
6:4	**TX FIFO threshold 100**	R/W	111b
3:1	**RESERVED**	R/W	—
0	**Dbg_pcs100_sel** 1 = select eee100 RX signals 0 = original	R/W	0b

5.2.81 PCS STATUS 1 REGISTER

Index (In Decimal): 3.1 Size: 16 bits

For the LL and LH bits, if the host reads this register as a new condition corresponding to the same bit occurs, the LL/LH bit will remain cleared/set. If a level event remains asserted, then the corresponding bit will remain cleared/set.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11	**TX LPI received** 1 = TX PCS has received LPI 0 = LPI not received	RO/LH	0b
10	**RX LPI received** 1 = RX PCS has received LPI 0 = LPI not received	RO/LH	0b
9	**TX LPI indication** 1 = TX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
8	**RX LPI indication** 1 = RX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
7	**Fault** 1 = Fault condition detected 0 = No fault condition detected	RO	0b
6	**Clock stop capable** 1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO	1b
5:3	**RESERVED**	RO	—
2	**PCS receive link status** 1 = PCS receive link up 0 = PCS receive link down	RO	0b
1	**Low-power ability** 1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	Note 5-20
0	**RESERVED**	RO	—

Note 5-20 This bit is a 1 if either the 1000BASE-T EEE or 100BASE-TX EEE bit in the EEE Advertisement Register is set. Otherwise it is a 0.

5.2.82 EEE QUIET TIMER REGISTER

Index (In Decimal): 3.8 Size: 16 bits

Bits	Description	Type	Default
15:0	**Quiet-Timer** 1G-EEE quieter Timer Max Value	R/W	006Eh

5.2.83 EEE UPDATE TIMER REGISTER

Index (In Decimal): 3.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Update-Timer** 1G-EEE Update Timer Max Value	R/W	005Fh

5.2.84 EEE LINK-FAIL TIMER REGISTER

Index (In Decimal): 3.10 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Link-Fail-Timer** 1G-EEE Link-Fail Timer Max Value	R/W	5Ah

5.2.85 EEE POST-UPDATE TIMER REGISTER

Index (In Decimal): 3.11 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Post-Update-Timer** 1G-EEE Post-Update Timer Max Value	R/W	50h

5.2.86 EEE WAITWQ TIMER REGISTER

Index (In Decimal): 3.12 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WaitWQ-Timer** 1G-EEE WaitWQ Timer Max Value	R/W	5Bh

5.2.87 EEE WAKE TIMER REGISTER

Index (In Decimal): 3.13 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Wake-Timer** 1G-EEE Wake Timer Max Value	R/W	89h

5.2.88 EEE WAKETX TIMER REGISTER

Index (In Decimal): 3.14 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WakeTX-Timer** 1G-EEE WakeTX Timer Max Value	R/W	1Fh

5.2.89 EEE WAKEMZ TIMER REGISTER

Index (In Decimal): 3.15 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WakeMz-Timer** 1G-EEE WakeMz Timer Max Value	R/W	6Eh

5.2.90 EEE CONTROL AND CAPABILITY REGISTER

Index (In Decimal): 3.20 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**100GBASE-R deep sleep** 1 = EEE deep sleep is supported for 100GBASE-R 0 = EEE deep sleep is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
12	**100GBASE-R fast wake** 1 = EEE fast wake is supported for 100GBASE-R 0 = EEE fast wake is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
11:10	**RESERVED**	RO	—
9	**40GBASE-R deep sleep** 1 = EEE deep sleep is supported for 40GBASE-R 0 = EEE deep sleep is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
8	**40GBASE-R fast wake** 1 = EEE fast wake is supported for 40GBASE-R 0 = EEE fast wake is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
7	**RESERVED**	RO	—
6	**10GBASE-KR EEE** 0 = EEE is not supported for 10GBASE-KR. 1 = EEE is supported for 10GBASE-KR. **Note:** The device does not support this mode.	RO	0b

Bits	Description	Type	Default
5	**10GBASE-KX4 EEE** 0 = EEE is not supported for 10GBASE-KX4. 1 = EEE is supported for 10GBASE-KX4. **Note:** The device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = EEE is not supported for 10GBASE-KX. 1 = EEE is supported for 10GBASE-KX. **Note:** The device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = EEE is not supported for 10GBASE-T. 1 = EEE is supported for 10GBASE-T. **Note:** The device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = EEE is not supported for 1000BASE-T. 1 = EEE is supported for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = EEE is not supported for 100BASE-TX. 1 = EEE is supported for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	—

5.2.91 EEE WAKE ERROR COUNTER REGISTER

Index (In Decimal): 3.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**EEE Wake Error Counter** This counter is cleared to zeros on read and is held to all ones on overflow.	RC	0000h

5.2.92 EEE 100 TIMER-0 REGISTER

Index (In Decimal): 3.24 Size: 16 bits

Bits	Description	Type	Default
15:8	**TX_SLEEP_TIMER_ADD** tx_sleep_time = (5250 + TX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_WAKE_TIMER_ADD** tx_wake_time = (513 + TX_WAKE_TIMER_ADD * 4) * 40ns	R/W	00h
0	**RESERVED**	R/W	0b

5.2.93 EEE 100 TIMER-1 REGISTER

Index (In Decimal): 3.25 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_SLEEP_TIMER_ADD** rx_sleep_time = (6250 + RX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_QUIET_TIMER_ADD** tx_quiet_time = (525000 + TX_QUIET_TIMER_ADD * 8192) * 40ns	R/W	00h
0	**eee_100_test** 1 = force TX LPI	R/W	0b

5.2.94 EEE 100 TIMER-2 REGISTER

Index (In Decimal): 3.26 Size: 16 bits

Bits	Description	Type	Default
15:12	**RX_WAIT_IDLE_EXIT_TIMER_ADD** rx_wait_idle_exit_time = (16 + RX_WAIT_IDLE_EXIT_TIMER_ADD * 2) * 40ns	R/W	0h
11:8	**RX_IDLE_WAIT_TIMER_ADD** rx_idle_wait_time = (20 + RX_IDLE_WAIT_TIMER_ADD * 2) * 40ns	R/W	0h
7:0	**RX_QUIET_TIMER_ADD** rx_quiet_time = (625000 + RX_QUIET_TIMER_ADD * 4096) * 40ns	R/W	00h

5.2.95 EEE 100 TIMER-3 REGISTER

Index (In Decimal): 3.27 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_WAKE_TIMER_ADD** rx_wake_time = (512 + RX_WAKE_TIMER_ADD * 4) * 40ns	R/W	00h
7:0	**RX_LINK_FAIL_TIMER_ADD** rx_link_fail_time = (2500 + RX_LINK_FAIL_TIMER_ADD * 16) * 40ns	R/W	00h

5.2.96 EEE ADVERTISEMENT REGISTER

Index (In Decimal): 7.60 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	—
13	**100GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR4 deep sleep 1 = Advertise EEE capability for 100GBASE-CR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
12	**100GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KR4 deep sleep 1 = Advertise EEE capability for 100GBASE-KR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
11	**100GBASE-KP4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KP4 deep sleep 1 = Advertise EEE capability for 100GBASE-KP4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
10	**100GBASE-CR10 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR10 deep sleep 1 = Advertise EEE capability for 100GBASE-CR10 deep sleep **Note:** The device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	—
8	**40GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-CR4 deep sleep 1 = Advertise EEE capability for 40GBASE-CR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
7	**40GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-KR4 deep sleep 1 = Advertise EEE capability for 40GBASE-KR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Do not advertise EEE capability for 10GBASE-KR 1 = Advertise EEE capability for 10GBASE-KR **Note:** The device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Do not advertise EEE capability for 10GBASE-KX4 1 = Advertise EEE capability for 10GBASE-KX4 **Note:** The device does not support this mode.	R/W	0b

Bits	Description	Type	Default
4	**10GBASE-KX EEE** 0 = Do not advertise EEE capability for 10GBASE-KX 1 = Advertise EEE capability for 10GBASE-KX **Note:** The device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Do not advertise EEE capability for 10GBASE-T 1 = Advertise EEE capability for 10GBASE-T **Note:** The device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Do not advertise EEE capability for 1000BASE-T 1 = Advertise EEE capability for 1000BASE-T	R/W	1b
1	**100BASE-TX EEE** 0 = Do not advertise EEE capability for 100BASE-TX. 1 = Advertise EEE capability for 100BASE-TX.	R/W	1b
0	**RESERVED**	R/W	—

5.2.97 EEE LINK PARTNER ABILITY REGISTER

Index (In Decimal): 7.61 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	RO	0b
9	**RESERVED**	RO	0b
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	RO	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	RO	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	RO	0b

Bits	Description	Type	Default
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	—

5.2.98 EEE LINK PARTNER ABILITY OVERRIDE REGISTER

Index (In Decimal): 7.62 Size: 16 bits

Bits	Description	Type	Default
15	**LP AN Override** 0 = Use Link partner AN results 1 = Use bits 10:0 as Link partner results	R/W	0b
14:11	**RESERVED**	R/W	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	—
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	R/W	0b

Bits	Description	Type	Default
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	R/W	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	R/W	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	R/W	0b
0	**RESERVED**	R/W	—

5.2.99 EEE MESSAGE CODE REGISTER

Index (In Decimal): 7.63 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	—
10:0	**EEE_message_code** Programmable EEE specific message code for AN	R/W	00Ah

5.2.100 XTAL CONTROL REGISTER

Index (In Decimal): 28.1 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	—
13	**XTAL Disable** Crystal oscillator disable 0 = XTAL enabled 1 = XTAL disabled	R/W NASR	0b
12:0	**RESERVED**	R/W NASR	—

5.2.101 AFED CONTROL REGISTER

Index (In Decimal): 28.9 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**p_cat3** 0 = cat5 parameter for 10 Base-Te TX 1 = cat3 parameter for 10 Base-T TX	R/W	0b
8:0	**RESERVED**	RO	—

5.2.102 LDO CONTROL REGISTER

Index (In Decimal): 28.14 Size: 16 bits

Bits	Description	Type	Default
15	**LDO enable** turn off VDD regulator by software 1 = off 0 = on	R/W NASR	0b
14:12	**LDO reference tune<2:0>** Tune LDO output voltage @Iload=200mA 000 = 1.097 V 001 = 1.139 V 010 = RESERVED 011 = RESERVED 100 = RESERVED 101 = RESERVED 110 = RESERVED 111 = RESERVED	R/W NASR	000b
11:0	**RESERVED**	R/W	—

5.2.103 EDPD CONTROL REGISTER

Index (In Decimal): 28.36 Size: 16 bits

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**EDPD Low Power** 0 = EDPD mode disabled 1 = EDPD mode enabled	RO	0b
5:4	**p_edpd_mask_timer[1:0]** 00 = EDPD mask for 2.6us 01 = 3.2us 10 = 4.0us 11 = 5.0us	R/W	00b
3:2	**p_edpd_timer[1:0]** 00 = EDPD pulse separation for 1s 01 = 1.3s 10 = 1.6s 11 = 1.9s	R/W	00b
1	**p_EDPD_random_dis** 1 = use edpd_timer value as EDPD pulse separation selection 0 = use random seed value as EDPD pulse separation selection	R/W	0b

Bits	Description	Type	Default
0	**EDPD Mode Enable** 0 = EDPD mode disabled 1 = EDPD mode enabled	R/W	0b

5.2.104 EMITX CONTROL REGISTER

Index (In Decimal): 28.37 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1:0	**p_scale**	RO	00b

5.2.105 EMITX COEFFICIENT REGISTERS

Index (In Decimal): 28.38-52 Size: 16 bits

Register	Bits	Description	Type	Default
38	15	**RESERVED**	RO	—
	14:8	**p_coeff1**	RO	31d
	7	**RESERVED**	RO	—
	6:0	**p_coeff0**	RO	15d
39	15	**RESERVED**	RO	—
	14:8	**p_coeff3**	RO	31d
	7	**RESERVED**	RO	—
	6:0	**p_coeff2**	RO	31d
40	15	**RESERVED**	RO	—
	14:8	**p_coeff5**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff4**	RO	16d

Register	Bits	Description	Type	Default
41	15	**RESERVED**	RO	—
	14:8	**p_coeff7**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff6**	RO	0d
42	15	**RESERVED**	RO	—
	14:8	**p_coeff9**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff8**	RO	0d
43	15	**RESERVED**	RO	—
	14:8	**p_coeff11**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff10**	RO	0d
44	15	**RESERVED**	RO	—
	14:8	**p_coeff13**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff12**	R/W	0d
45	15	**RESERVED**	RO	—
	14:8	**p_coeff15**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff14**	R/W	0d
46	15	**RESERVED**	RO	—
	14:8	**p_coeff17**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff16**	R/W	0d
47	15	**RESERVED**	RO	—
	14:8	**p_coeff19**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff18**	R/W	0d
48	15	**RESERVED**	RO	—
	14:8	**p_coeff21**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff20**	R/W	0d

Register	Bits	Description	Type	Default
49	15	**RESERVED**	RO	—
	14:8	**p_coeff23**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff22**	R/W	0d
50	15	**RESERVED**	RO	—
	14:8	**p_coeff25**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff24**	R/W	0d
51	15	**RESERVED**	RO	—
	14:8	**p_coeff27**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff26**	R/W	0d
52	15	**RESERVED**	RO	—
	14:8	**p_coeff29**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff28**	R/W	0d

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004785B (01-10-25)	Section 3.1, Register Nomenclature	New section
	Section 5.1.15, PCS Loopback Swap/Polarity Control Register	Renamed table as PCS LOOPBACK SWAP/ POLARITY CONTROL REGISTER. Added bits 7:6 and bit 2.
	Section 5.1.21, Output Control Register	Changed LED Polarity bits 5:0 to RO.
	Section 5.2.69, 1000M Fast Link Down Enable Register	New section
DS00004785A (10-12-22)	Initial release	

NOTES:

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