VSC8512

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8512 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8512 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "QSGMII/SGMII SerDes Interfaces"
- Section 6.0, "Device Clocks"
- Section 7.0, "Digital Interface and I/O"
- Section 8.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8512 implementor should have the following documents on hand:

- *VSC8512-02 12-Port 10/100/1000BASE-T PHY with SGMII and QSGMII MAC Data Sheet*
- VSC7247+VSC8512 reference design is available; the schematic is the evaluation design for VSC8512. There is no standalone (PHY only) EVB for VSC8512. See www.microchip.com/VSC5611EV.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

3.0 POWER

Table 3-1 shows the power supply pins for VSC8512.

TABLE 3-1: POWER SUPPLY PINS

Name	Pins	Description	Comments
VDD_[1:80]	G6, G7, G8, G11, G12, G15, G16, G19, G20, G21, H6, H7, H8, H9, H10, H11, H12, H15, H16, H17, H18, H19, H20, H21, L6, L7, L20, L21, M6, M7, M20, M21, N6, N7, N20, N21, P6, P7, P20, P21, R6, R7, R20, R21, T6, T7, T20, T21, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21	Digital 1.0V power	Digital, no ferrite bead
VDD_A_[1:16]	AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21	Analog SerDes 1.0V power	Analog, use ferrite bead
VDD_AH_[1:36]	D4, D5, D11, D16, E4, E5, E8, E11, E12, E15, E16, E19, E22, E23, F4, F5, F7, F8, F11, F12, F15, F16, F19, F20, F22, F23, J3, J4, J23, J24, M3, M4, M5, M22, M23, M24	Analog 2.5V power	Analog, use ferrite bead
VDD_AL_[1:24]	E9, E10, E17, E18, F9, F10, F17, F18, G9, G10, G17, G18, J5, J6, J7, J20, J21, J22, K5, K6, K7, K20, K21, K22	Analog 1.0V power	Analog, use ferrite bead
VDD_IO_[1:20]	E6, E7, E20, E21, F6, F21, P5, R5, T5, U5, V5, W5, Y5, AA5, AB5, AC4, AC5, AD4, AE3, AF2	Digital 2.5V power	Digital, no ferrite bead
VDD_IODDR_[1:14]	P22, R22, T22, U22, V22, W22, Y22, AA22, AB22, AC22, AD23, AE24, AF25, AF24	0V Ground	Ground
VDD_VS_[1:16]	AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21	Analog SerDes 1.0V power	Analog, use ferrite bead
VSS	C6	0V Ground	Ground

TABLE 3-1: POWER SUPPLY PINS (CONTINUED)

Name	Pins	Description	Comments
VSS_[1:163]	B1, B26, G3, G5, G22, G24, H3, H5, H22, H24, K3, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K24, L3, L5, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L22, L24, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, N3, N4, N5, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, N19, N22, N23, N24, P3, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P23, P24, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, Y12, Y16, Y20, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AA12, AA16, AA20, AC3, AD5, AD22, AE1, AE5, AE12, AE16, AE20, AE23, AE26, AF5, AF12, AF16, AF20, AF23, AE4	0V Ground	Ground

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. Refer to Table 3-2. Note the current values in the table need more margin of at least 30-35% based on the typical current for the power supplies design of 2.5V and 1.0V in the system design.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Power Rail	Voltage	Typical (A)	Maximum Power Dissipation (W)
QSGMII to 1000BASE-T Current Consumption			
VDD_AH + VDD_IO	2.5V	1.37 + 0.06	3.575*30% = 4.65
VDD + VDD_A +VDD_AL + VDD_VS	1.0V	1.15 + 0.18 + 0.19 + 0.09	1.61*30% = 2.09
Total Maximum PD	—	—	6.74
QSGMII to 1000BASE-X Current Consumption			
VDD_AH + VDD_IO	2.5V	0.93 + 0.06	2.45*35% = 3.31
VDD + VDD_A +VDD_AL + VDD_VS	1.0V	0.95 + 0.2 + 0.16 + 0.13	1.44*35% = 1.94
Total Maximum PD	—	—	5.25
QSGMII to 100BASE-FX Current Consumption			
VDD_AH + VDD_IO	2.5V	0.93 + 0.06	2.45*35% = 3.31
VDD + VDD_A +VDD_AL + VDD_VS	1.0V	0.95 + 0.2 + 0.16 + 0.13	1.44*35% = 1.94
Total Maximum PD	—	—	5.25
SGMII to 1000BASE-T Current Consumption			
VDD_AH + VDD_IO	2.5V	1.37 + 0.06	3.575*30% = 4.65
VDD + VDD_A +VDD_AL + VDD_VS	1.0V	1.18 + 0.25 + 0.19 + 0.09	1.71*30% = 2.22
Total Maximum PD	—	—	6.87

3.2 Power Supply Planes

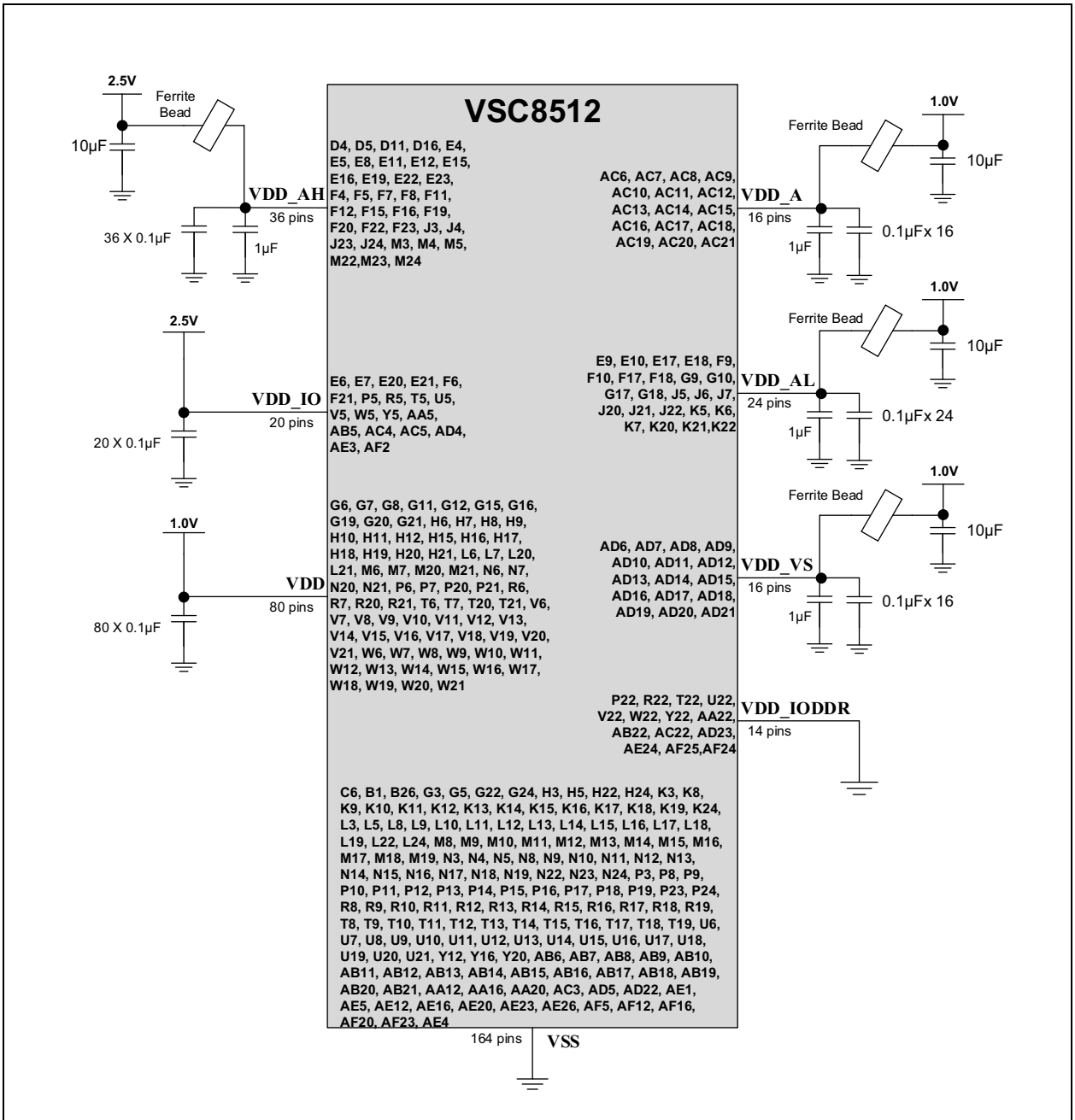
- VSC8512 requires two power rails: 2.5V and 1.0V. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are: VDD_AH at 2.5V; and VDD_A, VDD_AL, and VDD_VS at 1.0V.
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended on digital supplies **VDD** and **VDD_IO**.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8512's power pins for every pin.
- Make sure that bulk capacitors (1 µF to 22 µF) are incorporated in each power rail of power supply.
- If the VSC8512 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 ETHERNET SIGNALS

4.1 10/100/1000 Mbps Interface Connection

The VSC8512 has 12 GPHY ports from PHY 0 to PHY 11 for port 0, port 1, port 2, up to port 11. Detailed pin numbers from PHY 0 to PHY 11 sequence and descriptions are as follows:

- **P[0:11]_D0N** (L25, G25, C25, B22, B18, B14, B10, B6, B2, F2, K2, and P2): These pins are the transmit/receive negative connection from pair A of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D0P** (L26, G26, C26, A22, A18, A14, A10, A6, A2, F1, K1, and P1): These pins are the transmit/receive positive connection from pair A of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D1N** (M25, H25, D25, B23, B19, B15, B11, B7, B3, E2, J2, and N2): These pins are the transmit/receive negative connection from pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D1P** (M26, H26, D26, A23, A19, A15, A11, A7, A3, E1, J1, and N1): These pins are the transmit/receive positive connection from pair B of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D2N** (N25, J25, E25, B24, B20, B16, B12, B8, B4, D2, H2, and M2): These pins are the transmit/receive negative connection from pair C of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D2P** (N26, J26, E26, A24, A20, A16, A12, A8, A4, D1, H1, and M1): These pins are the transmit/receive positive connection from pair C of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D3N** (P25, K25, F25, B25, B21, B17, B13, B9, B5, C2, G2, and L2): These pins are the transmit/receive negative connection from pair D of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P[0:11]_D3P** (P26, K26, F26, A25, A21, A17, A13, A9, A5, C1, G1, and L1): These pins are the transmit/receive positive connection from pair D of the internal PHY 0 to PHY 11. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

There are two types of 10/100/1000 Mbps channel connections solutions: (1) Solution #1 is for an external environment with no electrical noise and with no ESD to be considered (see Figure 4-1), and (2) Solution #2 is for an external environment with electrical noise and with ESD to be considered (see Figure 4-2).

FIGURE 4-1: SOLUTION #1 FOR 12 PORTS OF 10/100/1000 MBPS CHANNEL CONNECTIONS

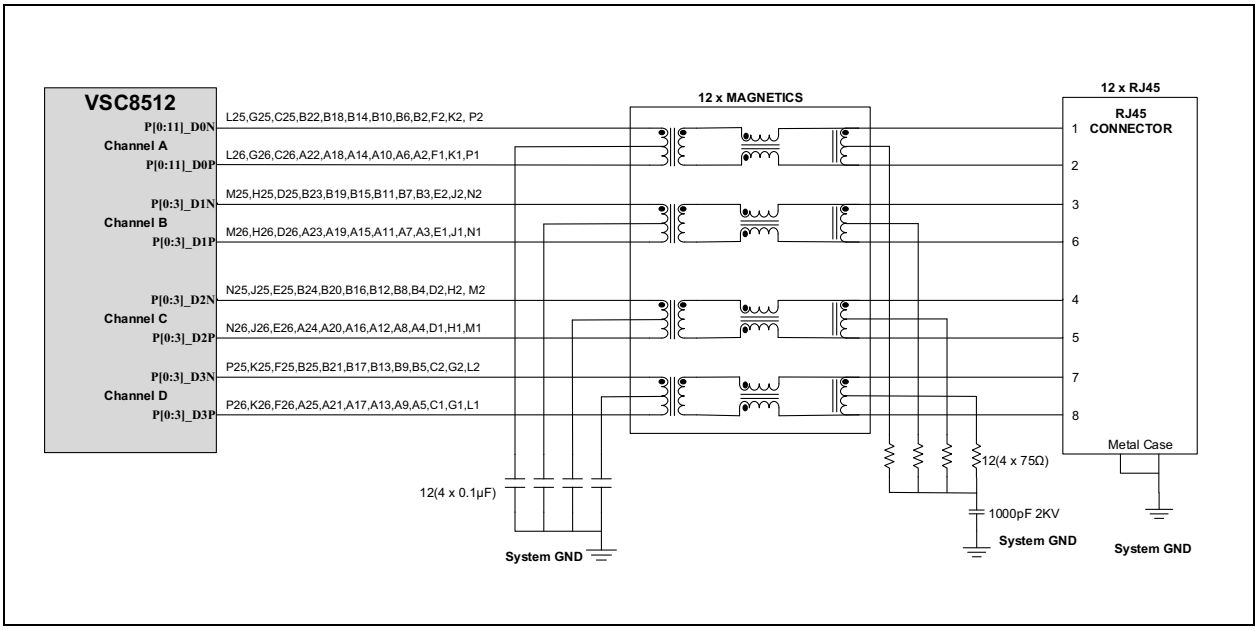
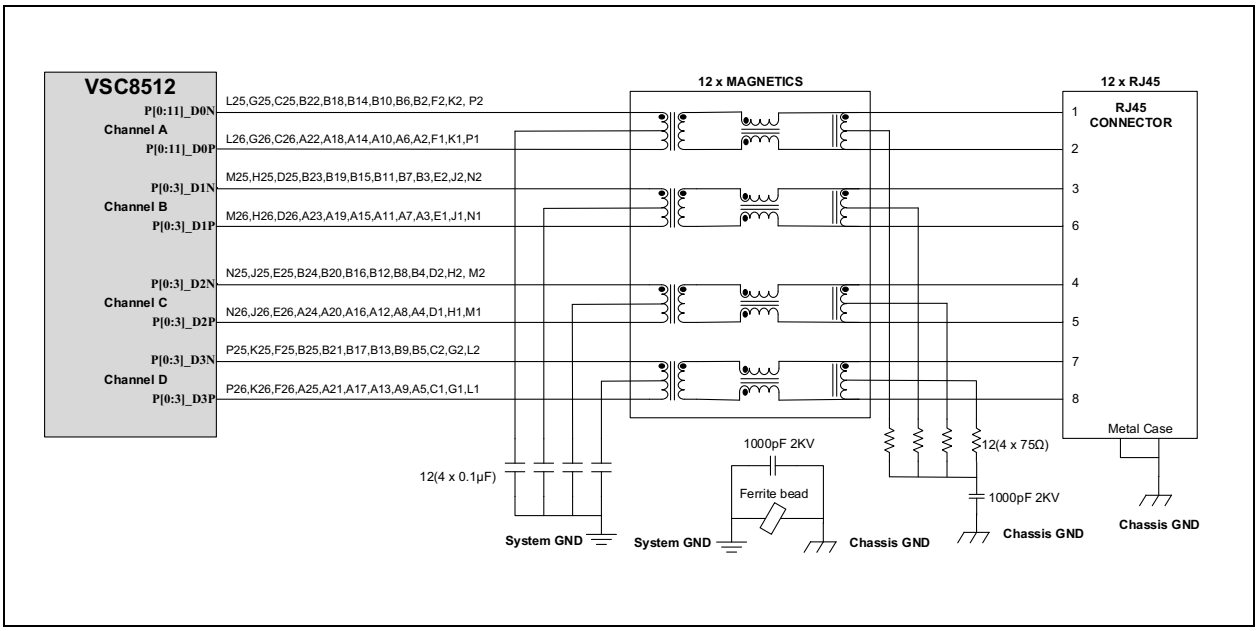


FIGURE 4-2: SOLUTION #2 FOR 12 PORTS OF 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection and RJ45 Connection

- The center tap connection on the VSC8512 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8512 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8512 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8512 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetics should not be connected together without the 0.1 µF capacitor to GND. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground, it is shared by all ports of the PHY chip, ports 1-12.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, "PCB Layout Considerations" for guidance on how chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on the Microchip Technology product page) for reference.

4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss requiring the PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of a pair should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8512 device or other sensitive devices in the PCB layout placement for better ESD.

5.0 QSGMII/SGMII SERDES INTERFACES

- The VSC8512 device supports three QSGMII MAC interfaces, 12 SGMII/SerDes MAC interfaces, or four SerDes media interfaces.
- For details on the QSGMII MAC interface, see Section 5.1, "QSGMII MAC". For details on the SGMII/SerDes MAC interface, see Section 5.2, "SGMII/SerDes MAC". For details on the SerDes media interface, see Section 5.3, "SerDes Media Interface".

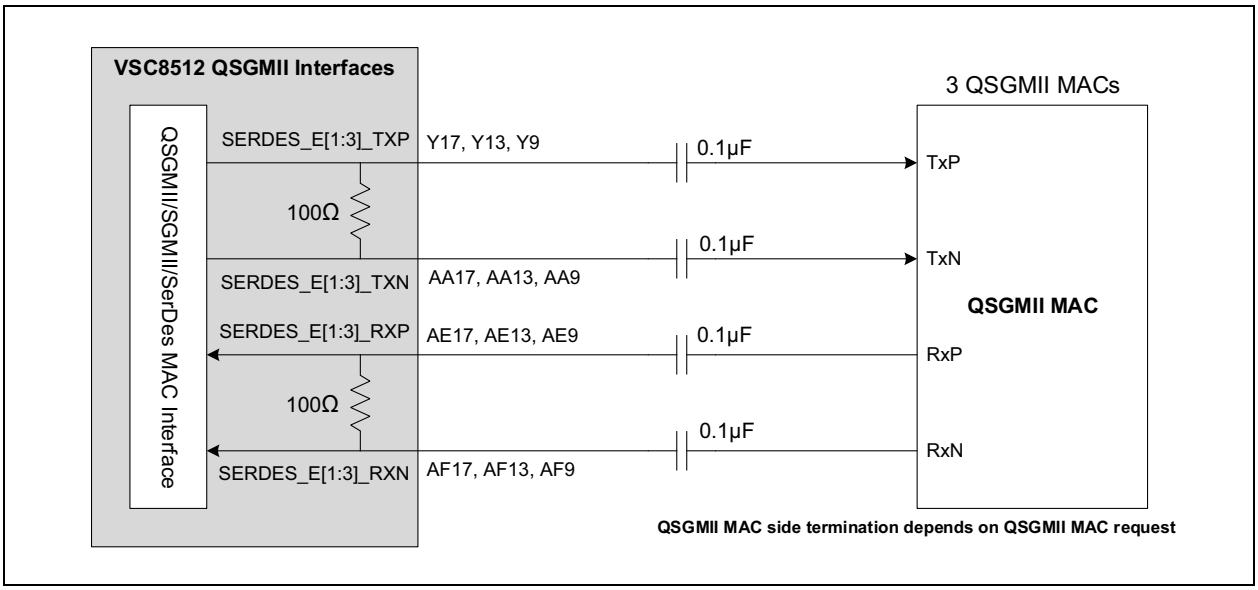
5.1 QSGMII MAC

- The VSC8512 device supports three QSGMII MAC interfaces, QSGMII [0:2], when the operating mode is set to Mode 0 register 19G [15:14] = '00' for QSGMII to CAT5 mode or is set to Mode 2 register 19G [15:14] = '10' for QSGMII to CAT5 and Fiber Media mode.
- For details on the pins numbers, descriptions, and connections of three QSGMII interfaces, see Table 5-1 and Figure 5-1.

TABLE 5-1: QSGMII MAC INTERFACES PINS

QSGMII	Pin Name	Pin Number	Type	Description
QSGMII [0:2] Receive	SERDES_E[1:3]_RXN	AF17, AF13, AF9	I, DIFF	QSGMII MAC receiver input pairs
	SERDES_E[1:3]_RXP	AE17, AE13, AE9	I, DIFF	
QSGMII [0:2] Transmit	SERDES_E[1:3]_TXN	AA17, AA13, AA9	O, DIFF	QSGMII MAC transmitter output pairs
	SERDES_E[1:3]_TXP	Y17, Y13, Y9	O, DIFF	

FIGURE 5-1: THREE QSGMII MAC INTERFACE TO QSGMII MAC CONNECTIONS



5.2 SGMII/SerDes MAC

- When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8512 device can be connected to an SGMII-compatible MAC.
- The VSC8512 device supports a total of twelve SGMII/SerDes MAC interfaces when the operating modes is set to Mode 1 with register 19G [15:14] = '01' for SGMII/SerDes to CAT5 mode to meet the maximum twelve external SGMII/SerDes MACs.
- For detailed pin numbers, descriptions, and connections of the twelve SGMII/SerDes MAC interfaces, see Table 5-2, Figure 5-2, and Figure 5-3.

TABLE 5-2: TWELVE SGMII/SERDES MAC INTERFACES PINS

SGMII/SerDes Port #	Pin Name	Pin Number	Type	Description
0, 3, 6, 9	SERDES_E[0:3]_RXN	AF21, AF17, AF13, AF9	I, DIFF	SGMII/SerDes MAC receiver input pairs
	SERDES_E[0:3]_RXP	AE21, AE17, AE13, AE9	I, DIFF	
	SERDES_E[0:3]_TXN	AA21, AA17, AA13, AA9	O, DIFF	SGMII/SerDes MAC transmitter output pairs
	SERDES_E[0:3]_TXP	Y21, Y17, Y13, Y9	O, DIFF	
1, 2, 4, 5, 7, 8, 10, 11	SERDES[0:7]_RXN	AF19, AF18, AF15, AF14, AF11, AF10, AF7, AF6	I, DIFF	SGMII/SerDes MAC receiver input pairs
	SERDES[0:7]_RXP	AE19, AE18, AE15, AE14, AE11, AE10, AE7, AE6	I, DIFF	
	SERDES[0:7]_TXN	AA19, AA18, AA15, AA14, AA11, AA10, AA7, AA6	O, DIFF	SGMII/SerDes MAC transmitter output pairs
	SERDES[0:7]_TXP	Y19, Y18, Y15, Y14, Y11, Y10, Y7, Y6	O, DIFF	

5.2.1 SGMII/SERDES MAC INTERFACE TO EXTERNAL SGMII/SERDES MAC

- For design connections of the twelve SGMII/SerDes MAC interfaces, see Figure 5-2 and Figure 5-3.

FIGURE 5-2: FOUR SGMII/SERDES MAC INTERFACES TO SGMII/SERDES MAC CONNECTIONS USING ENHANCED SERDES INTERFACES

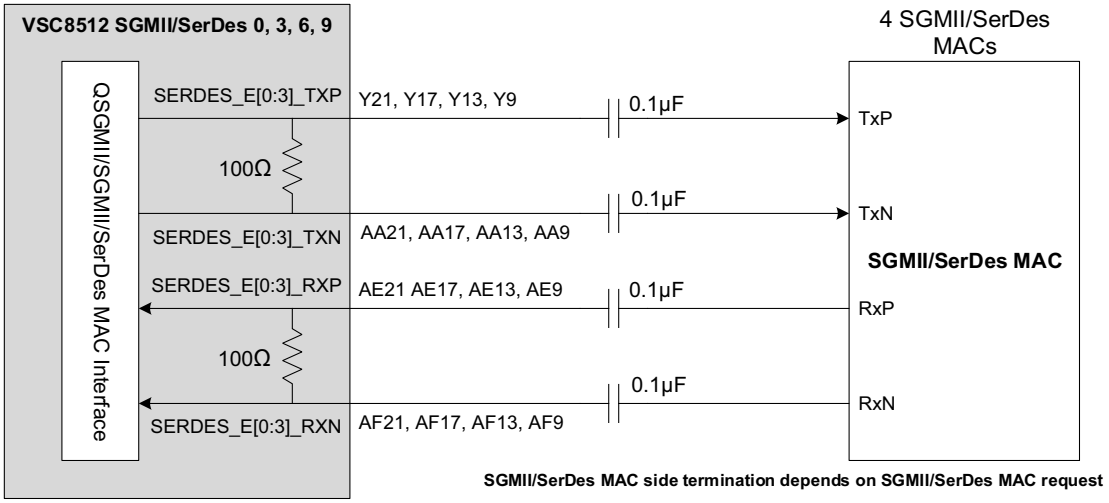
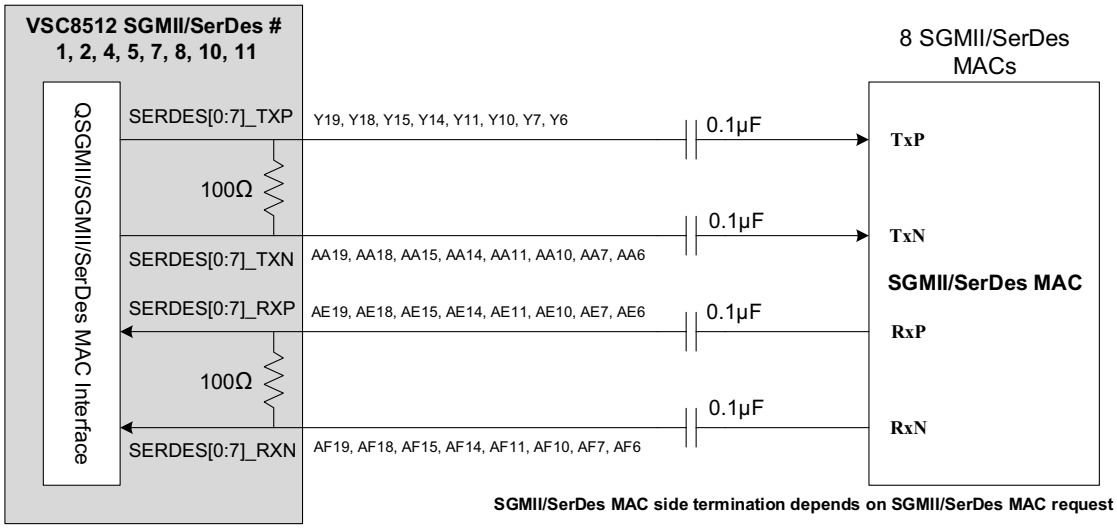


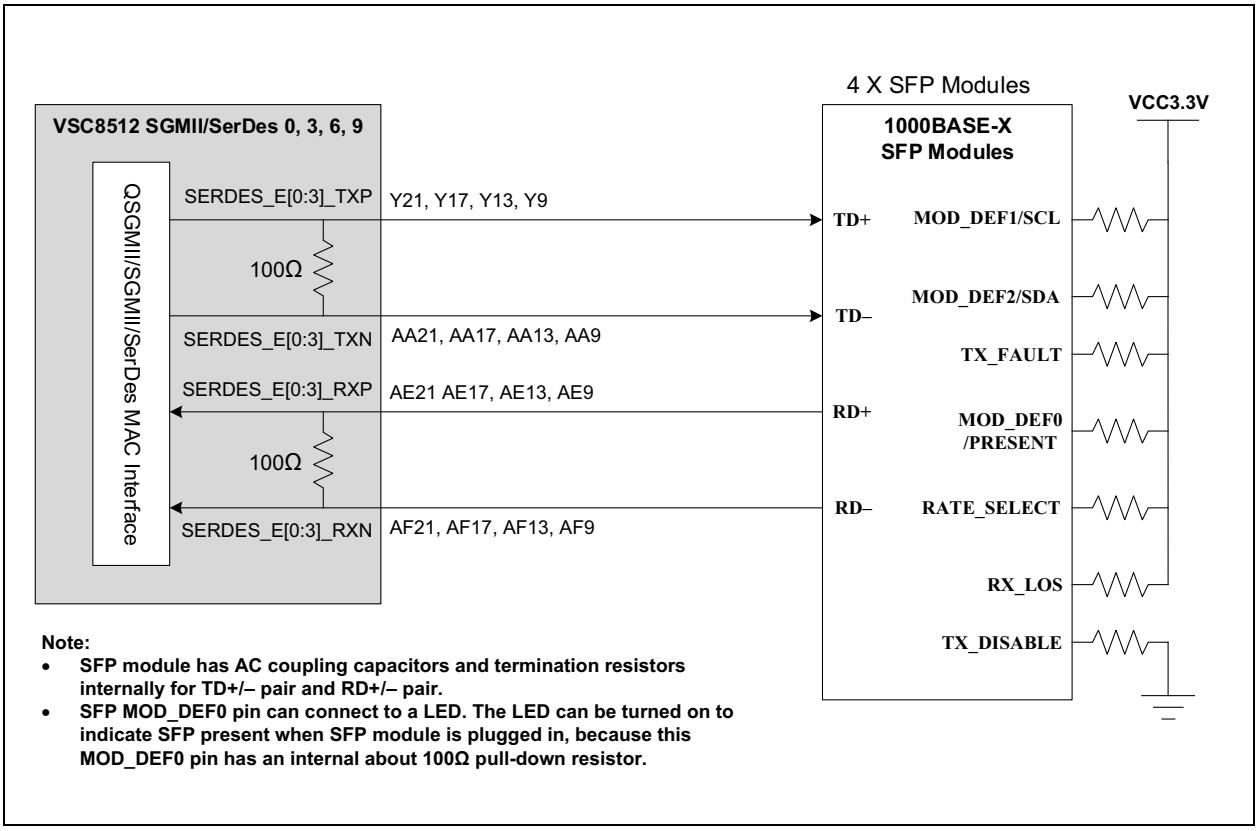
FIGURE 5-3: EIGHT SGMII/SERDES MAC INTERFACES TO SGMII/SERDES MAC CONNECTIONS



5.2.2 SERDES MAC INTERFACE TO SFPS

- When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8512 device provides data throughput at a rate of 1000 Mbps only. 10 Mbps and 100 Mbps rates are not supported.
- Figure 5-4 and Figure 5-5 show the SerDes MAC interface connection to 1000BASE-X SFP.

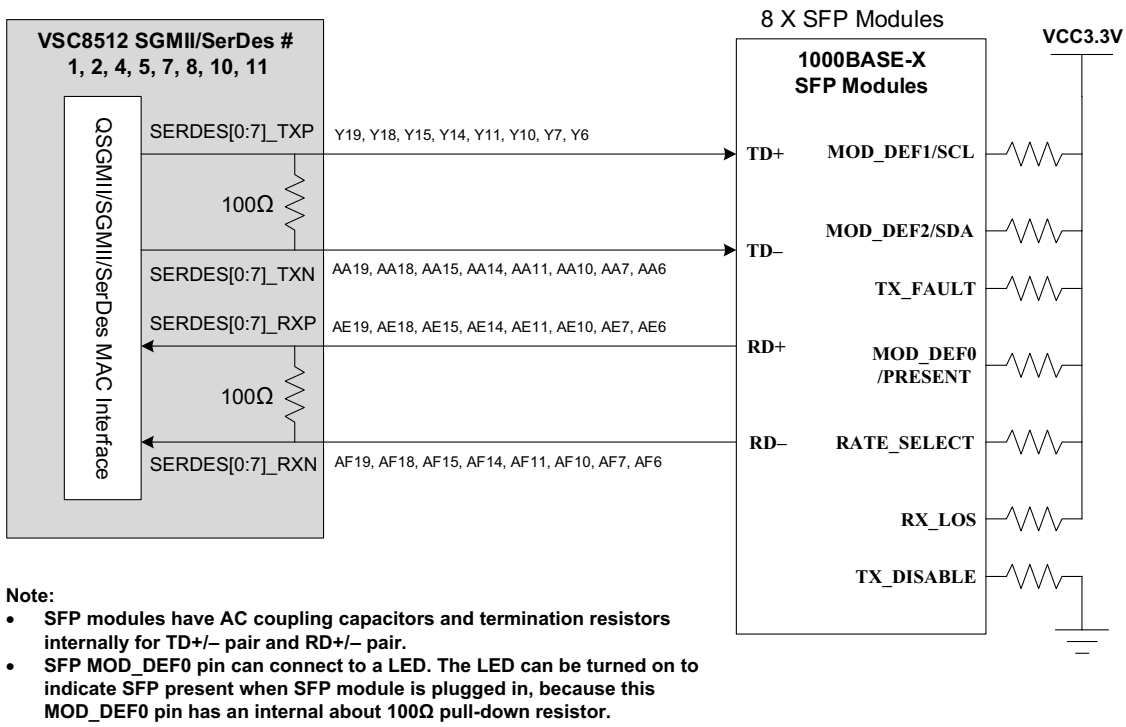
FIGURE 5-4: FOUR SGMII/SERDES MAC INTERFACES TO 1000BASE-X SFP CONNECTIONS USING ENHANCED SERDES INTERFACES



Note:

- **SFP module has AC coupling capacitors and termination resistors internally for TD+/– pair and RD+/– pair.**
- **SFP MOD_DEF0 pin can connect to a LED. The LED can be turned on to indicate SFP present when SFP module is plugged in, because this MOD_DEF0 pin has an internal about 100Ω pull-down resistor.**

FIGURE 5-5: EIGHT SGMII/SERDES MAC INTERFACES TO 1000BASE-X SFP CONNECTIONS



Note:
- **SFP modules have AC coupling capacitors and termination resistors internally for TD+/– pair and RD+/– pair.**
- **SFP MOD_DEF0 pin can connect to a LED. The LED can be turned on to indicate SFP present when SFP module is plugged in, because this MOD_DEF0 pin has an internal about 100Ω pull-down resistor.**

5.3 SerDes Media Interface

- The VSC8512 device supports four SerDes media interfaces when the operating modes is set to Mode 2 with register 19G [15:14] = ‘10’ for SerDes media interface. The interface provides full-duplex or half-duplex 100BASE-FX/1000BASE-X operation, as well as protocol conversion for 10/100/1000BASE-T copper SFP devices.
- The configuration can implement QSGMII to1000BASE-X, 100BASE-FX, and 10/100/1000BASE-T application.
- For detailed pin numbers, descriptions, and connections of four SerDes media interfaces, see Table 5-3, Figure 5-6, and Figure 5-7.

TABLE 5-3: FOUR SERDES MEDIA INTERFACES PINS

Fiber Port #	Pin Name	Pin Number	Type	Description
SERDES [4:7] is for Fiber #11, 10, 9, 8	SERDES[4:7]_RXN	AF11, AF10, AF7, AF6	I, DIFF	SerDes media receiver input pairs
	SERDES[4:7]_RXP	AE11, AE10, AE7, AE6	I, DIFF	
	SERDES[4:7]_TXN	AA11, AA10, AA7, AA6	O, DIFF	SerDes media transmitter output pairs
	SERDES[4:7]_TXP	Y11, Y10, Y7, Y6	O, DIFF	

FIGURE 5-6: FOUR SERDES MEDIA INTERFACES TO 1000BASE-X OR 1000BASE-T CONNECTIONS

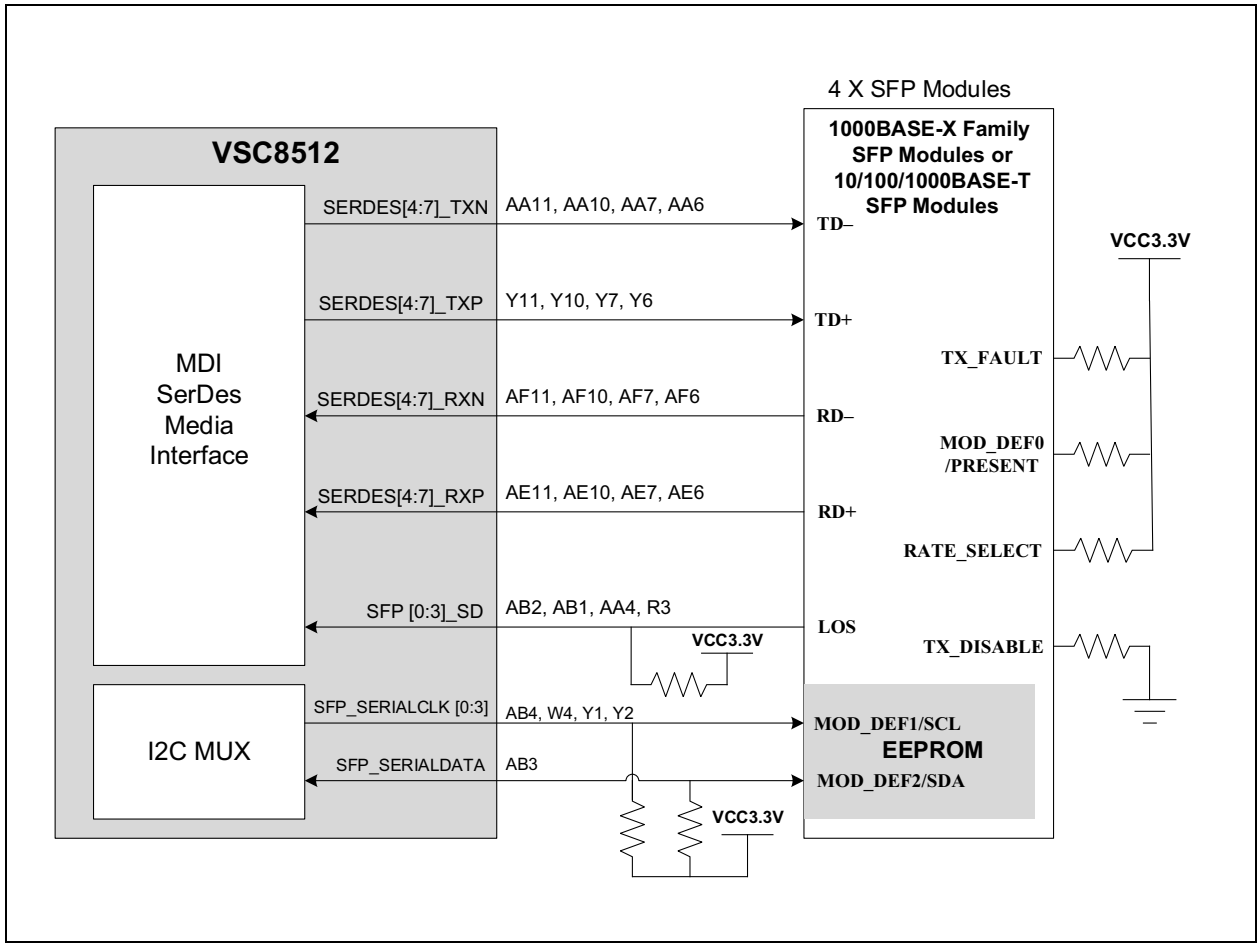
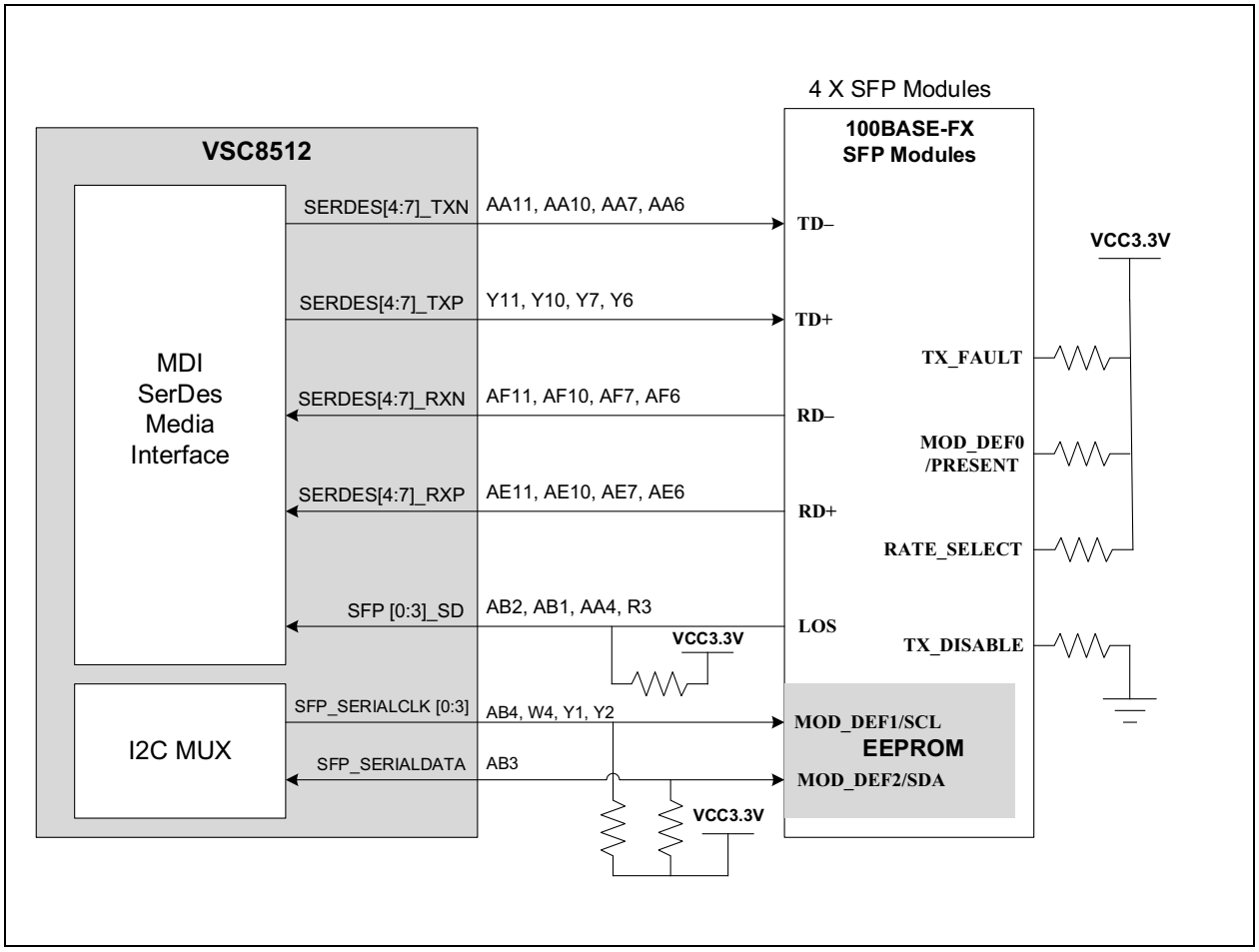


FIGURE 5-7: FOUR SERDES MEDIA INTERFACES TO 100BASE-FX CONNECTIONS



5.4 QSGMII/SGMII/SerDes MAC Design Rules

- Use AC coupling with 0.1 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If the SGMII/SerDes port is unused, both the **RDx** pair and **TDx** pair pins can be left floating (No Connect).

6.0 DEVICE CLOCKS

The VSC8512 device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements of this interface.

6.1 Reference Clock Information

- Refer to Table 6-1 for pin numbers and more information.

TABLE 6-1: REFERENCE CLOCK RELATED PINS

Pin Name	Pin Number	Type	Description
REFCLK_N	AA8	I, ADIFF	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on REFCLK_SEL[2:0] input state.
REFCLK_P	Y8	I, ADIFF	
REFCLK_SEL[0:2]	C12, C13, C14	I, PD	Reference clock frequency select.

- The VSC8512 supports multiple reference clock input frequencies options through the strap pins [C12, C13, C14] of strap pins REFCLK_SEL [0:2] to select system clock frequency. See Table 6-2 for detail strap options.

TABLE 6-2: REFCLK FREQUENCY SELECTION

REFCLK_SEL [0:2]	Clock Frequency	Configurations
000	125 MHz	Keep all strap pins in default their value
001	156.25 MHz	REFCLK_SEL2 pin C14 is pulled up by pull-up resistor
100	25 MHz	REFCLK_SEL0 pin C12 is pulled up by pull-up resistor

When reference clocks are used, ensure that:

- The jitter requirements in the data sheet are met.
- The amplitude specifications in the data sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 µF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC8512 side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- Unused strap pins can be left floating (No Connect).

6.2 Single-Ended REFCLK Circuit Design

- To use a single-ended REFCLK, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK are shown in Figure 6-1 and Table 6-3.

FIGURE 6-1: SINGLE-ENDED REFCLK CONNECTIONS

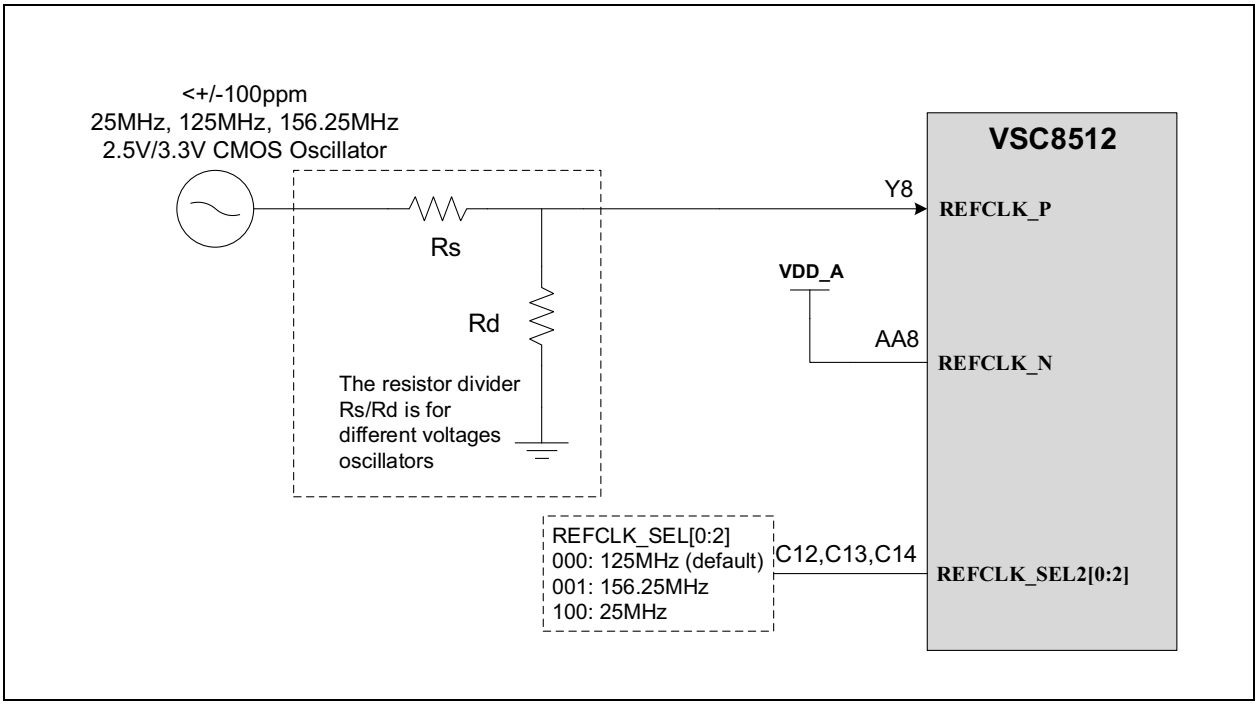


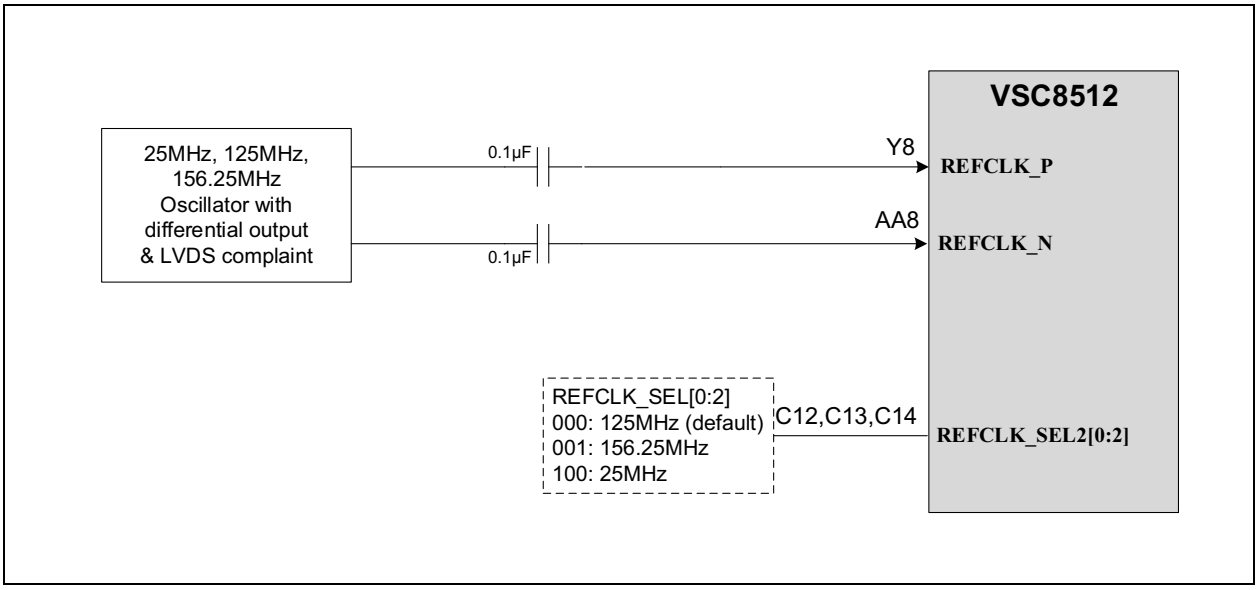
TABLE 6-3: SINGLE-ENDED REFCLK INPUT RESISTOR DIVIDER

Oscillator CMOS Output Voltage	Resistor Divider Rs Value (Ω)	Resistor Divider Rd Value (Ω)
2.5V	220	910
3.3V	270	430

6.3 Differential REFCLK Circuit Design

- AC-coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS-compliant.
- The configurations for differential REFCLK are shown in Figure 6-2.

FIGURE 6-2: DIFFERENTIAL REFCLK CONNECTIONS



6.4 Media Recovered Clock Output

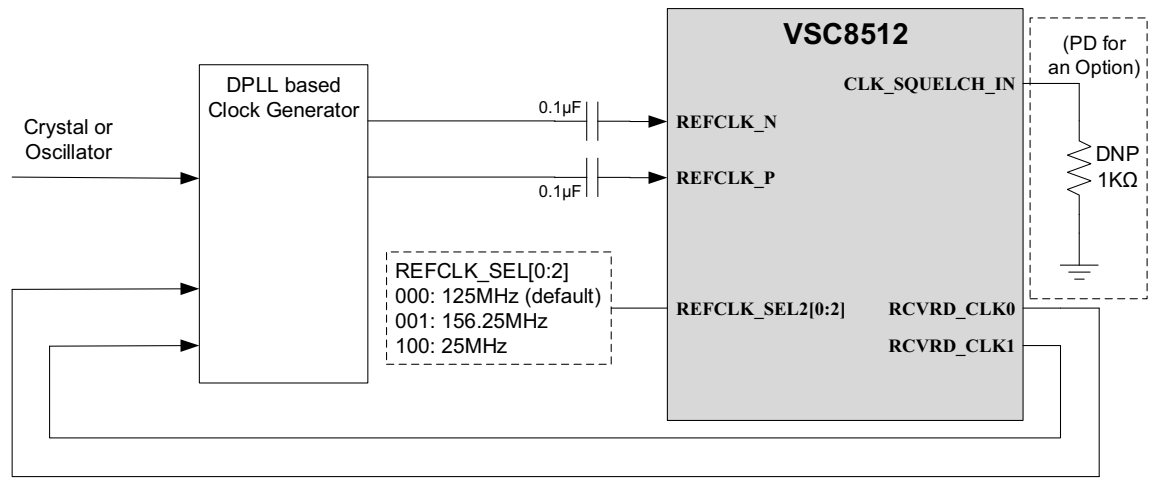
For Synchronous Ethernet applications, the VSC8512 includes two recovered clock output pins. Refer to Table 6-4 for pin numbers and more information.

TABLE 6-4: REFERENCE CLOCK RELATED PINS

Pin Name	Pin Number	Type	Description
RCVRD_CLK0	AE2	O	Recovered clock frequency select. These pins are not active when NRESET is asserted. Clock outputs can be enabled or disabled using registers 23G and 24G. When disabled, the pin is held low.
RCVRD_CLK1	AD3	O	
CLK_SQUELCH_IN	Y3	I/O, PU	This pin is the input control to squelch the recovered clock. The CLK_SQUELCH_IN pin controls the squelching of the clock. Both RCVRD_CLK0 and RCVRD_CLK1 are squelched when the CLK_SQUELCH_IN pin is high. An external pull-down resistor is required for Synchronous Ethernet applications, in order to output either of the recovered clocks.

- When using Synchronous Ethernet applications, see Figure 6-3 for reference.

FIGURE 6-3: TYPICAL SYNCHRONOUS ETHERNET CLOCK CONFIGURATION



Note:
- **One or both RCVRDCLK recovered clocks**
- **CLK_SQUELCH_IN pin has internal pull-up (PU) to squelch the RCVRDCLK1/2 outputs always, add a pull-down (PD) DNP resistor in design to disable squelch as an option if using the recovered clocks.**

7.0 DIGITAL INTERFACE AND I/O

7.1 Serial Management Interface (SMI) Pins

- The VSC8512 device includes an IEEE 802.3-compliant serial management interface (SMI) that is controlled by its **MDC**, **MDIO**, and **MDINT** pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.
- The SMI is a synchronous serial interface with input data to the VSC8512 on the MDIO pin that is clocked on the rising edge of the **MDC** pin. The output data is sent on the **MDIO** pin on the rising edge of the MDC signal. The interface can be clocked at a rate from minimum kHz, typical 2.5 MHz to maximum 12.5 MHz, depending on the total load on MDIO. An external 2 kΩ pull-up resistor is recommended on the **MDIO** pin when using maximum 12.5 MHz MDC clock. If using 2.5 MHz or less MDC frequency, it is acceptable to use 10 kΩ pull-up resistor for the **MDIO** pin. See Table 7-1 for SMI interface pin numbers and more information.

TABLE 7-1: SMI INTERFACE PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
MDC	AF4	I	A maximum of 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	AF3	I/O, OD	Serial data is written or read from this pin bidirectionally between the PHY and the station manager synchronously on the positive edge of MDC. One external pull-up resistor is required. The pull-up resistor should be tied to the VDD_IO power, and its value depends on the MDC clock frequency.
MDINT	C10	I/O, OD, OS	This pin is the Management interrupt signal. This output is open-drain and requires an external pull-up resistor. It may be wired-OR with other open-drain interrupt signals. If MDINT is unused, it may be left unconnected, without a resistor.

7.2 GPIO Pins

- The VSC8512-11 provides 30 multiplexed multipurpose pins. Eight multiplexed general-purpose pins are related with input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers with ‘G’, for example register 13G. Table 7-2 shows all GPIO pins of the VSC8512.
- These GPIO pins have internal pull-up (PU). Any unused GPIO pins can be left floating (No Connect).

TABLE 7-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL

Pin Name	Pin Number	Type	Description
GPIO_2	AB2	I/O, PU	General purpose I/O
GPIO_3	AB1	I/O, PU	General purpose I/O
GPIO_4	AA4	I/O, PU	General purpose I/O
GPIO_13	W3	I/O, PU	General purpose I/O
GPIO_14	W2	I/O, PU	General purpose I/O
GPIO_15	W1	I/O, PU	General purpose I/O
GPIO_16	V4	I/O, PU	General purpose I/O
GPIO_29	R3	I/O, PU	General purpose I/O

7.3 JTAG Pins

- If JTAG is not used, **TRST** should be pulled low. The other pins may be left floating (No Connect). See Table 7-3 for JTAG pin information.

TABLE 7-3: JTAG PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
JTAG_CLK	D17	I, PU	Boundary scan, test clock input. Internally pulled high.
JTAG_DI	D18	I, PU	Boundary scan, test data input. Internally pulled high.
JTAG_DO	D19	O	Boundary scan, test data output
JTAG_TMS	D20	I, PU	Boundary scan, test mode selects. Internally pulled high.
JTAG_TRST	CD21	I, PU	Boundary scan, test Reset input. Internally pulled high. **Note:** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation.

8.0 MISCELLANEOUS

8.1 Reset

- The VSC8512 must be reset at power-up. One option is to hold **NRESET** low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **NRESET** low for a minimum of 2 ms after power-up. **NRESET** is typically driven by a voltage monitor device or by the management processor or FPGA. See Table 8-1 for more information on the reference clocks.

TABLE 8-1: RESET PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
nRESET	C4	I	Reset. Active low input that powers down the device and sets all register bits to their default state.

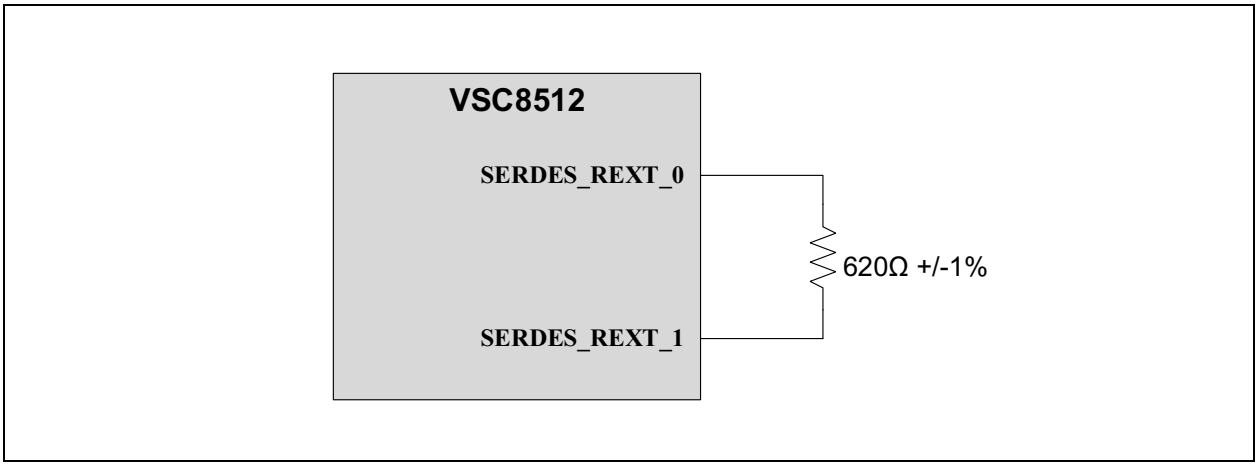
8.2 Reference Resistor

- Connect a 620Ω ±1% resistor between **SERDES_REXT_0** and **SERDES_REXT_1** as shown in Figure 8-1. See Table 8-2 for additional details on the pins.

TABLE 8-2: REFERENCE RESISTOR DESCRIPTIONS

Pin Name	Pin Number	Level	Description
SERDES_REXT_0	AE22	Analog	SerDes bias pins. Connect to a 620Ω 1% resistor.
SERDES_REXT_1	AF22	Analog	

FIGURE 8-1: SERDES BIAS RESISTOR



8.3 LED Pins

- The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits [13:10]. The default polarity is active low. The register 25G can be configured for different LED modes.
- The VSC8512 LED pins are for 12-port status. Each VSC8512 PHY port can support two single-colored LEDs of LED0 and LED1.
- The use of 330Ω current limit resistor and VDD_IO for LED power are recommended.
- Refer to Table 8-3 for details LED pins information.

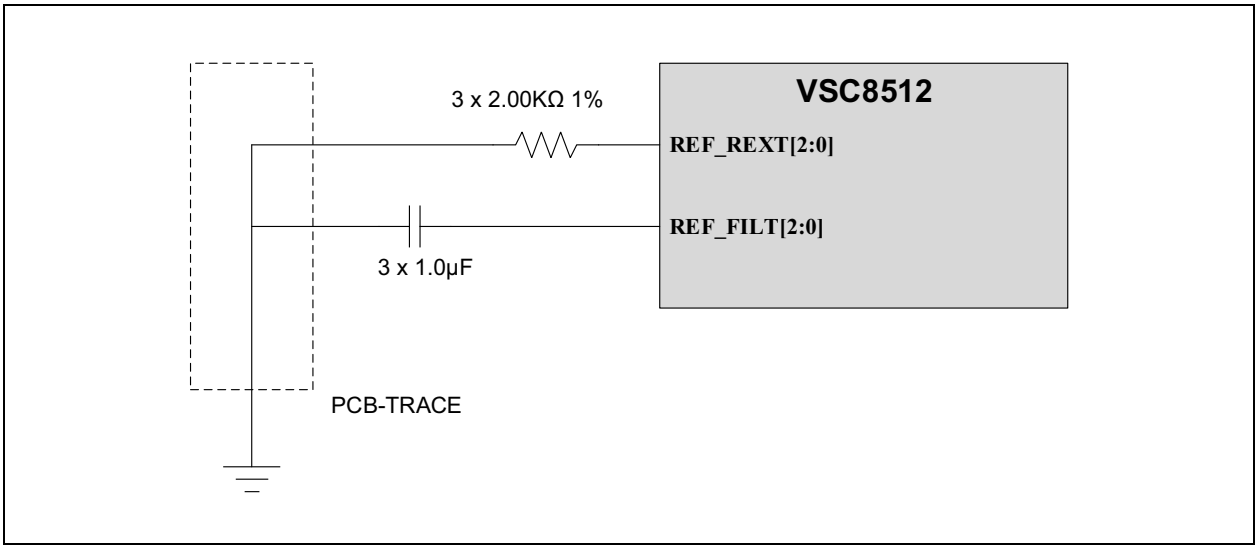
TABLE 8-3: LED PINS AND BASIC DEFAULT FUNCTION

Pin Name	Pin Number	Type	Description
PHY[0:11]_LED0	V3, V2, V1, U4, U3, U2, U1, T4, T3, T2, T1, R4	O	LED0 is for PHY [0:11]. LED0 default is LED mode 1 for link 1000/Activity, and LED mode can be changed by register 29 bits [3:0]. Refer to the data sheet for detail 0-15 LED modes.
PHY[0:11]_LED1	AA3, AA2, AA1, Y4, Y3, Y2, Y1, W4, W3, W2, W1, V4	O	LED1 is for PHY [0:11]. LED1 default is LED mode 2 for link 100/Activity, and LED mode can be changed by register 29 bits [7:4]. Refer to the data sheet for detail 0-15 LED modes.

8.4 Analog Bias Pins

- The **REF_REXT[2:0]** pin (pin K4, E13, and K23) on the VSC8512 device should connect to the system ground through three 2 kΩ resistors with a tolerance of 1.0% and minimum 1/16W. The pins are used to set up critical bias currents for the Ethernet physical device.
- The **REF_FILT[2:0]** pin (pin L4, E14, and L23) on the VSC8512 device should connect to the system ground through three 1 µF capacitor with 10% tolerance; NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in Figure 8-2. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8512.

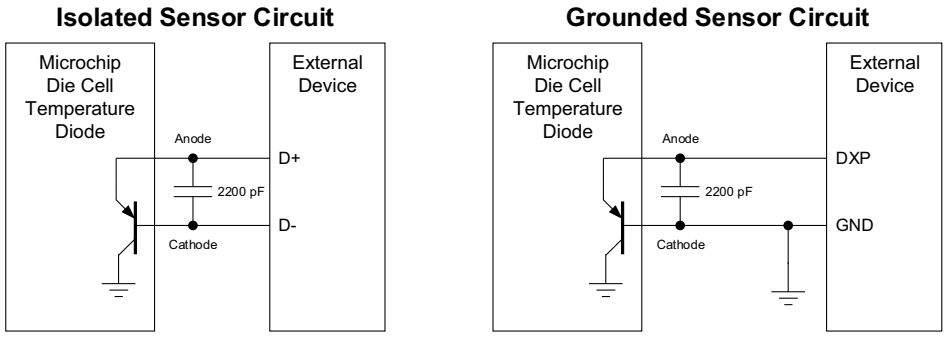
FIGURE 8-2: VOLTAGE REFERENCE SCHEMATIC



8.5 Temperature Sensor Diode

- The temperature sensor diode pins provide access to an on-die diode and internal circuitry for monitoring die temperature. To use it, connect an external thermal sensor located on the board or in a stand-alone measurement kit. The feature can be as an option in application.
- The **THERMDA** pin (pin C23) is the Thermal Diode Anode pin, which needs to be pulled down by a pull-down resistor if not used.
- The **THERMDC_VSS** pin (pin C22) is the Thermal Diode Cathode pin connected to system ground. The temperature sensor must be chosen accordingly. This pin needs to be pulled down by a pull-down resistor if not used.
- Temperature measurement using a thermal diode is very sensitive to noise. Figure 8-3 illustrates a generic application design.

FIGURE 8-3: THERMAL DIODE CONNECTIONS



Note: Microchip does not support or recommend operation of the thermal diode under reverse bias.

8.6 PHY Address Pins

- The VSC8512 device includes three external PHY address pins, **PHYADD [4:3]**, to allow control of multiple PHY devices on a system board sharing a common management bus. The VSC8512-02 includes two external PHY address pins to allow control of multiple PHY devices on a system board that are sharing a common management bus. Based on the settings of these two address control pins, the internal PHYs in the VSC8512-02 device take on the address ranges as shown in Table 8-4.

TABLE 8-4: PHY ADDRESS PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
PHYADD3	C7	I, PD	PHYADD [4:3] PHY address range select for accessing each PHY's register through SMI interface. PHY Address Range Selection PHYADD [4:3], Internal PHY Addresses 00: 0-11 01: 12-23 10: 4-15 11: 20-31
PHYADD4	C8	I, PD	

8.7 Other Pins

- The **COMA_MODE** (pin C3), when asserted high, all PHYs are held in a powered down state; and when deasserted low, all PHYs are powered up and resume normal operation. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of reset. Hence, this pin should be pulled down by a pull-down resistor.
- The **FAST_LINK_STATUS** (pin R1) provides a Fast Link Failure indication signal. If this feature is not used, this pin should be pulled down by a pull-down resistor.

8.8 Unused and No Connection Pins

- The **RESERVED_[3:8, 10:15, 22:29, 201:209, 211:221, 223, 225, 232:237, 240:248]** pins (pins C9, C11, C18, C17, C16, C15, G23, H23, D14, D13, H4, G4, AE8, AF8, P4, AD1, AD2, AC1, AC2,C10, C19, C20, C21, C24, D3, D6, D7, D8, D9, D12, D15, D22, D23, D24, E3, E24, F3, F13, F14, F24, G14, H14, J14, J15, J16, J17, J18, J19, J8, J9, J10, J11, J12, J13, H13, G13, and D10) are reserved signal. Leave them unconnected.
- The **NC** pins (pins AA23, AA24, AA25, AA26, AB23, AB24, AB25, AB26, AC23, AC24, AC25, AC26, AD24, AD25, AD26, AE25, C5, R23, R24, R25, R26, T23, T24, T25, T26, U23, U24, U25, U26, V23, V24, V25, V26, W23, W24, W25, W26, Y23, Y24, Y25, and Y26) are unconnected pins. Leave them floating.

8.9 General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 kΩ resistor is recommended to use.
- If there is no pull-down resistor value specified, a 1 kΩ or 4.7 kΩ resistor is recommended to use.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Refer to Table 3-1 and Table 3-2 to ensure that the power pins are correct. Select the correct power supply components with at least about 25-30% margin for the system power consumption.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection and filtering.		
	Section 3.4, "Decoupling Capacitors"	If doing PCB layout, see this section for the bulk decoupling capacitor required.		
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pins connection for quad-port circuit design based on product design requirement to select the design according to Figure 4-1 or Figure 4-2.		
	Section 4.2, "10/100/1000 Magnetics Connection and RJ45 Connection"	Verify the magnetics and the Common-mode capacitors connection based on Figure 4-1 or Figure 4-2.		
	Section 4.3, "PCB Layout Considerations"	Refer to this section for PCB layout design reference to check if the Gigabit copper port PCB layout request is met.		
Section 5.0, "QSGMII/SGMII SerDes Interfaces"	Section 5.1, "QSGMII MAC"	Refer to Table 5-1 and Figure 5-1 to check if correct pins are used for the three QSGMII MAC interfaces design with correct connection.		
	Section 5.2, "SGMII/SerDes MAC"	Refer to Table 5-2 to check if correct pins are used for the 12 SGMII/SerDes MAC interfaces.		
	Section 5.2.1, "SGMII/SerDes MAC Interface to External SGMII/SerDes MAC"	Refer to Figure 5-2 and Figure 5-3 to check if correct design is used for SGMII/SerDes MAC interfaces connecting to another end SGMII/SerDes MAC interfaces.		
	Section 5.2.2, "SerDes MAC Interface to SFPs"	Refer to Figure 5-4 and Figure 5-5 to check if correct design is used for SGMII/SerDes MAC interfaces connecting to 1000ASE-X SFPs .		
	Section 5.3, "SerDes Media Interface"	Refer to Table 5-3 to check if correct pins are used for the four SerDes media interfaces. Refer to Figure 5-6 for design using four 1000BASE-X or 1000BASE-T SFPs. Refer to Figure 5-7 for design using four 100ASE-FX SFPs.		
	Section 5.4, "QSGMII/SGMII/SerDes MAC Design Rules"	For SerDes QSGMII MAC interface PCB layout, follow the SerDes design rules requirement in this partial PCB layout.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Device Clocks"	Section 6.1, "Reference Clock Information"	Refer to Table 6-1 and Table 6-2 to select the reference clock frequency and correct clock related pins.		
	Section 6.2, "Single-Ended REFCLK Circuit Design"	Refer to Figure 6-1 and Table 6-3 for correct single-ended clock circuit design.		
	Section 6.3, "Differential REFCLK Circuit Design"	Refer to Figure 6-2 for correct differential clock circuit design.		
	Section 6.4, "Media Recovered Clock Output"	Refer to Table 6-4 and Figure 6-3 for a typical recovered clock circuit design and for correct usage of recovered clock pins and correct configuration.		
Section 7.0, "Digital Interface and I/O"	Section 7.1, "Serial Management Interface (SMI) Pins"	Refer to Table 7-1 and the descriptions in this section for SMI interface circuit design.		
	Section 7.2, "GPIO Pins"	Refer to Table 7-2 and the descriptions in this section for all GPIO pins in the circuit design.		
	Section 7.3, "JTAG Pins"	Refer to Table 7-3 and the descriptions in this section for all JTAG pins in the circuit design.		
Section 8.0, "Miscellaneous"	Section 8.1, "Reset"	Refer to Table 8-1 and check if the designed reset circuit meets the reset time requirement.		
	Section 8.2, "Reference Resistor"	Refer to Figure 8-1 and make sure to connect a 620Ω ±1% resistor between the **SERDES_REXT_0** pin and the **SERDES_REXT_1** pin.		
	Section 8.3, "LED Pins"	Check if correct LED pins are used based on Table 8-3, current limit resistors, and LED power.		
	Section 8.4, "Analog Bias Pins"	Refer to Figure 8-2 and check if correct pull-down resistor value for **REF_REXT [2:0]** pins is used. Check if correct pull-down capacitor value for **REF_FILT [2:0]** pins is used.		
	Section 8.5, "Temperature Sensor Diode"	If designing with the temperature sensor diode, see Figure 8-3 as the design reference.		
	Section 8.6, "PHY Address Pins"	Check if the correct PHY address pins are used based on Table 8-4 to configure the correct PHY address the design requires.		
	Section 8.7, "Other Pins"	For **COMA_MODE** and **FASTLINK_STATUS** pins, check this section for the correct design.		
	Section 8.8, "Unused and No Connection Pins"	Verify all reserved pins and NC pins are unconnected.		
	Section 8.9, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004697A (08-03-22)	Initial release	

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