



**MICROCHIP**

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**Chip-Scale Atomic Clock (CSAC)  
SA65 User's Guide**

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## Preface

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Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXXXXA”, where “XXXXXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics, to open a list of available online help files.

### PURPOSE OF THIS GUIDE

The CSAC user's guide provides basic recommendations for designing products to use Microchip's Chip-Scale Atomic Clock (CSAC) SA65. The guidelines in the document are generic because specific product requirements vary from one application to the other.

This material consists of a brief description of CSAC design supported by block diagrams, description of environmental issues, installation guidelines, and unit operation.

### WHO SHOULD READ THIS GUIDE

This document is intended for engineers and telecommunications professionals who are designing, installing, operating, or maintaining time, frequency, and synchronization systems having a requirement for a low profile and highly precise frequency generator.

To use this document effectively, you should have a good understanding of digital telecommunications technologies and analog frequency generation and synthesis techniques.

### DOCUMENT LAYOUT

This guide contains the following sections:

- **Chapter 1. “Product Overview”**: Provides an overview of the product, describes the major hardware and software features, and lists the system specifications.
- **Chapter 2. “Functional Description”**: Contains the Principle of Operation, Start-Up Sequence, and aspects related to first power-up.
- **Chapter 3. “Programmer’s Reference”**: Provides an overview of the telemetry interface and command structure.
- **Chapter 4. “Development Kit”**: Describes the package contents, evaluation board information, and how to use the Clockstudio™ software.
- **Chapter 5. “Design Guide”**: Contains information about disciplining, heat sinking, soldering, and additional notes about the evaluation board.

# CSAC SA65 User's Guide

## CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

### DOCUMENTATION CONVENTIONS

Description	Represents	Examples
<b>Arial font:</b>		
Italic characters	Referenced books	<i>MPLAB<sup>®</sup> IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File&gt;Save</i></u>
Bold characters	A dialog button	Click <b>OK</b>
	A tab	Click the <b>Power</b> tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
<b>Courier New font:</b>		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets [ ]	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: {   }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

## WARNINGS, CAUTIONS, RECOMMENDATIONS, AND NOTES

Warnings, Cautions, Recommendations, and Notes attract attention to essential or critical information in this guide. The types of information included in each are displayed in a style consistent with the examples below.

### WARNING

To avoid serious personal injury or death, do not disregard warnings. All warnings use this style. Warnings are installation, operation, or maintenance procedures, practices, or statements that, if not strictly observed, may result in serious personal injury or even death.

### CAUTION

To avoid personal injury, do not disregard cautions. All cautions use this style. Cautions are installation, operation, or maintenance procedures, practices, conditions, or statements, that if not strictly observed, may result in damage to, or destruction of, the equipment. Cautions are also used to indicate a long-term health hazard.

**Note:** All notes use this style. Notes contain installation, operation, or maintenance procedures, practices, conditions, or statements that alert you to important information, which may make your task easier or increase your understanding.

## WHERE TO FIND ANSWERS TO PRODUCT AND DOCUMENT QUESTIONS

For additional information about the products described in this guide, please contact your Microchip representative or your local sales office. You can also contact us on the web at [www.microchip.com/csac](http://www.microchip.com/csac).

When this manual is updated the latest version will be available for downloading from Microchip's web site. Manuals are provided in PDF format for ease of use. After downloading, you can view the manual on a computer or print it using Adobe Acrobat Reader.

Manual updates are available at: [www.microchip.com/csac](http://www.microchip.com/csac).

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San Jose, CA 95134

Toll-free in North America: 1-888-367-7966

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- Technical Support

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Technical support is available through the website at:

<http://www.microchip.com/support>.

## DOCUMENT REVISION HISTORY

### Revision A (May 2021)

- Initial release of this document as Microchip DS50003159A.

### Revision B (June 2021)

- Updated the note box in **Section 3.3.12 “Set HeaterBoostLimit (.)”**.

### Revision C (August 2022)

- Updated **Section 2.6 “Frequency Steering”**.
- Updated **Section 2.7 “1 PPS Output”**.
- Added **Section 2.8 “Time-Interval Counter”**.
- Added Figure 2-6.
- Updated **Section 2.10 “1 PPS Disciplining”**.
- Added Figure 2-7.
- Updated **Section 2.12 “Time-of-Day”**.
- Updated the first Note in **Section 2.14 “Ultra-Low Power Operating Mode”**.
- Updated **Section 3.3.1 “Telemetry (6 and ^)”**.
- Updated Table 3-3.
- Updated Table 3-5.
- Updated **Section 3.3.2 “Frequency Adjustment (F)”**.
- Updated **Section 3.3.4 “1 PPS Synchronization (S)”**.
- Updated **Section 3.3.6 “Set Volatile 1 PPS Disciplining Time Constant (d)”**.
- Updated **Section 3.3.8 “Set Ultra-Low Power Mode Parameters (U)”**.
- Updated **Section 4.2 “Evaluation Board Overview”**.
- Updated **Section 4.4 “Clockstudio Software Information”**.

### Revision D (April 2025)

- Updated support contact information
- Updated figures to represent the current Clockstudio software interface
- Updated **Section 2.7 “1 PPS Output”** and **Section 3.3.10 “Set Threshold for DiscOK Indicator (m)”** regarding 1 PPS output width options
- Updated **Chapter 4. “Development Kit”** to include images and information regarding the CSAC Development Kit.

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## Chapter 1. Product Overview

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### 1.1 INTRODUCTION

The Microchip Model SA65 Chip-Scale Atomic Clock (CSAC) is the world's smallest, lowest power atomic clock technology. This user's guide provides the basic guidelines and recommendations for designing products with the CSAC. These are generic and should be tailored for each application.

This document is intended for engineers, technicians, and technologists who are designing, installing, operating or maintaining time, frequency, and synchronization systems. The CSAC is a low-profile, highly precise frequency generator. To use this document effectively, an understanding of digital communication technologies is required. It is advantageous to have a background in frequency generation and synthesis techniques.

### 1.2 SA65 OVERVIEW

The Microchip CSAC SA65 provides the accuracy and stability of atomic clock technology with reduced size, weight, and power consumption. The small size (less than 17 cc) and low power consumption of the CSAC (less than 125 mW) enable atomic timing accuracy in portable, battery-powered applications.



**FIGURE 1-1:** *Microchip SA65 Chip-Scale Atomic Clock (CSAC).*

The CSAC provides RF and 1 PPS outputs at standard CMOS levels. It accepts a 1 PPS input to synchronize the output to within 100 ns of a reference clock. It can also discipline its phase and frequency to within 1 ns and  $1 \times 10^{-12}$  of the reference clock, respectively.

This user's guide provides engineering information for use of the CSAC. It also provides supporting information for use of the CSAC Developer Kit (part number 090-04326-000). The design details of the developer's kit can be used to assist with host system design (for example, power conditioning or signal buffering). This guide must be used in conjunction with the current data sheet for CSAC SA65, which is available on the Microchip website at [www.microchip.com](http://www.microchip.com).

## CAUTION

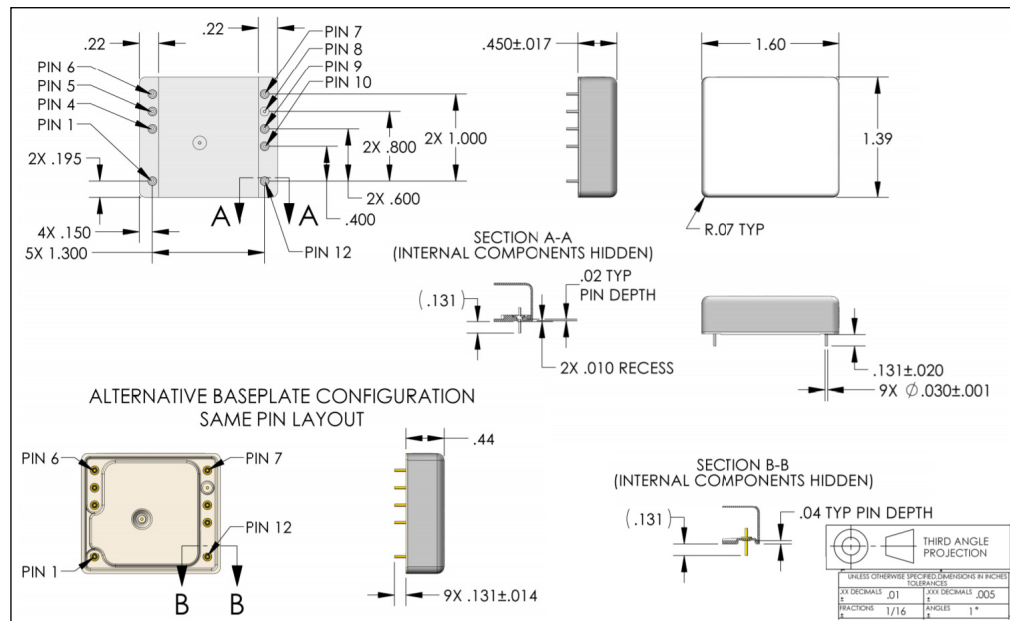
To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

### 1.2.1 Packaging

Retain the original CSAC ESD-safe packaging material in the event that the device needs to be returned to Microchip for service.

### 1.2.2 Mechanical Interface and Mounting Considerations

The physical dimensions of the CSAC are 1.6" x 1.4" x 0.45" H. [Figure 1-2](#) shows the detailed dimensions of CSAC. The CSAC baseplate and cover are 80% nickel-iron magnetic alloy per ASTM A753, Type 4 (Mu-Metal or Hy-Mu80™).



**FIGURE 1-2:** CSAC SA65 Interface Control Drawing.

[Table 1-1](#) shows the pinout of the CSAC.

**TABLE 1-1: CSAC SA65 PINOUT**

Pin	I.D.	Pinout Diagram
1	Tune	
2	N/A	
3	N/A	
4	BITE	
5	Tx	
6	Rx	
7	VCC	
8	GND	
9	1 PPS Input	
10	1 PPS Output	
11	N/A	
12	RF Output	

**Note:** Pins labeled “N/A” are not present in the CSAC.

### 1.2.3 Recommended Operating Characteristics

The CSAC pinout is shown in [Table 1-1](#). The electrical function of each pin is shown in [Table 1-2](#).

**TABLE 1-2: RECOMMENDED OPERATING CHARACTERISTICS**

Pin	Function	Level	Reference Section
1	Analog tuning input (Note 1)	0V to 2.5V	<b>Section 2.13 “Analog Tuning”</b>
4	Built-In Test Equipment (BITE) (Note 2)	LogicH > 2.8V LogicL < 0.3V	<b>Section 2.3 “Built-In Test Equipment (BITE)”</b>
5, 6	Serial Communication	2.8V < LogicH < 3.0V 0V < LogicL < 0.3V	<b>Chapter 3. “Programmer’s Reference”</b>
7	VCC	3.3V ±0.1V	—
8	Ground	—	—
9	1 PPS In (Note 3)	2.5V < LogicH < 3.3V 0V < LogicL < 0.5V	—
10	1 PPS Out (Note 4, Note 5)	LogicH > 2.8V LogicL < 0.3V	<b>Section 2.7 “1 PPS Output”</b>
12	RF Out	LogicH > 2.8V LogicL < 0.3V	<b>Section 2.4 “RF Output Characteristics”</b>

- Note 1:** Analog Tuning Sensitivity is  $\Delta f/f = (V_{TUNE} - 1250 \text{ mV}) \times 1.77 \times 10^{-11}/\text{mV}$ .
- 2:** Built-In Test Equipment: 0 = Normal operation, 1 = Unlock condition.
- 3:** Timing reference is rising edge of input pulse on pin 9.
- 4:** Output 1 PPS pulse duration adjustment depends on CSAC RF output frequency. For 10 MHz CSAC, output pulse is adjustable from 100  $\mu\text{s}$  to 400  $\mu\text{s}$  in 100  $\mu\text{s}$  increments. Output pulse is 100  $\mu\text{s}$  in duration for option 001. Refer to the data sheet for other options. (400  $\mu\text{s}$  for firmware versions 1.06 and earlier).
- 5:** Timing reference is the rising edge of pin 10. Rise time <10 ns at a load capacitance of 10 pF.
- 6:** See the CSAC SA65 data sheet for updated parameters.

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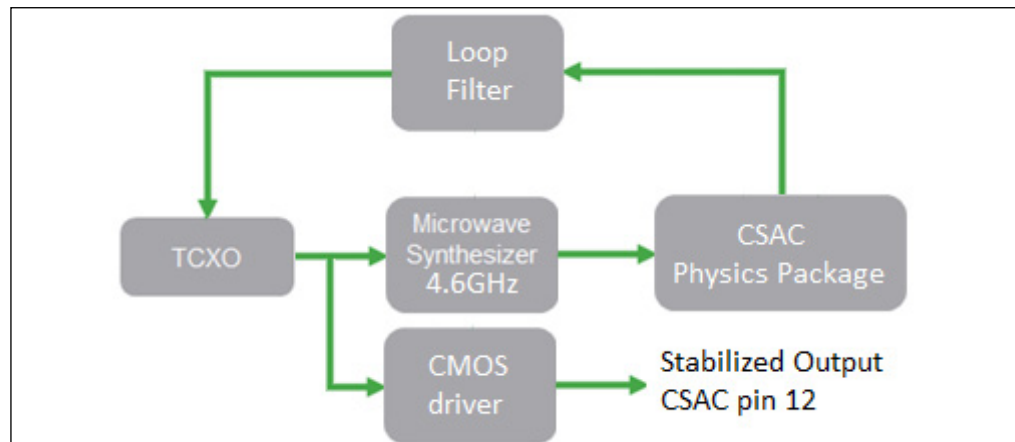
NOTES:

## Chapter 2. Functional Description

The following is a functional description of the CSAC.

### 2.1 PRINCIPLE OF OPERATION

The CSAC is a passive atomic clock, incorporating the interrogation technique of coherent population trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the CSAC architecture is beyond the scope of this user's guide. The following illustration shows a simplified block diagram of the CSAC.



**FIGURE 2-1:** Simplified CSAC Block Diagram.

The principal RF output from the CSAC is provided by a temperature-compensated crystal oscillator (TCXO), which is buffered by a CMOS logic gate and provided on the CSAC output pin 12. In normal operation, the frequency of the TCXO is continuously compared and corrected to the ground state hyperfine frequency of the cesium atoms, contained within the physics package, which thereby improves the stability and environmental sensitivity of the TCXO by four to five orders of magnitude. In addition to the TCXO and the physics package ([Note 1](#)), the essential components of the CSAC are the microwave synthesizer and the microprocessor ([Note 2](#)). The microwave synthesizer generates 4596.3x MHz with tuning resolution of approximately  $1 \times 10^{-12}$ . The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the TCXO, optimization of physics package operation, state-of-health monitoring, and command and control through the serial communications port.

When the CSAC is initially powered on, it performs an acquisition sequence, which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored through the status field of the telemetry (see [Section 3.3.1 “Telemetry \(6 and ^\)”](#)). On power-up, the status begins at 8 (oven warm-up). The status value decrements numerically through the acquisition until normal operation (status = 0) is achieved. On rare occasions, the status countdown will reset during the acquisition. This is normal behavior if it does not disrupt the time-to-lock specification.

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- Note 1:** R. Lutwak, et. al., The Chip-Scale Atomic Clock - Low-Power Physics Package, Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting, December 7–9, 2004, Washington, DC.
- 2:** R. Lutwak, et. al., The MAC - A Miniature Atomic Clock, Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting, August 29–31, 2005, Vancouver, BC.

## 2.2 START-UP SEQUENCE

### CAUTION

**To avoid severe damage to the unit, do not apply power to the incorrect terminals. The CSAC does not have reverse voltage protection.**

When power is connected to pin 7, the CSAC unit begins its warm-up cycle. 10 MHz and 1 PPS output signals appear immediately upon power-up, but the output signals are not stable until the atomic control loop is locked (indicated CMOS\_low on the BITE pin).

Within 3 minutes at 25°C, the CSAC achieves Lock and BITE = 0 (**Section 2.3 “Built-In Test Equipment (BITE)”**). Power consumption during warm-up is greater than during normal operation; as specified on the CSAC data sheet.

It is recommended to always allow CSAC to remain powered on for >102 seconds after it acquires LOCK, after which CSAC will store the recently acquired set points to memory. Allowing the CSAC to periodically store its set points minimizes the possibility of the CSAC subsequently powering on with obsolete set points. Otherwise, upon the next power up, the unit may need to reacquire its set points and time-to-lock may be out of specification.

## 2.3 BUILT-IN TEST EQUIPMENT (BITE)

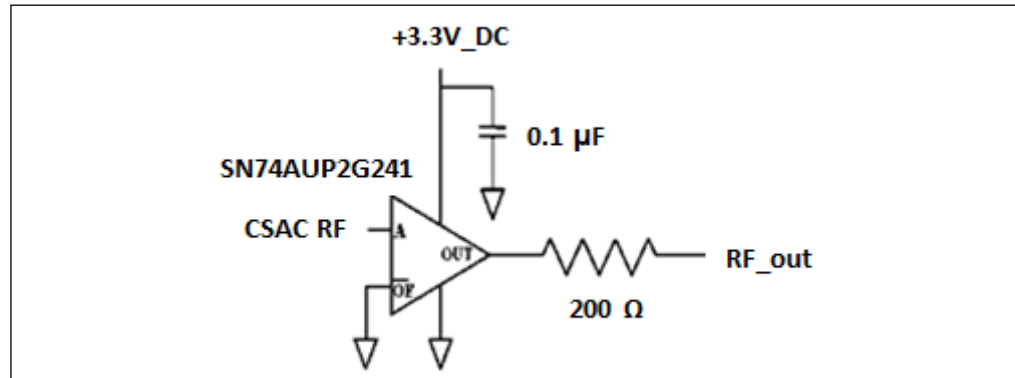
CSAC state-of-health can be monitored electronically on pin 4 (BITE) of the CSAC. Frequency lock is indicated both by status = 0 in the status field of telemetry and by the electrical state of the BITE output pin, which is high (logic 1) upon initial power-on and whenever status  $\neq$  0. The BITE pin is a high impedance CMOS logic output.

**Note:** When not locked, BITE = 1 and also status  $\neq$  0 in the status field of the telemetry output string.

At the conclusion of the acquisition sequence (status = 0), BITE remains high for an additional 5 seconds in order to avoid false indication in the event of acquisition failure. Subsequently, BITE provides an immediate (within 2 seconds) indication of lock failure or alarm.

## 2.4 RF OUTPUT CHARACTERISTICS

The buffered CMOS RF output is provided on pin 12 of the CSAC. The output series impedance is 200Ω. For reference, the output driver circuit of the CSAC is shown in the following illustration.



**FIGURE 2-2:** CSAC RF Output Driver Circuit.

The CSAC is designed for embedded low-power applications. It is expected to drive a high impedance input, not a 50Ω measurement instrument or transmission line.

**Note:** Driving a 50Ω line at 13 dBm consumes nearly as much power as the CSAC itself. If a low impedance output driver is required, a driver circuit must be implemented external to the CSAC, such as the one implemented on the Evaluation Board (see **Section 4.2 “Evaluation Board Overview”**).

The RF output appears on pin 12 after the CSAC is powered ON and is always present, regardless of the lock status. When the CSAC is out of lock (BITE = 1, status ≠ 0), the output frequency is provided by the free-running TCXO. Typically, the unlocked frequency accuracy during acquisition is significantly better than this ( $<1 \times 10^{-8}$ ) as the CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

## 2.5 WHAT TO EXPECT DURING FIRST POWER-UP

The CSAC output frequency is calibrated prior to shipment. However, the shipment conditions may affect the absolute frequency offset when received by the end-user due to temperature excursions, vibration, duration of transit, and so on. As such, some frequency offset should be expected when the CSAC is first powered on by the user. Offsets may be corrected, as explained in **Section 2.6 “Frequency Steering”**.

## 2.6 FREQUENCY STEERING

**Note:** Clockstudio™ software is a graphical interface provided for convenient communication and evaluation of CSAC. To display the functionality of CSAC, screen shots of the Clockstudio GUI are included in the sections that follow. For more information on Clockstudio, see **Section 4.4 “Clockstudio Software Information”**.

For external steering and/or calibration, the CSAC internal microwave synthesizer may be adjusted by the user through the !F command (see **Section 3.3.2 “Frequency Adjustment (F)”**). Steering values are entered in (integer) units of  $1 \times 10^{-15}$ , though the resolution realized by the CSAC hardware is approximately  $1 \times 10^{-12}$ . Steering commands may be entered as either absolute steers (!FA) or as relative steers (!FD).

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In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. In either case, the maximum steer that can be applied to the CSAC is  $\pm 2 \times 10^{-8}$  ( $\pm 2000000000 \times 10^{-15}$ ). If a larger value is sent to the CSAC, the maximum allowed steer is applied.

To overcome the software steering limit of  $\pm 2 \times 10^{-8}$ , the frequency latch command (!FL) may be employed (for more information, see **Section 2.6.1 “Frequency Calibration”**). Ultimately, the CSAC steering capability is physically limited by the TCXO tuning voltage. An alarm will trigger when this voltage is breached.

**Note:** Steering commands can only be entered when the unit is locked (Status=0). Steering commands entered when Status  $\neq$  0 are ignored.

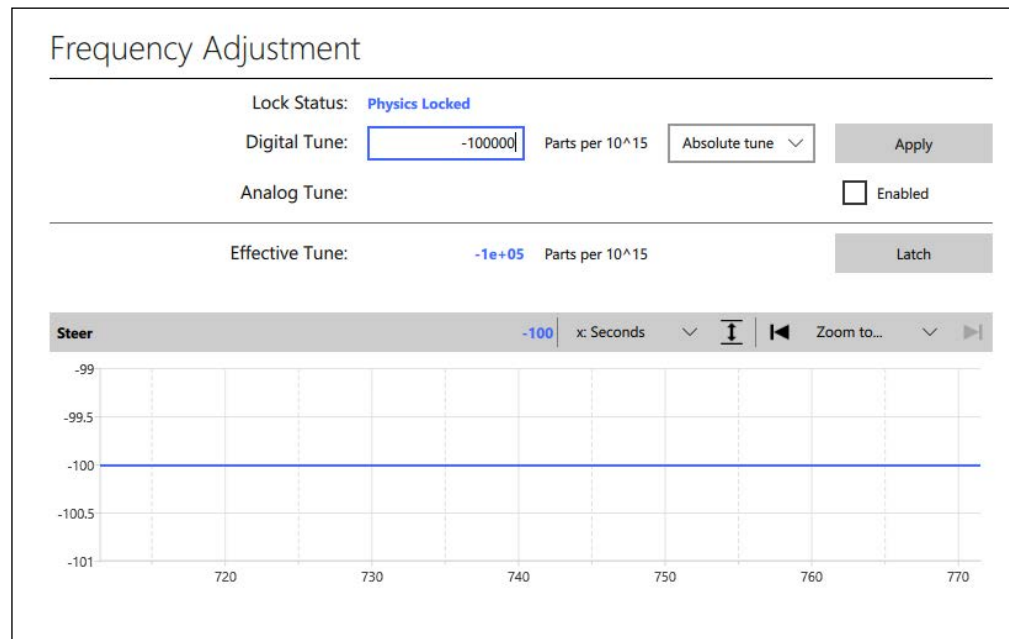
Frequency steering is volatile. Upon reboot, the CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the Frequency Latch command (**Section 3.3.2 “Frequency Adjustment (F)”**).

The current steering value appears in the telemetry string as *Steer*.

**Note:** Steer reports the actual hardware steering, in units of  $\times 10^{-12}$ , even though the software registers maintain resolution of  $\times 10^{-15}$ , so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction in the lowest digit due to roundoff error. An example is provided in **Section 3.3.2 “Frequency Adjustment (F)”**.

To apply a frequency correction from Clockstudio, click on the Frequency Adjustment tab, then select relative or absolute from the pull-down menu and enter the desired steering into the Digital Tune field in  $\times 10^{-15}$ .

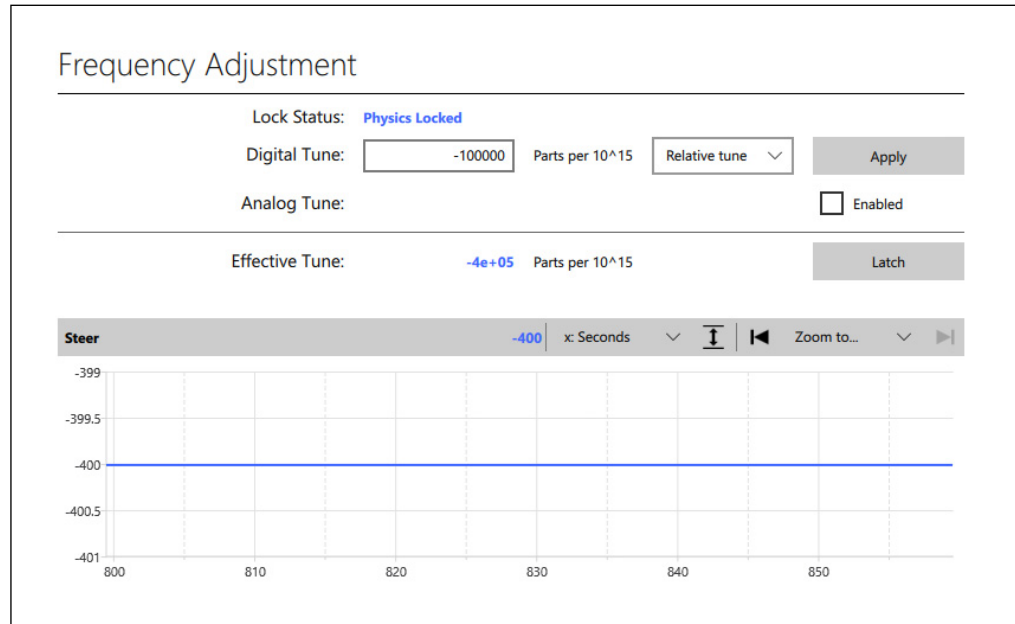
**Figure 2-3** shows an example where an absolute correction of  $-100000 \times 10^{-15}$  is entered. The correction is applied to the CSAC when **Apply** is selected.



**FIGURE 2-3:** Absolute Frequency Adjustment.

As shown in Figure 2-3, after **Apply** is clicked, the correction is applied to the CSAC and the value of `Steer` changes (on the next polling update) to indicate the internal correction of  $-100 \times 10^{-12}$ .

Figure 2-4 shows an example of relative frequency tuning after absolute steer is reset to 0. In this example, each time **Apply** is clicked, an additional correction of  $-100000 \times 10^{-15}$  is applied to the CSAC. In this screen shot, **Apply** has been clicked a total of four times. The resultant value of `Steer` is  $-400 \times 10^{-12}$ .



**FIGURE 2-4:** Relative Frequency Adjustment.

## 2.6.1 Frequency Calibration

The internal frequency calibration of the CSAC is set prior to shipment. The calibration may need to be updated from time to time to remove cumulative frequency aging offsets.

Calibration of the CSAC is a two-step process. First, the CSAC is steered onto frequency, either through an external `!F` command (see Section 2.6 “Frequency Steering”), through 1 PPS disciplining (see Section 2.10 “1 PPS Disciplining”), or with analog tuning (see Section 2.13 “Analog Tuning”). Second, the present value of `Steer` is summed into the non-volatile calibration register through the Frequency Latch command (see Section 3.3.2 “Frequency Adjustment (F)”). Following a Latch command, the value of `Steer` resets to zero.

**Note:** The Latch command is only valid when the CSAC is locked (Status = 0).

To latch the current steer value to non-volatile storage from Clockstudio, click **LATCH**.

**Note:** It may be tempting, particularly in disciplining applications, to frequently latch the steering value into calibration in the event of unforeseen power outage. This is highly discouraged because the lifetime of the CSAC's non-volatile memory is finite; updating it too frequently will damage the memory blocks and render the CSAC inoperable.

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## 2.7 1 PPS OUTPUT

A CMOS level 1 pulse-per-second (1 PPS) output is available on pin 10 upon power-up (PPSOUT). The output series impedance is 200Ω. The output driver circuit is similar to that of the RF output (see [Figure 2-2](#)). Nominal levels are 0VDC to 3.3VDC. For synchronization purposes, the on-time point is the rising edge of pin 10.

PPSOUT is derived by digital division of the RF reference frequency. The frequency stability and accuracy of PPSOUT reflects that of the RF output. When unlocked (BITE = 1, status ≠ 0), PPSOUT stability reflects that of the free-running TCXO.

Control of PPSOUT signal, synchronization, and disciplining is provided on the 1 PPS Disciplining tab in Clockstudio. The 1 PPS Disciplining tab is shown in [Figure 2-5](#).

1 Pulse-per-Second Output

Auto Sync:  Enabled Sync Now

Pulse Width:  ns

Disciplining:

Time Constant:  seconds

Discipline Threshold:  ns

Cable Delay:  ns

Discard Apply

**FIGURE 2-5:** 1 PPS Disciplining Tab.

The output pulse width (PPSWidth) of PPSOUT can be set to a value between 10 μs and 500,000 μs in increments of 10 μs by adjusting PPSWidth (more information in [Section 3.3.11 “Set PPSwidth \(>\).”](#)). To adjust PPSWidth from Clockstudio, enter the new value (in nanoseconds) into the Pulse Width field and click **Apply**.

**Note:** The increments of PPSWidth are under the assumption of a 10 MHz CSAC. For a CSAC with a different output frequency, consult the datasheet for the available increments of PPSWidth.

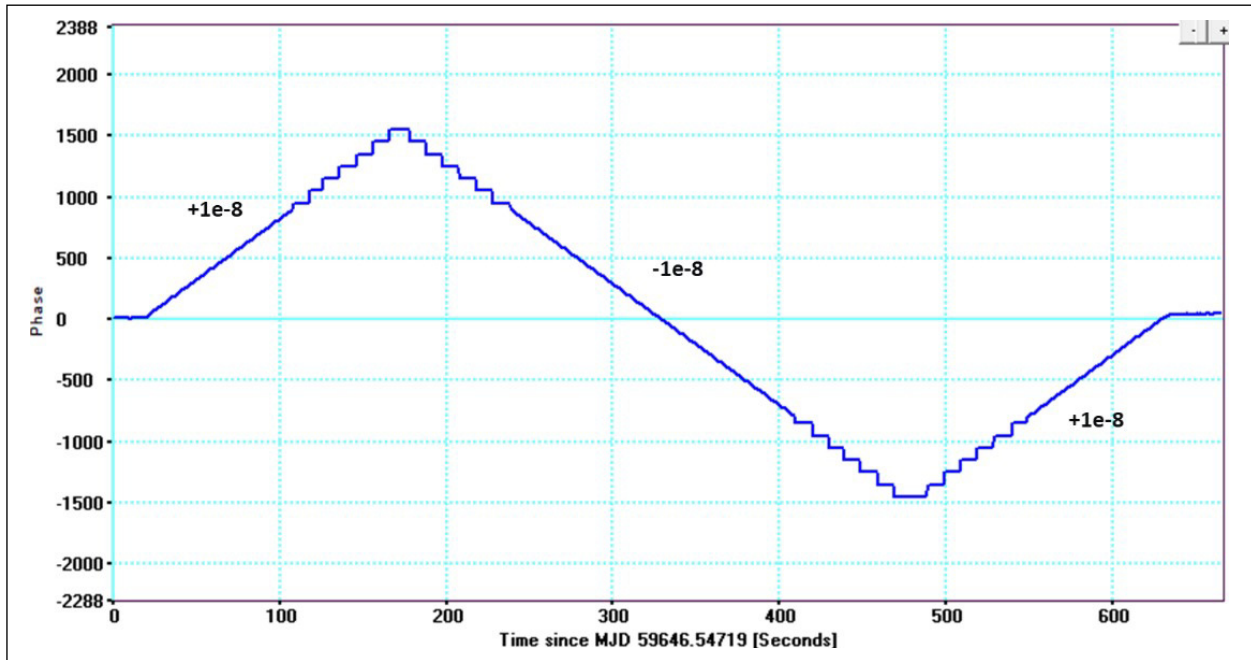
## 2.8 TIME-INTERVAL COUNTER

The CSAC accepts a user-supplied 1 PPS input reference signal as an input on pin 9 (PPSEXT). The CSAC time-interval counter (TIC) measures the time interval (TI) between the rising edges of PPSOUT and PPSEXT. The TIC measurement is reported in the telemetry field “**Phase**” (see [Section 3.3.1 “Telemetry \(6 and ^\)”](#)), where the sign convention is (Phase = PPSEXT – PPSOUT), i.e. a negative value of **Phase** indicates that PPSOUT occurs after PPSEXT by **Phase** ns.

For values of **Phase** outside the range of ±800 ns the TIC reports **Phase** with resolution of 100 ns (10 MHz CSAC). For values of **Phase** within ±800 ns, the TIC reports **Phase** with resolution of 1 ns.

The TIC operates whenever a rising edge appears on PPSEXT. If no PPSEXT is detected for more than 2 seconds, the TIC reports “---” in the telemetry **Phase** field.

Upon initial startup, prior to any synchronization between PPSOUT and PPSEXT, the TIC will report the (unsynchronized) **Phase** on the range of ±0.5 seconds (±500000000 ns).



**FIGURE 2-6:** Time-Interval Counter Performance.

Figure 2-6 illustrates the transition of the TIC output (**Phase** telemetry parameter) from fine to coarse measurement as PPSOUT is swept through **Phase** = 0. For this data, PPSOUT was synchronized to PPSEXT prior to time=0. Frequency **Steers** of  $\pm 1e-8$  were applied to the CSAC at times 25 sec., 175 sec., and 475 sec.

## 2.9 1 PPS SYNCHRONIZATION

The rising edge of the 1 PPS output is synchronous with one rising edge of the RF output (pin 12). The 1 PPS output may be synchronized with a particular cycle of the RF by applying a synchronization pulse to PPSEXT (pin 9). When synchronized, the counters are reset such that the 1 PPS output occurs on the RF rising edge, which is immediately subsequent to the externally applied rising edge. In this way, the CSAC 1 PPS can be synchronized to within one clock cycle ( $-100$  ns to  $+100$  ns) of the external reference.

During the synchronization process, the length of the second immediately following the next rising edge of PPSEXT is adjusted to accomplish synchronization. In the case where PPSEXT appears ahead of PPSOUT by  $<0.5$  seconds, the subsequent epoch may be extended by up to 0.5 seconds. In the case where PPSEXT appears following PPSOUT by  $<0.5$  seconds, the subsequent epoch is shortened by up to 0.5 seconds.

The CSAC provides two modes for 1 PPS synchronization, Manual and Automatic, which are selected through a bit in the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**).

**Note:** The configuration of the mode register is non-volatile (preserved across power cycles).

## 2.9.1 Manual Synchronization

In Manual Synchronization mode (default), the CSAC ignores any signal present on the PPSEXT (pin 9) until commanded. When a synchronization command is received (see **Section 3.3.4 “1 PPS Synchronization (S)”**), the PPSOUT is synchronized to the next rising edge of PPSEXT to appear on pin 9.

This mode is applicable to configurations where the CSAC is embedded in a system where a 1 PPS reference signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the CSAC to synchronize after it has verified the state-of-health of the 1 PPS reference source (for example, after querying lock state of a GPS receiver).

To manually synchronize the CSAC from Clockstudio, make sure that a valid 1 PPS reference is connected to the 1 PPS reference input and click **Sync Now** on the 1 PPS panel (**Figure 2-5**). The CSAC synchronizes to the next rising edge of PPSEXT detected on pin 9.

## 2.9.2 Automatic Synchronization

In Automatic Synchronization mode, the CSAC synchronizes PPSOUT to every PPSEXT rising edge that appears on pin 9. In this mode, synchronization may be performed by connecting a reference 1 PPS signal to pin 9 without needing to issue the synchronization command. Automatic synchronization can be enabled/disabled through bit 3 (0x0008) in the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**).

This mode can be useful, for example, in cases where the host system does not communicate with the CSAC and uses gating of the PPS to indicate validity.

**Note:** Automatic Synchronization mode and Disciplining mode (see **Section 2.10 “1 PPS Disciplining”**) are mutually exclusive. Enabling either in the mode register disables the other.

To enable Automatic Synchronization from Clockstudio, select the **Enable Autosync** checkbox on the 1 PPS panel and click **Apply Changes** (see **Figure 2-5**).

## 2.10 1 PPS DISCIPLINING

In order to achieve higher-resolution synchronization of PPSOUT as well as frequency calibration of the CSAC, the CSAC incorporates a simple proportional-integral (PI) disciplining algorithm.

Based on the measurements of the TIC, the disciplining algorithms adjust the CSAC's microwave synthesizer through the digital tuning value (*steer*, observed from the telemetry string). The algorithm steers the frequency so as to simultaneously discipline both the time- and frequency-error of the CSAC to that of the external reference, ultimately achieving accuracies of <5 ns and  $1 \times 10^{-12}$ , respectively. Note that, unlike the !FA and !FD commands, there is no software limitation upon the disciplined value of *steer*.

Disciplining can be enabled/disabled through bit 4 (0x0010) in the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**). The time constant of the steering algorithm is user selectable through the !D command (see **Section 3.3.5 “Set 1 PPS Disciplining Time Constant (D)”**).

**Note:** Both mode setting and time constant are non-volatile, that is, preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1 PPS synchronization operation (see **Section 3.3.4 “1 PPS Synchronization (S)”**) is executed to bring the 1 PPS output within 100 ns of the reference. Initialization is performed when Disciplining is first enabled in the mode register and, in the case where Disciplining is already enabled after the CSAC achieves frequency lock (BITE = 0, status = 0).

Automatic synchronization, at  $\pm 100$  ns, is enabled along with Disciplining, in order to maintain  $\text{PPSOUT} - \text{PPSEXT} < \pm 100$  ns. This may happen, for example, during the early stages of disciplining, particularly if the initial frequency or phase of PPSOUT is far from that of PPSEXT.

In the event that the 1 PPS reference is removed from pin 9 while Disciplining, the CSAC remains in holdover and preserves the most recent steering value. If the 1 PPS reference subsequently reappears, Disciplining continues where it left off, without reinitializing.

If it is necessary to force re-initialization of the disciplining variables, perhaps because the reference source is deemed untrustworthy and subsequently recovers, this can be accomplished by disabling and re-enabling Disciplining in the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**).

In the Clockstudio software, enabling/disabling Disciplining and setting the discipline time constant are both accomplished on the 1 PPS panel, accessible from the View menu (See [Figure 2-5](#)). To modify the discipline time constant, enter the new value in the field (10 to 10000 in seconds) and click **Apply Changes**.

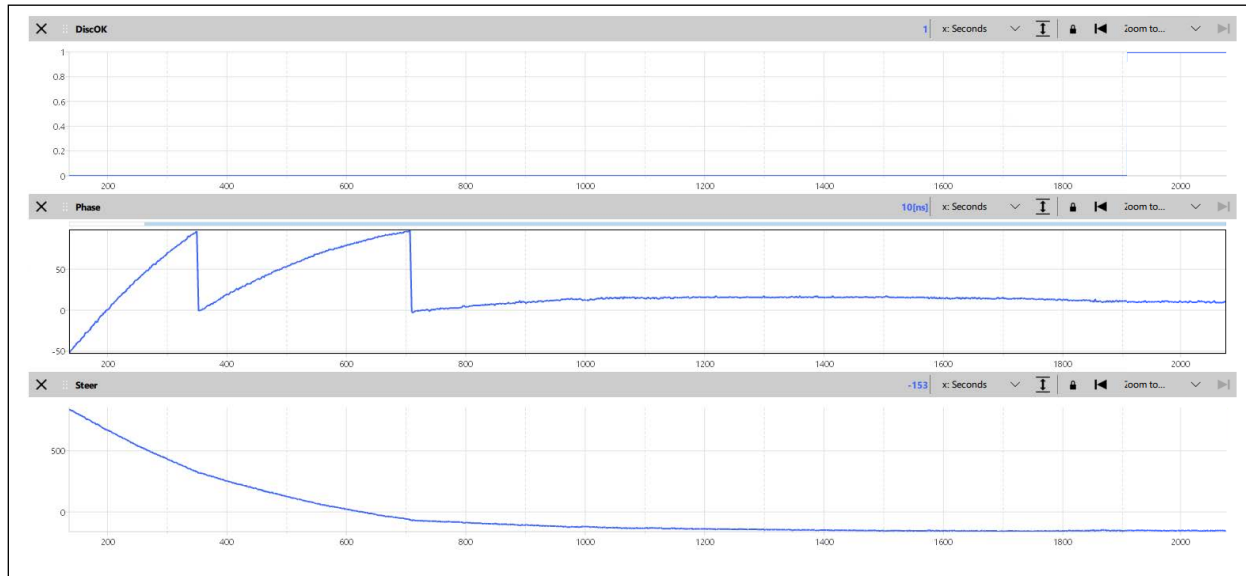
The status of Disciplining is indicated by the `DiscOK` parameter in the telemetry. `DiscOK = 0` upon startup. `DiscOK = 1` when magnitude of TIC measurement is less than a user-specified threshold (see **Section 3.3.10 “Set Threshold for DiscOK Indicator (m)”**) for two time constants of duration. `DiscOK = 2` when in holdover (disciplining enabled but no 1 PPS present).

**Note:** Automatic Synchronization mode (see **Section 2.9.2 “Automatic Synchronization”**) and Disciplining mode are mutually exclusive. Enabling either in the mode register disables the other.

The `DiscOK` indicator and `DiscOKthreshold` have no impact on the behavior or performance of the CSAC. `DiscOK` is a simple status indicator. In practice, `DiscOK` is frequently employed for detection of initial acquisition to an external reference. It is less useful for long-term monitoring, where intermediate excursions may exceed the long-term stability objective.

In the Clockstudio software, the current status of `DiscOK` and the `DiscOKthreshold` setting both appear on the 1 PPS panel, accessible from the View menu (See [Figure 2-5](#)). To modify `DiscOKthreshold`, enter the new value (10 to 10000 in nanoseconds) in the field and click **Apply**.

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**FIGURE 2-7:** PPS Disciplining.

Figure 2-7 shows an example of Disciplining with  $\text{DisciplineTau} = 600$  as well as  $\text{DiscOKthreshold} = 20$ . As Discipline steered both phase and frequency to 0 with a 600 sec. time constant, Discipline periodically re-synced PPSOUT to PPSEXT in order to maintain Phase within  $\pm 100$  ns. DiscOK transitioned from 0 to 1 when Phase  $< 20$  ns for two 600-second time constants.

## 2.10.1 Cable Length Compensation

The zero point of disciplining can be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the PPSEXT at the CSAC 1 PPS input pin. The compensation value can optionally be stored in the CSAC non-volatile RAM for persistent calibration.

The maximum compensation adjustment is  $\pm 25$  ns, with resolution of 100 ps. The compensation value is entered into the CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1 PPS. For example, if there is 10 ns of delay (approximately 2 meters of RG-58 coaxial cable) between the on-time point and the CSAC 1 PPS input then the compensation value would be +100.

**Note:** Compensation is implemented in the disciplining algorithm, not in the TIC itself. The phase measurement, as reported through telemetry, reports the actual phase measurement, that is, if the CSAC is disciplined with +10 ns of compensation, the phase meter reports  $-10$  ns of phase error.

Compensation is set with the `!DC` command (see [Section 3.3.6 “Set Volatile 1 PPS Disciplining Time Constant \(d\)”](#)).

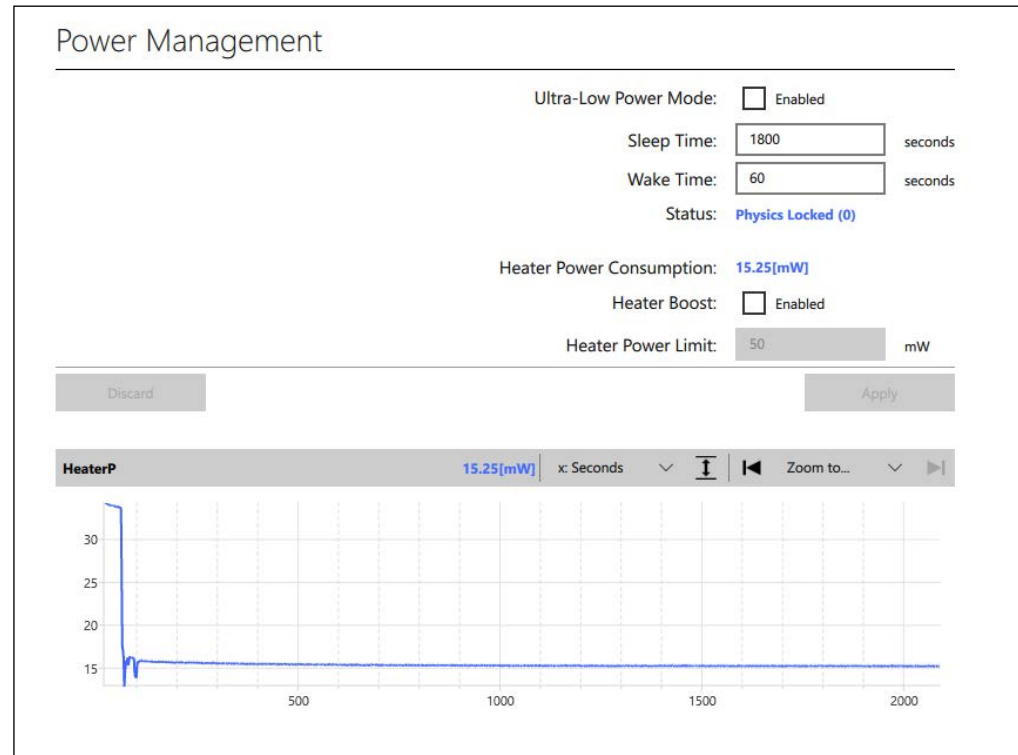
## 2.11 POWER CONTROL

CSAC time-to-lock (TTL) from cold start is limited by the need to initially warm-up the central core of the physics package which, in turn, is limited by the power supply capacity. TTL may be reduced at the expense of additional CSAC power draw during warm-up, based on the user-specified **HeaterBoostLimit**.

**HeaterBoostLimit** is a non-volatile parameter that specifies the maximum power provided by the heater control circuit. The units of **HeaterBoostLimit** are milliwatts, the limits are 50 mW to 250 mW, and the default value is 50 mW. (see **Section 3.3.12 “Set HeaterBoostLimit (.)”**).

With **HeaterBoostLimit** set to the default value of 50 mW, CSAC will meet the warm-up power specification on the data sheet. Increasing the value of **HeaterBoostLimit** will improve lock time at the expense of warm-up power, beyond the data sheet specification.

To configure **HeaterBoostLimit** using Clockstudio, open the Power Management Tab as shown in **Figure 2-8**. Check the **Enabled** box, enter the maximum power, and click **Apply**.



**FIGURE 2-8:** Clockstudio Power Management Tab.

## 2.12 TIME-OF-DAY

The CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer, which is incremented synchronously with the rising edge of the 1 PPS output. Until set otherwise, TOD begins counting from zero when the CSAC is powered on.

TOD is retrieved from the CSAC with the `!T?` command (see **Section 3.3.9 “Time-of-Day (TOD)”**). When the `!T?` command is received, the CSAC waits for the next rising edge of 1 PPS before replying with the TOD of the current epoch, that is, if the command is received during epoch N, then the reply N+1 appears immediately following the next PPSOUT. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD can be set with the `!T` command. The `!T` command includes provision both for setting an absolute number or for a differential ( $\pm$ ) adjustment of the present TOD. An example is provided in **Section 3.3.9 “Time-of-Day (TOD)”**. To avoid ambiguity in setting the TOD, it is recommended that the host system wait for PPSOUT prior to transmitting the setting/adjustment immediately thereafter.

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The Clockstudio software shows TOD on the Time of Day tab, as shown in [Figure 2-9](#).

**FIGURE 2-9:** Clockstudio Time of Day Tab.

The raw CSAC TOD value is shown in the lower field of the panel (here 2281). The upper display of the TOD panel realizes the timekeeping convention of the C programming language (in UNIX and Microsoft Windows), which counts time in seconds from midnight on January 1, 1970. Upon clicking **Send**, it sets the CSAC time according to the host PC's TOD counter (either local time or UTC depending on the setting of the pull-down menu above the Apply button). The + and - buttons for hours and seconds adjustment will increment or decrement the CSAC TOD by  $\pm 3600$  or  $\pm 1$  second respectively.

## 2.13 ANALOG TUNING

To enable analog frequency tuning for implementation in legacy (quartz crystal) applications, the frequency of the CSAC can be tuned with an external voltage applied to pin 1. This functionality can be enabled/disabled through a bit in the mode register (see [Section 3.3.3 “Set/Clear Operating Modes \(M\)”](#)). The applied voltage is digitized by an internal analog-to-digital converter and the correction is applied to the microwave synthesizer at a rate of once per second, that is, the maximum tuning rate is 1 Hz.

When analog tuning is enabled, the voltage applied at pin 1 and the resultant steering are reported in the standard telemetry stream (see [Section 3.3.1 “Telemetry \(6 and ^\)”](#)). The tuning voltage input range is 0VDC to 2.5VDC, which corresponds to a full scale tuning range of  $4.4 \times 10^{-8}$ . Nominal zero-correction tuning occurs at a tuning input voltage of 1250 mV. The fractional frequency correction, for a given applied voltage, is given by Equation 2-1.

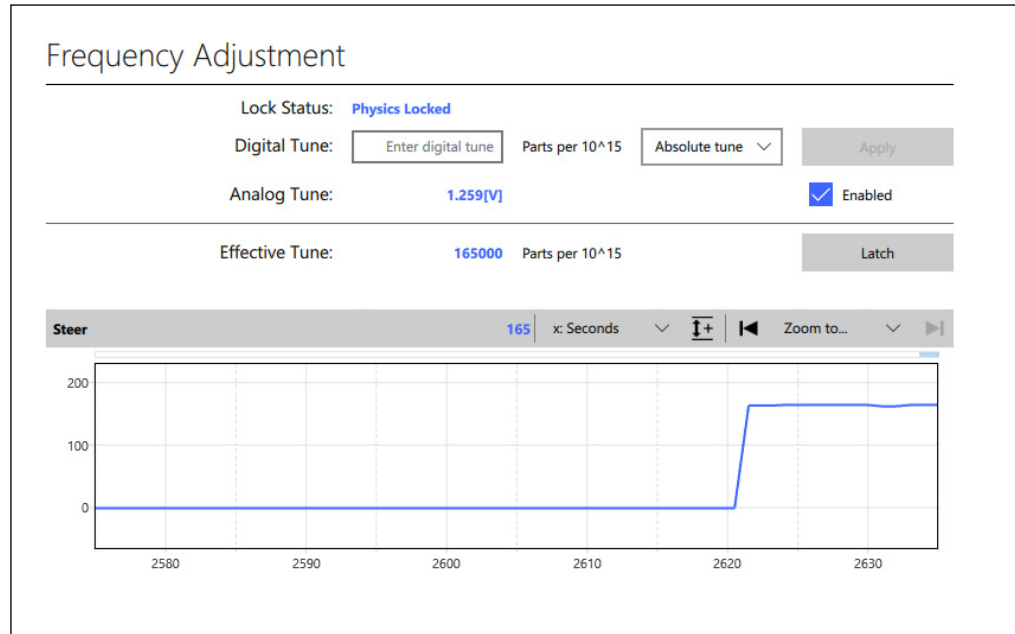
### EQUATION 2-1:

$$\Delta f/f = (V_{\text{TUNE}} - 1250\text{mV}) \times 1.77 \times 10^{-11} / (\text{mV})$$

**Note:** This formula is accurate for a CSAC operating at 10.0 MHz output frequency. Consult the data sheet for tuning curves of CSACs at alternate frequencies. The tuning input pin is nominally biased at  $\approx 1250$  mV, that is, approximately zero correction.

**Note:** Bias voltage may vary due to component variations and/or exhibit temperature sensitivity. Therefore, analog tuning should not be enabled unless the functionality is necessary and the analog tuning input pin is connected to a low noise, low impedance voltage source. For non-legacy applications, it is recommended that this feature remain disabled, and that corrections be applied through the digital communications interface (see **Section 2.6 “Frequency Steering”**) to avoid degradation of the CSAC short-term stability due to voltage noise applied to the tuning pin.

Analog tuning can be enabled/disabled and monitored from the Frequency Adjustment tab in the Clockstudio software, as shown in [Figure 2-10](#).



**FIGURE 2-10:** Analog Tuning Settings on Frequency Adjustment Tab.

When analog tuning is enabled, the voltage present on pin 1 is displayed in the Analog Tuning field and also reflected in the current reported value of steer on the main panel. To enable or disable analog tuning, select the **Enable Analog Tuning** checkbox and click **Apply Changes**.

## 2.14 ULTRA-LOW POWER OPERATING MODE

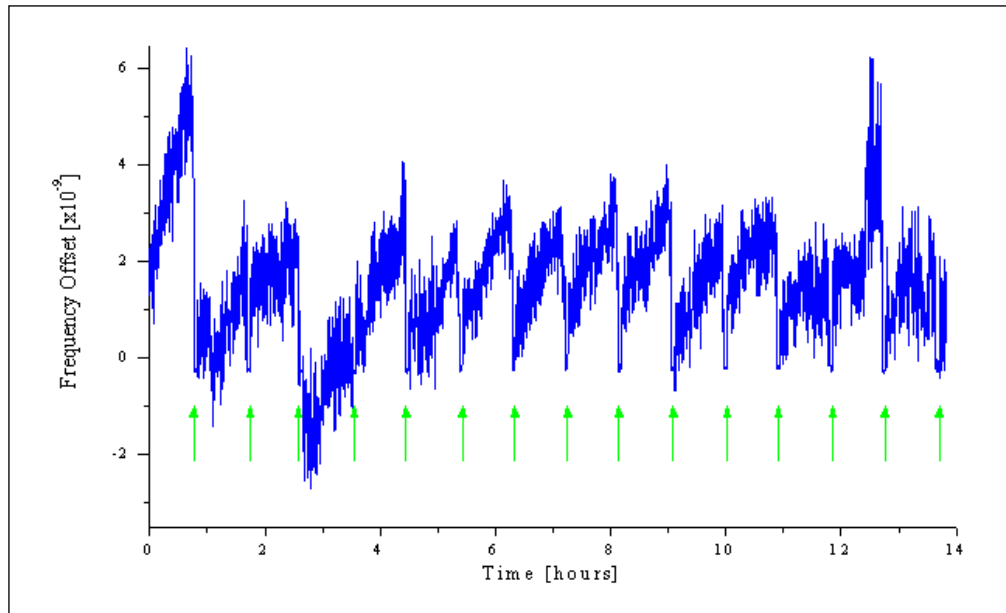
The majority of the power in the CSAC is consumed by the physics package and microwave synthesizer. In ultra-low power (ULP) mode, the physics package and synthesizer can be disabled for a user-specified length of time, during which the CSAC operates as a free-running TCXO. Periodically, the atomic clock portion of the CSAC is powered on (again for a user-specified amount of time) and the TCXO is re-calibrated to the atomic frequency. Operating in this mode, the CSAC exhibits the short-term performance of a TCXO and the long-term performance of the atomic clock at significantly lower power compared to standard mode. For example, if the atomic clock portion is only powered on for 5 minutes out of every hour (2 minutes for lock acquisition + 3 minutes of run time), then the time-averaged power of the CSAC may be <30 mW.

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Between calibration cycles, the CSAC in ULP mode exhibits the performance characteristics of a free-running TCXO and therefore exhibits significantly higher short-term frequency drift and environmental (temperature and vibration) sensitivity than a normally operating CSAC. ULP mode is principally recommended only for applications that require long-term, rather than short-term, frequency or time stability.

**Note:** Due to the unique behavior and configurability of ULP, the data sheet performance specifications for the CSAC cannot be guaranteed while in ULP mode. Contact Microchip for additional assistance in evaluating and optimizing ULP for your specific application.

The following illustration shows an example of a CSAC operating in ULP mode, with wake-time = 300 seconds (5 min.) and sleep-time = 3300 seconds (55 min.).



**FIGURE 2-11:** Frequency Record of CSAC in ULP Mode.

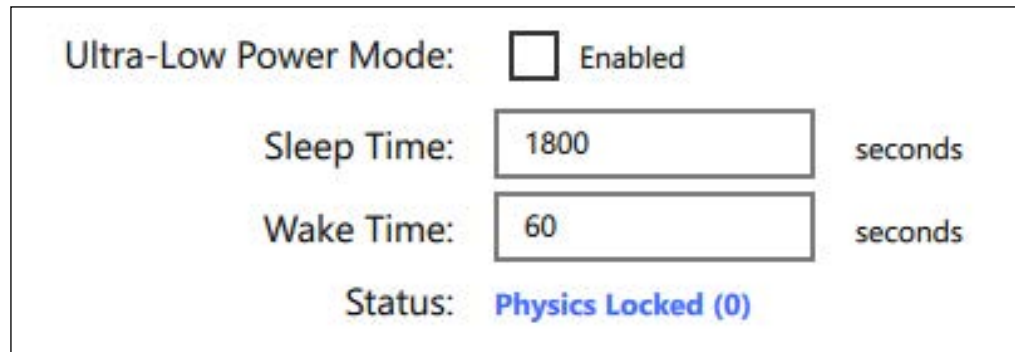
The green arrows indicate the full-power calibrations. Note the relatively poor TCXO drift and temperature behavior between calibrations.

ULP is an unusual operating mode for an atomic clock and it is important for the user to understand how the clock is behaving to effectively implement this feature in a system. In particular, note the following:

- When operating in ULP mode, the Status register indicates Status = 9 (asleep) when the atomic clock portion of the CSAC is asleep. Each wake cycle is indicated by the usual lock process (Status = 8, 7, 6,...) followed by wake-time seconds of operation at Status = 0 before the cycle repeats. This cycle is also reflected on the BITE pin, which is 1 (high) whenever the CSAC is unlocked (or asleep) and only 0 (low) during the locked periods.
- When using Disciplining (see **Section 2.10 “1 PPS Disciplining”**) in conjunction with ULP, disciplining functionality is disabled during sleep and unlocked cycles, though steering information is preserved and updated across wake cycles.
- Frequency Steering commands may only be entered when the CSAC is locked (Status = 0) (see **Section 2.6 “Frequency Steering”**).
- If enabled, Analog Tuning (see **Section 2.13 “Analog Tuning”**) is only active when the CSAC is awake and the CSAC is locked (Status = 0).

ULP is enabled through bit 5 (0x0020) in the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**). Sleep-time and wake-time intervals are set by the !U command (see **Section 3.3.8 “Set Ultra-Low Power Mode Parameters (U)”**). These values are non-volatile; they persist across power cycles. Note that the wake-time begins counting after the CSAC achieves lock, so the actual time that the atomic clock portion of the CSAC is powered on is the sum of the time to lock and the user-configured wake-time. The minimum allowed values of wake-time and sleep-time are 10 seconds and 1800 seconds, respectively.

To configure ULP parameters using Clockstudio, select the **Power Management** tab to access the settings shown in [Figure 2-12](#).



Ultra-Low Power Mode:  Enabled

Sleep Time:  seconds

Wake Time:  seconds

Status: **Physics Locked (0)**

**FIGURE 2-12:** Ultra-Low Power Mode Settings on the Power Management Tab.

Enter the desired settings and click **Apply Changes** to upload new settings to the CSAC.

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NOTES:

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## Chapter 3. Programmer's Reference

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Pins 5 and 6 provide a serial interface for communication with the CSAC. The protocol is fundamentally similar to RS-232, with the exception that the voltage levels are CMOS (0V to  $V_{CC}$ ), rather than  $\pm 12V$ .

The serial communication parameters are as follows: (57600-8-N-1)

- 57,600 Baud
- 8 data bits
- No parity
- 1 stop bit
- No flow control

For interfacing with a standard RS-232 controller interface, which requires  $\pm 12V$  logic levels, an external level shifter must be employed, such as the Maxim MAX202.

The evaluation board, which supports a USB interface, utilizes a MCP2200 USB to UART converter. Access to the TX and RX pins are made via Test Points 11 and 12 (see **Section 4.2 “Evaluation Board Overview”**).

### 3.1 OVERVIEW OF TELEMETRY INTERFACE

The CSAC communicates exclusively with printable (non-binary) ASCII characters.

In general, commands are to be preceded by an exclamation point (!) and followed by a carriage-return /linefeed [`CRLF`] pair (ASCII 0x0D 0x0A). For convenience and efficiency, most commands also provide a single-character shortcut, which is executed immediately, that is without bracketing by ! and [`CRLF`]. For example, the single character shortcut ^ is functionally identical to !^[`CRLF`].

After transmitting ! but prior to sending [`CRLF`], a command may be aborted by sending the escape character (ASCII 0x1B).

All commands produce a response from the CSAC, which are human readable, with individual lines ending in [`CRLF`]. If an unsupported or improperly formatted command is received, the CSAC responds with ? [`CRLF`].

#### 3.1.1 Checksum (Error-Checking Option for Telemetry Interface Communications)

For improved communications reliability, an NMEA-style checksum may be enabled through bit 6 (0x0040) of the mode register (see **Section 3.3.3 “Set/Clear Operating Modes (M)”**). When enabled, the checksum is required for all input commands and is present on all replies from the CSAC.

The checksum is a two-byte ASCII representation (in hexadecimal) of the XOR of all characters in the command between—but not including—the ! and the [`CRLF`] characters. The checksum is preceded by a \* character and appended to the command immediately prior to the [`CRLF`]. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (enable analog tuning through mode register):

Command: !MA\*0C [`CRLF`]

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Unit response: 0x0041\*4D [CRLF]

Example (disable checksum through mode register)

Command: !Mc\*2E [CRLF]

Unit response: 0x0000 [CRLF]

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the CSAC responds with \* [CRLF].

Example (malformed checksum):

Command: !Mc\*2D [CRLF]

Unit response: \* [CRLF]

**Note:** Communicating with the CSAC via Clockstudio™ does not require a checksum. Any commands sent to the CSAC via the Clockstudio console will have a checksum generated automatically. However, if a checksum is provided, the CSAC will respond appropriately.

## 3.1.2 How to Calculate the Checksum

The checksum value is a two digit hexadecimal representation of the logical XOR of each character in the command (excluding “!” and “[CRLF]”). Table 3-1 illustrates computation of the checksum for sending the !MD [CRLF] command. In Table 3-1, M and D are converted to their binary equivalents and the XOR is computed in the bottom row. The corresponding hexadecimal value of that XOR is “9”. Hence, the command should be sent as !MD\*09 [CRLF].

**TABLE 3-1: CHECKSUM CALCULATION EXAMPLE**

Checksum Component	ASCII Character	Binary Value	Hex Value
Input Command Characters	M	0100 1101	—
	D	0010 0100	—
Logical XOR	—	0000 1001	9

## 3.2 COMMAND SUMMARY

Table 3-2 summarizes the CSAC commands.

**TABLE 3-2: COMMAND SUMMARY**

Shortcut	Description	Command	Reference Section
6	Return telemetry headers as comma-delimited string.	!6 [CRLF]	Section 3.3.1 “Telemetry (6 and ^)”
^	Return telemetry as comma-delimited string.	!^ [CRLF]	Section 3.3.1 “Telemetry (6 and ^)”
F	Set/report frequency adjustment.	!F? [CRLF]	Section 3.3.2 “Frequency Adjustment (F)”
M	Set/report operating mode register bits.	!M? [CRLF]	Section 3.3.3 “Set/Clear Operating Modes (M)”
S	Sync CSAC 1 PPS to external 1 PPS.	!S [CRLF]	Section 3.3.4 “1 PPS Synchronization (S)”
D	Set/report 1 PPS disciplining time constant.	!D? [CRLF]	Section 3.3.5 “Set 1 PPS Disciplining Time Constant (D)”
U	Set/report ultra-low power mode parameters.	!U? [CRLF]	Section 3.3.8 “Set Ultra-Low Power Mode Parameters (U)”
T	Set/report time-of-day.	!T? [CRLF]	Section 3.3.9 “Time-of-Day (TOD)”
m	Set/report DiscOKthreshold.	!m? [CRLF]	Section 3.3.10 “Set Threshold for DiscOK Indicator (m)”
>	Set/report PPSwidth.	!>? [CRLF]	Section 3.3.11 “Set PPSwidth (>).”
.	Set/report HeaterBoostLimit	!.? [CRLF]	Section 3.3.12 “Set Heater-BoostLimit (.)”
p	Report Part Number	!p? [CRLF]	Section 3.3.13 “Report Part Number (p)”
?	Help.	!? [CRLF]	Section 3.3.14 “Help (?)”

## 3.3 DETAILED COMMAND DESCRIPTIONS

The following are descriptions of the CSAC's commands.

### 3.3.1 Telemetry (6 and ^)

CSAC supports two commands, !6 and !^, to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Example:

Telemetry headers command: !6 [CRLF]

Unit response: Status, Alarm, SN, Mode, Contrast,  
LaserI, TCXO, HeatP, Sig, Temp, Steer, ATune, Phase, DiscOK,  
TOD, LTime, Ver [CRLF]

Example:

Telemetry data command: !^ [CRLF]

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Unit response:

0, 0x0000, 2202CS77501, 0x0000, 19215, 0.97, 1.544, 12.81, 1.992, 26.90, 0, 0, ---, ---, 153, 59, 2.4

Not including the 3-character checksum, if enabled, the maximum length of a telemetry string is 129 characters. See [Table 3-3](#) for details.

**Note:** The single-characters 6 and ^ are shortcuts for !6 [CRLF] and !^ [CRLF], respectively.

[Table 3-3](#) lists the telemetry parameters and their associated header identifiers.

**TABLE 3-3: TELEMETRY PARAMETERS**

Identifier	Description	Notes	String Length
Status	Unit status	See Note 1 and <a href="#">Table 3-4</a>	Up to 2 decimal digits (2 characters)
Alarm	Pending unit alarms	See Note 2 and <a href="#">Table 3-5</a>	"0x" + 4 hexadecimal digits (6 characters max)
SN	Unit serial number	See Note 3	11 characters
Mode	Mode of operation	See <a href="#">Table 3-6</a>	"0x" + 4 hexadecimal digits (6 characters max)
Contrast	Indication of signal level	Typically >1000 when locked, and ≈ 0 when unlocked	16 bits unsigned (5 characters max)
LaserI	Laser current (mA)	Typically 0.6 mA to 1.3 mA	16 bits unsigned + "." + 2 digits precision (8 characters max)
TCXO	Tuning voltage (V)	0VDC to 2.5VDC tuning range ≈ ±10 × 10 <sup>6</sup>	16 bits unsigned + "." + 3 digits precision. Maximum value is 400.03 (6 characters max)
HeatP	Physics package heater power (mW)	Typical 6 mW to 20 mW under normal operating conditions and 25°C ambient	16 bits unsigned + "." + 2 digits precision. Maximum value is 250.0 (6 characters max)
Sig	DC signal level (V)	Typical 0.8V to 1.7V under normal operating conditions	16 bits unsigned + "." + 3 digits precision. Maximum value is 2.490 (5 characters max)
Temp	Unit temperature (°C)	Absolute accuracy is ±2°C	16 bits unsigned + "." + 2 digits precision. Range is -54.19 to 159.65 (6 characters max)
Steer	Frequency adjust	In pp10 <sup>12</sup>	32 bits signed (11 characters max)
ATune	Analog tuning voltage input	--- when analog tuning is disabled, 0V to 2.5V when enabled	16 bits unsigned + "." + 3 digits precision. Maximum value is 2.500 (5 characters max)
Phase	Difference between PPSOUT and PPSIN (ns)	Reports "---" if no PPSIN detected for >2 seconds.	32 bits signed. Range is ±500000000 nano-seconds (10 characters max)
DiscOK	Discipline status (0-2)	0 = acquiring, 1 = locked, 2 = holdover when disciplining enabled, otherwise ---	"0", "1", "2" or "---" (3 characters max)
TOD	Time (seconds)	Starts at 0 upon power-up unless set by command	32 bits unsigned (10 characters max)
LTime	Time since lock (seconds)	Starts at 0 upon lock	31 bits unsigned (10 characters max)
FWver	Firmware version	M.m where M is major revision and m is minor revision	"2.0" (4 characters, may be longer in future firmware)

- Note 1:** Status reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When Status ≠ 0, BITE = 1. When Status = 0, BITE = 0.
- 2:** Alarms indicate detection of anomalous operating conditions while locked. Alarm is the logical OR of all pending alarms, as shown in the following table. An alarm will not persist if the condition is fixed or if the unit is reset.
- 3:** CSAC serial numbers are of the form YYMMCSXXXXX where YYMM is the year and month of production and XXXXX is the serialized production unit number.

**TABLE 3-4: STATUS CODES OF CSAC**

Status	Acquisition Stage
9	Asleep (ULP mode only).
8	Initial warm-up.
7	Heater equilibration.
6	Microwave power acquisition.
5	Laser current acquisition.
4	Laser power acquisition.
3	Microwave frequency acquisition.
2	Microwave frequency stabilization.
1	Microwave frequency steering.
0	Locked.

**Note:** If CSAC returns a status code other than shown in [Table 3-4](#), then it is re-acquiring its set points. In this case, warm-up time takes longer than stated on the CSAC SA65 data sheet. To avoid this, it is recommended to always allow CSAC to remain powered on for >102 seconds after it acquires LOCK. 102 seconds is the minimum amount of time necessary to save CSAC set points to memory, thus avoiding set-point re-acquisition upon its next power up.

**TABLE 3-5: ALARM CODES**

Alarm	Definition	Alarm Limit
0x0001	Signal contrast low.	Contrast <1000
0x0002	Synthesizer tuning at limit.	Synthesizer detuned from calibration by >30 kHz or <-15 kHz
0x0004	Temperature bridge unbalanced.	Bridge—set-point >±20 mV
0x0008	Heater Boosted ( <a href="#">Note 2</a> )	Heater boost is actively boosting
0x0010	DC light level low.	(Set-point - DCL) > ±0.1V
0x0020	DC light level high.	(DCL - set-point) > ±0.1V
0x0040	Heater voltage low.	<30 mV
0x0080	Heater voltage high.	>2.48V
0x0100	µW power control low.	<20 mV
0x0200	µW power control high.	>2.48V
0x0400	TCXO control voltage low.	<0.1V
0x0800	TCXO control voltage high.	>2.4V
0x1000	Laser current low.	<0.5 mA
0x2000	Laser current high.	>2.3 mA
0x4000	Stack overflow (firmware error).	—

**Note 1:** Alarms indicate detection of out-of-range measurements. Alarms may appear momentarily, due to statistical variation of signals, which do not necessarily indicate performance degradation. If any alarm persists for longer than 1 second, a reboot is initiated.

**2:** Alarm 0x0008 is a non-fatal alarm, provided for information only, and will not initiate a reboot.

**Note:** The telemetry interface allows users to send commands at a rate up to the baud rate. However, sending commands, specifically the telemetry commands (G and ^) may cause unwanted frequency behavior if sent at a rate faster than 1 Hz. Limit telemetry requests to 1/sec to avoid any unwanted-frequency behavior.

### 3.3.2 Frequency Adjustment (F)

The output frequency of the CSAC may be adjusted (steered) through the communications port. The internal resolution of the fractional frequency correction is approximately  $1 \times 10^{-12}$ . The correction is entered in integer units of  $\times 10^{-15}$ . The maximum allowed correction is  $\pm 20000000$  ( $2 \times 10^{-8}$ ). Corrections may be applied as either Absolute or Relative, depending on the first character following the !F, that is !FA or !FD for absolute or relative (delta) respectively. In the case of absolute steering, the value of the Steer register is replaced with the new value.

In the case of relative (delta) steering, the new value is summed with the existing value in the Steer register, that is, two relative corrections of  $-10000$  result in a total offset of  $-2 \times 10^{-11}$ . The current steering value is reported in the steer field of the telemetry in units of  $\times 10^{-12}$ . Note that the reported value of Steer reflects all current steering corrections including the User Steer (entered with !F) as well as the current steering inputs from Disciplining (see **Section 2.10 “1 PPS Disciplining”**) and Analog Tuning (see **Section 2.13 “Analog Tuning”**).

The format for the Adjust frequency command is !FYXXXXXX [CRLF] where Y is either A or D and XXXXX is the new correction in  $\times 10^{-15}$ .

Example: Apply absolute tuning correction of  $-1.23 \times 10^{-10}$ :

Command: !FA-123000 [CRLF]

Unit response: Steer = -123 [CRLF]

Example: Apply delta tuning correction of  $-1.23 \times 10^{-10}$ :

Command: !FD-123000 [CRLF]

Unit response: Steer = -246 [CRLF]

Example: Report current value of steer:

Command: !F? [CRLF]

Unit response: Steer = -246 [CRLF]

**Note:** The single-character F is a shortcut for !F? [CRLF].

The contents of the Steer register are volatile. Steer is reset to 0 when power is cycled to the CSAC. In many cases, it is desirable to preserve the steer upon power-down (for example, calibration of the CSAC). This is accomplished by sending a Frequency Latch command to the CSAC, which updates the internal calibration (stored in non-volatile memory) according to the current value of the Steer register and resets Steer to zero. Note that the Latch command is only valid when the CSAC is locked (Status = 0).

Example: Latch the current steer value:

Command: !FL [CRLF]

Unit response: Steer Latched [CRLF] Steer = 0 [CRLF]

Once a Latch command is issued, the previously latched value cannot be recovered. There is no command to restore “factory defaults”.

**Note:** The frequency steering command (!F) is recommended for real-time disciplining of CSACs, but the value should not be latched (!FL) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage. For example, if a !FL command is applied to the CSAC at a rate of 1/sec, the CSAC may experience operational failure within a few days of operation.

### 3.3.3 Set/Clear Operating Modes (M)

Operating modes of the CSAC are enabled/disabled by individual bits in the mode register. The !M command provides access to set/clear each of the bits independently. The mode register is non-volatile; Settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are shown in the following table.

**TABLE 3-6: OPERATING MODES OF CSAC**

Enable Bit Assignment	Enable Argument to !M_	Definition	Disable Argument to !M_
0x0001	A	Analog tuning.	a
0x0002	—	Reserved.	—
0x0008	S	1 PPS auto-sync.	s
0x0010	D	Discipline.	d
0x0020	U	Ultra-Low Power mode.	u
0x0040	C	Require checksum.	c
0x0080	—	Reserved.	—
—	?	Report current settings.	—

Example: Enable and then Disable disciplining:

Command: !MD [CRLF]

Unit response: 0x0010 [CRLF]

Command: !Md [CRLF]

Unit response: 0x0010 [CRLF]

The current value of the mode register is returned in the standard telemetry query (see **Section 3.3.1 “Telemetry (6 and ^)”**) or may be queried independently with the !M? command.

Example: Query mode register:

Command: !M? [CRLF]

Response: 0x0001 [CRLF]

**Note:** The single-character M is a shortcut for !M? [CRLF].

Autosync mode and Discipline mode are mutually exclusive. Setting either Autosync or Discipline disables the other.

## 3.3.4 1 PPS Synchronization (S)

To synchronize the 1 PPS output (pin 10) to an externally applied synchronization input (PPSEXT, pin 9), connect an external 1 PPS signal to pin 9 and send the !S command. The rising edge of PPSOUT will synchronize to within  $\pm 100$  ns of the next rising edge of the applied PPSEXT. If a valid 1 PPS input does not appear at the PPSEXT within 3 seconds, the operation is aborted and an error is returned.

Example: Synchronize 1 PPS:

Command: !S [CRLF]

Unit response: S [CRLF]

or: E [CRLF]

The unit response (S or E) occurs after either successful synchronization or 3-second timeout, respectively.

**Note:** The single-character S is a shortcut for !S [CRLF].

## 3.3.5 Set 1 PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally supplied 1 PPS reference source may be selected to provide optimal performance in a given application (see **Section 5.1 “The Art of Disciplining”**).

The time constant can range from 10 to 10000 seconds. The 1 PPS disciplining time constant is set with the !D command. The format for setting the time constant is !DX [CRLF] where X is the new time constant in seconds.

Example: Set disciplining time constant to 80 seconds:

Command: !D80 [CRLF]

Response: 80 [CRLF]

To query the current time constant setting, without modifying the value, use the command !D?

Example: Query current disciplining time constant:

Command: !D? [CRLF]

Response: 80 [CRLF]

**Note:** The single-character D is a shortcut for !D? [CRLF].

## 3.3.6 Set Volatile 1 PPS Disciplining Time Constant (d)

A volatile disciplining time constant may be set using the !d command. This time constant will be applied but will not persist across power cycling. This command is useful for quickly disciplining the CSAC during initial calibration while keeping a longer time constant in NVRAM in the event of a power cycle. The format for this command is !dX [CRLF] where X is the volatile time constant in seconds.

Example: Set a temporary time constant to 100 seconds:

Command: !d100 [CRLF]

Response: 100 [CRLF]

## 3.3.7 Set 1 PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1 PPS at the CSAC (see **Section 2.10.1 “Cable Length Compensation”**). Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of  $\pm 250$  (25 ns).

The sign of the compensation is such that a positive value reflects known delay in the arrival time of the 1 PPS. For instance, 2 meters of RG-58 cable requires compensation of approximately +10 ns.

The format for setting the cable length compensation value is `!DCX [CRLF]` where X is the new compensation value.

Example: Set cable length compensation to +15 nanoseconds:

Command: `!DC150 [CRLF]`

Response: `150 [CRLF]`

To query the current compensation setting, without modifying the value, use the command `!DC?`

Example: Query current compensation setting:

Command: `!DC? [CRLF]`

Response: `150 [CRLF]`

To store the current compensation setting in non-volatile RAM, use the command `!DCL`

Example: Latch current value of compensation to power-up default:

Command: `!DCL [CRLF]`

Response: `Phase comp latched [CRLF]`

## 3.3.8 Set Ultra-Low Power Mode Parameters (U)

**Note:** Placing the CSAC in ULP mode results in short-term drift performance of its internal TCXO.

The ultra-low power operating mode is defined by two parameters, Sleep-Time and Wake-Time, which may be set with the `!U` command in this format: `!USSS, WWW [CRLF]` where SSS is the sleep time in seconds and WWW is the wake time in seconds.

Example: Set sleep time = 55 minutes, wake time = 5 minutes:

Command: `!U3300, 300 [CRLF]`

Response: `3300, 300 [CRLF]`

The allowed ranges of Sleep-Time and Wake-Time are 1800 seconds to 65535 seconds and 10 seconds to 65535 seconds, respectively.

To query the ULP settings without modifying their values, use the command `!U?`.

Example: Query current ULP settings:

Command: `!U? [CRLF]`

Response: `3300, 300 [CRLF]`

**Note:** The single-character U is a shortcut for `!U? [CRLF]`.

## 3.3.9 Time-of-Day (TOD)

TOD is maintained internally within the CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the CSAC is powered on. The TOD is synchronized with the 1 PPS output. TOD is routinely transmitted in the telemetry string (see **Section 3.3.1 “Telemetry (6 and ^)”**).

TOD may be set externally with the `!T` command in this format: `!TYXXXX[CRLF]` where Y is either A for absolute setting or D for a delta adjustment of TOD and XXXX is either an unsigned integer TOD or a signed integer adjustment to the TOD.

Example: Absolute setting TOD to 1221578499:

Command: `!TA1221578499[CRLF]`

Unit response: `TimeOfDay = 1221578499[CRLF]`

Example: Retard TOD by 3600 seconds = 1 hour:

Command: `!TD-3600[CRLF]`

Unit response: `TimeOfDay = 1221574902[CRLF]`

The TOD may be reported synchronous with the 1 PPS output:

Example: Retrieve TOD command:

Command: `!T?[CRLF]`

Unit Response: `XXXX[CRLF]` where XXXX is the current TOD.

**Note:** This response does not occur until the next 1 PPS output pulse.

When queried with the `!T?` command, the first character of TOD appears on the communications port within 20 ms following the rising edge of the next 1 PPS output pulse. Because this necessarily creates a delay of up to a second between sending the `!T?` command and receiving a response from the CSAC, the host system must allow for an RS-232 receive timeout of at least 1000 ms when anticipating a response to the `!T?` command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see **Section 3.3.1 “Telemetry (6 and ^)”**).

**Note:** The single-character `T` is a shortcut for `!T?[CRLF]`.

## 3.3.10 Set Threshold for DiscOK Indicator (m)

The DiscOK field in the telemetry data indicates whether the measured PPS error has remained within +/- a user-defined threshold (DiscOKthreshold) for two intervals of the discipline time constant.

To set the DiscOKthreshold, use the command: `!mX[CRLF]` where X is the new DiscOKthreshold in nanoseconds. The range of DiscOKthreshold is 1 nanosecond to  $10^9$  nanoseconds, with a default of 20 nanoseconds.

Example: Set DiscOKthreshold to  $\pm 20$  nanoseconds:

Command: `!m20[CRLF]`

Response: `20[CRLF]`

To query the DiscOKthreshold setting, without modifying the values, use the command `!m?`.

Example: Query current DiscOKthreshold setting:

Command: `!m?[CRLF]`

Response: `20[CRLF]`

**Note:** The single-character `m` is a shortcut for `!m?[CRLF]`.

### 3.3.11 Set PPSwidth (>).

The pulse width of the CSAC 1 PPS output (pin 10) can be changed by using the `!>` command with this format: `!>X[CRLF]`, where `X` is a multiple of the base pulse width. Common base pulse widths for CSAC are listed in [Table 3-7](#).

The allowed range of PPSWidth is from 10  $\mu$ s to 500,000  $\mu$ s.

Example: Set PPSoutMultiplier to 2x multiple of base Pulse Width:

Command: `!>2[CRLF]`

Response: PPS Pulse Width = 2 times ~10 usec [CRLF]

To determine the base pulse width of the CSAC, use the command: `!>??`

Example: Query base pulse width of 10 MHz CSAC SA65

Command: `!>?? [CRLF]`

Response: PPS Pulse Basis = ~100 us [CRLF] or PPS Pulse Basis = ~10 us [CRLF]

**Note:** The difference between pulse widths between CSACs with the same output frequency is due to improved hardware control in newer SA65 units. It is recommended to query the base pulse width once during development to confirm the base pulse width.

**TABLE 3-7: COMMON BASE PULSE WIDTHS FOR CSAC**

SA65 Frequency (MHz)	Base Pulse Width ( $\mu$ s)
10.000	100 or 10
16.384	97.68 or 10
40.000	10

Alternatively, you can set the width of PPSOUT signal in microseconds by using the `!>u` command with this format `!>uX[CRLF]` where `X` is the number of microseconds of the desired pulse width. However, the CSAC is still restricted to multiples of the base width. If a pulse width that is not a multiple of the base width is entered, the CSAC will round to the nearest multiple.

Example: Set PPSWidth to 30  $\mu$ s

Command: `!>u30`

Response: PPS Pulse Width = 30 usec

Example: Set PPSWidth to 46  $\mu$ s

Command: `!>u46`

Response: PPS Pulse Width = 50 usec

To query the 1 PPS Out Pulse Width setting, without modifying the values, use the command `!>?`

Example: Query current 1 PPS Out Pulse Width as a multiple of the base width:

Command: `!>?[CRLF]`

Response: PPS Pulse Width 4 =times ~100 usec[CRLF]

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Example: Query current 1 PPS Out Pulse Width in  $\mu$ s

Command: !>u?[CRLF]

Response: PPS Pulse Width = 50 usec[CRLF]

**Note:** The single-character > is a shortcut for !>?[CRLF].

### 3.3.12 Set HeaterBoostLimit (.)

The maximum power draw of the CSAC Heater control circuits may be set controlled by setting the value of HeaterBoostLimit.

The allowed range of HeaterBoostLimit is from 50 to 250. The default value is 50.

Example: Set HeaterBoostLimit to 50 mW:

Command: !.50[CRLF]

Response: Heater power limit (mW): 50 [CRLF]

**Note:** The single-character . is a shortcut for !.?[CRLF].

### 3.3.13 Report Part Number (p)

The CSAC part number may be retrieved with the 'p' command. The stored part number is a free-form ASCII string of maximum length 15 bytes, including a NULL terminator.

Example: Retrieve Part Number:

Command: !p?[CRLF]

Response: Part Number: xxx-xxxx-xxx [CRLF]

### 3.3.14 Help (?)

The following table lists all available commands in response to the ? command.

**TABLE 3-8: UNIT RESPONSE TO HELP COMMAND (?)**

Command	Description
F-	Adjust frequency.
^-	Telemetry.
6-	Telemetry headers.
D-	Set 1 PPS discipline tau.
m-	Set 1 PPS discipline threshold for TIC in ns.
>-	Set 1 PPS out pulse width as 1–4 times default.
S-	Sync 1 PPS.
U-	Set parameters for ultra-low power mode.
M-	Change mode register.
T-	Change/report time of day.
.-	Adjust heater boost limit.
?-	Show this list.

**Note:** The single character ? is a shortcut for !?[CRLF].

## Chapter 4. Development Kit

The CSAC Development Kit includes hardware and cabling to facilitate validation of performance, brass-board demonstrations, and software interface development.

### 4.1 PACKAGE CONTENTS

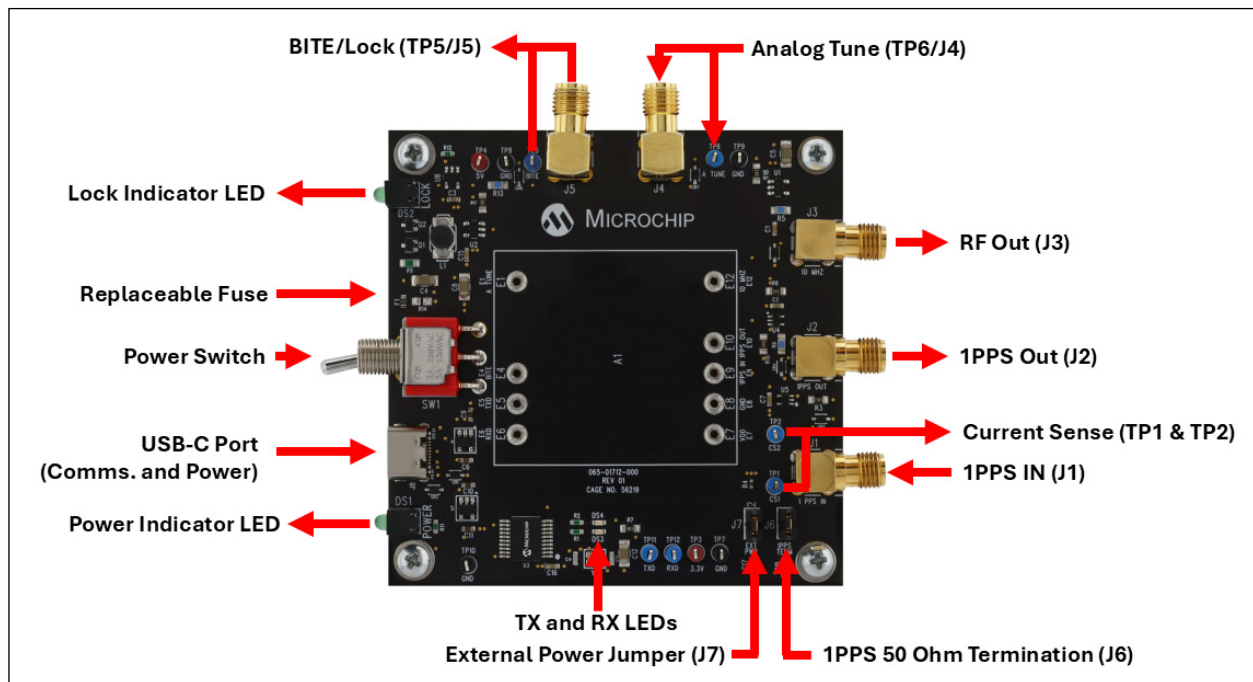
The following table lists the contents of the CSAC Development Kit (part number 090-04326-000).

**TABLE 4-1: CONTENTS OF CSAC DEVELOPER'S KIT**

Item	Part Number	Notes
Evaluation Board Assembly	066-01105-000	See <a href="#">development kit webpage</a> for schematic
USB C to USB A Cable	160-00999-000	USB 2.0 Standard.

### 4.2 EVALUATION BOARD OVERVIEW

Detailed schematics of the evaluation board are provided on the product page for the CSAC Development Kit. The following illustration shows the connections to the evaluation board.



**FIGURE 4-1: Evaluation Board Overview.**

The following items are included in the development kit PCB.

- **RF Output (SMA):** The CSAC output is an RF, CMOS 0VDC to 3.3VDC waveform. A high-speed buffer (U1) on the evaluation board converts the CMOS output to an AC-coupled output capable of delivering 10 dBm to a 50Ω load.

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- **3.3VDC Jumper (J7):** The evaluation board provides regulated 3.3VDC to the CSAC. In order to allow convenient measurement of the CSAC power consumption, a jumper is provided in the  $V_{CC}$  connection to the CSAC. To measure the CSAC current draw, turn off the evaluation board and install a low-impedance current meter in place of the jumper. Observe proper ESD protocols in making this measurement.
- **Replaceable Fuse (F1):** Littelfuse part number 0453 01.5.
- **USB-C Connection:** The evaluation board provides a serial to UART converter for connection to a PC. Connect the evaluation board (J1) to a PC with a USB-A to C 2.0 cable. Development Board revisions A and B do not support USB C to C cables. Use the provided cable to avoid complication.
- **Lock Indicator LED:** Indicates normal operation following initial acquisition of the clock signal. This is the logical complement of the BITE output (CSAC pin 4).
- **BITE (J5 & TP5):** This is a buffered output from pin 4 of the CSAC.
- **Power Switch:** Controls power to the evaluation board and to the CSAC.
- **Power LED:** Indicates the state of the power switch.
- **Analog Tuning Input (J4 & TP6):** This input is directly connected to pin 1 of the CSAC.
- **1 PPS Input (SMA):** The 1 PPS input connection to the evaluation board accepts a 1 PPS reference with peak amplitude between 3.3V-6V and generates a 0V to 3.3V CMOS pulse to the CSAC. By default, the 1 PPS input is terminated by a 50 $\Omega$  resistor. When 1 PPS IN is provided by a high-impedance source, remove J6 to remove the 50 $\Omega$  termination. See [Figure 4-1](#) for the location of J6 on the evaluation board.
- **1 PPS Output (SMA):** The 1 PPS output is buffered by a CMOS 0V to 3.3V logic gate on the evaluation board.
- **Current Sense Resistor (TP1 & TP2):** To monitor current draw of the CSAC, a 0.1 $\Omega$  resistor is placed in series on the VDD line. Measuring the voltage drop across TP1 and TP2 may be used to measure the VDD current.
- **TX and RX Test Points:** The TXD and RXD pins (CSAC Pins 5 & 6) can be directly accessed via TP11 & TP12. If these TPs are used, it is recommended to remove R7 to remove any interference from the USB/UART controller.

## 4.3 INSTALLING THE CSAC ON THE EVALUATION BOARD

### CAUTION

To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

Remove the CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment.

**Note:** The CSAC pinout is keyed (see [Table 1-1](#)) so the CSAC can only be inserted in the proper orientation. Gently insert the CSAC into the socket on the evaluation board.

Make sure the power switch is OFF on the evaluation board, as shown in [Figure 4-1](#). Connect the USB-C cable between J6 and an available USB port on your PC.

CSAC signal outputs are available from the evaluation board on connectors J3 (RF) and J2 (1 PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, and so on).

## 4.4 CLOCKSTUDIO SOFTWARE INFORMATION

The Microchip Clockstudio™ software provides a graphical user interface for monitoring and controlling the CSAC. Clockstudio may also be used for collecting and archiving monitor data from the CSAC. It can be run on any PC that runs Windows 10 or 11 and has at least one available Virtual COM Port.

**Note:** Multiple CSACs can be monitored from a single PC, provided additional USB and Virtual COM ports are available.

The software installation and software user's guide is available for download from the Microchip website: <https://www.microchip.com/clockstudio>

Upon accepting the default installation options (recommended), Clockstudio is installed in C:\Users\\AppData\Local\Programs\Clockstudio, a startup icon is added to the Start > Microchip > Clockstudio menu, and a Clockstudio icon is placed on the desktop.

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NOTES:

## Chapter 5. Design Guide

The following sections are the design guide for the CSAC.

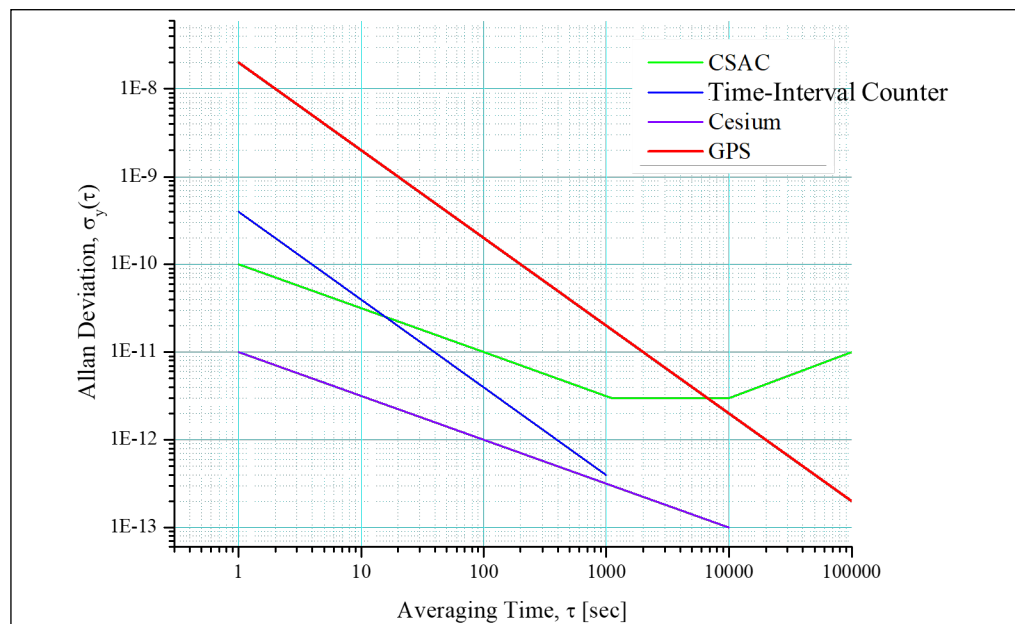
### 5.1 THE ART OF DISCIPLINING

Implemented correctly, disciplining can be utilized to calibrate the CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (time and frequency drift) of the CSAC. At the same time, the disciplined CSAC may be used to clean-up the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, disciplining may degrade the performance of the CSAC. For example, if the CSAC disciplined with a short time constant to a source that is noisier than CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the CSAC, the reference source, and the time-interval counter (TIC), and selecting the appropriate time constant that makes the best use of the available timing information.

The following graph shows typical instability (Allan Deviation) of the CSAC (in green), along with the noise floor of the phase meter (in blue). Also shown are the instabilities of typical reference sources, GPS (in red) and a high-performance cesium beam frequency standard (in purple).



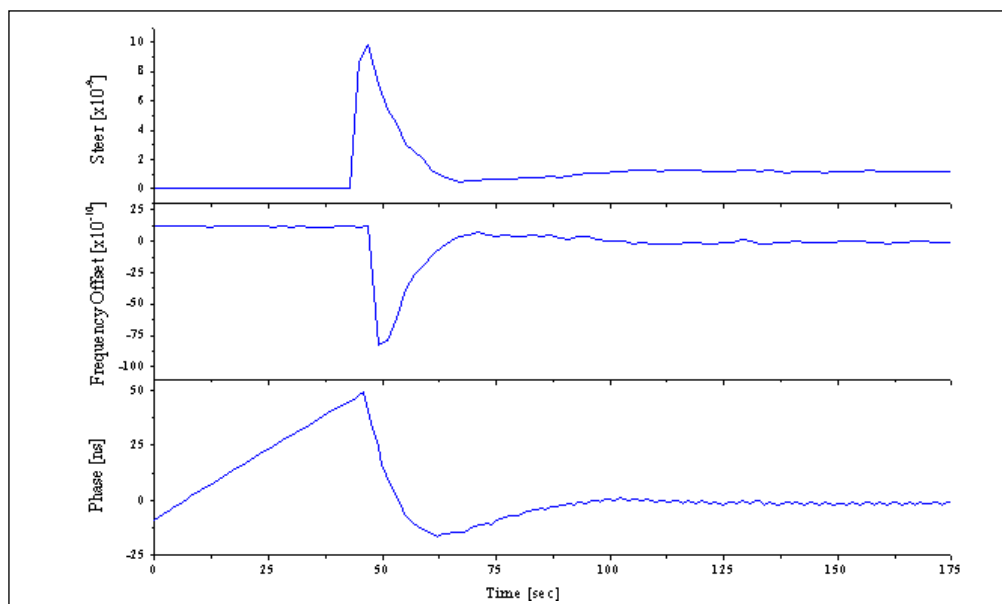
**FIGURE 5-1:** Frequency Stability (Allan Deviation) Versus Averaging Time.

When disciplining, the stability of the output of the CSAC (combined clock) at any averaging time reflects the noise properties of the dominant (most noisy) source. For example, if disciplining the CSAC to a GPS source, which is noisier than the CSAC for averaging times  $\tau < 5000$  seconds, the disciplining time constant should be set to  $\tau > 5000$  seconds so that the (superior) CSAC stability dominates for  $\tau < 5000$  seconds

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and the (superior) GPS stability dominates for  $\tau > 5000$  seconds. On the other hand, consider the case where the CSAC is disciplined to a high-performance cesium clock, which is more stable than the CSAC on all time scales. The noise is dominated by the TIC for  $\tau < 2$  seconds and by the CSAC for  $\tau > 2$  seconds. In this case, the disciplining time constant could be set to  $\tau = 2$  seconds for optimal performance.

The following graph shows an example of a CSAC, which is disciplined to a superior reference (in this case a hydrogen maser) with a time constant of 20 seconds. For this measurement, the CSAC was deliberately mis-tuned in both frequency ( $y$ ) and phase ( $\phi$ ) prior to the measurement, by  $y = 10 \times 10^{-10}$  and  $\phi = 50$  ns.



**FIGURE 5-2:** CSAC Disciplined to a Superior Reference.

In the previous graph, when disciplining was enabled, at  $t = 45$  seconds, the steering algorithm immediately inserted a frequency offset of  $-9 \times 10^{-9}$ , to steer out the 50 ns time error with 20 second time constant. The steering gradually reduces as the phase approaches zero such that both frequency and time error are corrected to within  $1/e$  of their initial values at one time constant (20 seconds) and  $1/e^4$  within two time constants (40 seconds). After five to six time constants ( $\approx 100$  seconds), frequency and time error are corrected to within  $\pm 5 \times 10^{-13}$  and  $\pm 5$  ns, respectively.

## 5.2 HEAT SINK

The CSAC does not require a heat sink because it consumes low power and therefore produces little heat. Furthermore, the external parts of CSAC are mu-metal (80% nickel), which is a poor thermal conductor (1/5 that of aluminum). There is no useful thermal path from the inside components to the baseplate or the cover.

## 5.3 NOTES ON SOLDERING

For initial testing and evaluation, it is recommended that the pins must not be modified or soldered to a PCB. The recommended socket for PCB attachment is Tyco P/N 4-5332070-4.

After evaluation, the pins can be hand soldered to a PCB using 63/37 tin/lead solder with a maximum soldering tip temperature of 329°C (625°F).

Hand soldering is a necessary requirement for CSAC, and solder re-flow is not recommended because the CSAC cannot go above storage temperature (it is likely to damage it).

The lead material is 52 Alloy with a plating of 50 µin gold minimum (ASTM 8488-01) over 100 µin nickel (QQ-N-290).

## 5.4 WRITES TO NVRAM

CSAC has a physical limit to the number of writes to NVRAM. As a best practice, and to maximize the life time of the memory devices, it is advisable to restrict the number of NVRAM writes as necessary.

The following are the scenarios of a write to NVRAM:

- Issuing a Frequency Latch command (format `!FL`) causes an NVRAM write.
- Issuing a PPS cable length compensation latch command (format `!DCL`) causes an NVRAM write.
- Issuing a PPS disciplining tau set command that changes discipline tau (format `!Dn` where n is a decimal number) causes an NVRAM write.
- Issuing a mode command that changes mode register (format `!Mx` where x is an alphabetical character) in list below causes an NVRAM write:
  - Communications Checksum on/off (`!MC` vs `!Mc`)
  - PPS auto-sync on/off (`!MS` vs `!Ms`)
  - PPS disciplining on/off (`!MD` vs `!Md`)
  - Analog tuning on/off (`!MA` vs `!Ma`)
  - ULP on/off (`!MU` vs `!Mu`)
- Issuing a ULP configuration command (format `!Un,p` where n and p are decimal numbers) causes an NVRAM write.
- Every ULP cycle, firmware does an automatic NVRAM write.
- Issuing a HeaterBoostLimit set command that changes HeaterBoostLimit (format `!.x`, where x is a decimal number) causes an NVRAM write.
- Every auto-reset (status 0->8) due to alarm where status reverts from lock state, firmware does an automatic NVRAM write.
- Periodically every 30 days in clock-lock state, firmware does an automatic NVRAM write.
- Issuing a PPS pulse width set command that changes pulse width (format `!>N` where N is a decimal number) will cause an NVRAM write.
- Issuing a DiscOKthreshold command that changes DiscOKthreshold (format `!mN` where N is a decimal number) will cause an NVRAM write.
- Lock set points are saved after each acquisition of a lock state. This write occurs ~102 seconds after Lock is achieved.

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