REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-04-08

DOCUMENT DESCRIPTION

Component Placement Checklist for the LAN9311I, 128-pin XVTQFP Package

SMSC
80 Arkay Drive
Hauppauge, New York 11788

Document Number	Revision
CC524344	A

Component Placement Checklist for LAN9311I

Information Particular for the 128-pin XVTQFP Package

LAN9311I XVTQFP Phy No. 1 Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXP1, pin 111) as close to the LAN9311I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXN1, pin 110) as close to the LAN9311I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (RXP1, pin 116) as close to the LAN9311I as possible.

4. Place the 49.9 Ω RX termination pull-up (RXN1, pin 115) as close to the LAN9311I as possible.

LAN9311I XVTQFP Phy No. 2 Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXP2, pin 126) as close to the LAN9311I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXN2, pin 127) as close to the LAN9311I as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (RXP2, pin 123) as close to the LAN9311I as possible.

4. Place the 49.9 Ω RX termination pull-up (RXN2, pin 124) as close to the LAN9311I as possible.

LAN9311I XVTQFP Magnetic No. 1:

1. Place the 10.0 Ω TX/RX Channel Center Tap feed resistor as close to the magnetics as possible.

2. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

3. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

LAN9311I XVTQFP Magnetic No. 2:

1. Place the 10.0 Ω TX/RX Channel Center Tap feed resistor as close to the magnetics as possible.

2. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

3. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

RJ45 Connector No. 1 & No. 2:

1. Place the RJ45 connector, the magnetics and the LAN9311I XVTQFP as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9311I XVTQFP.

3. Select and place the magnetics as to set up the best routing scheme from the LAN9311I XVTQFP to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

4. Place the Unused Wire Pair termination resistors and the 1000 ρF, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.

5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

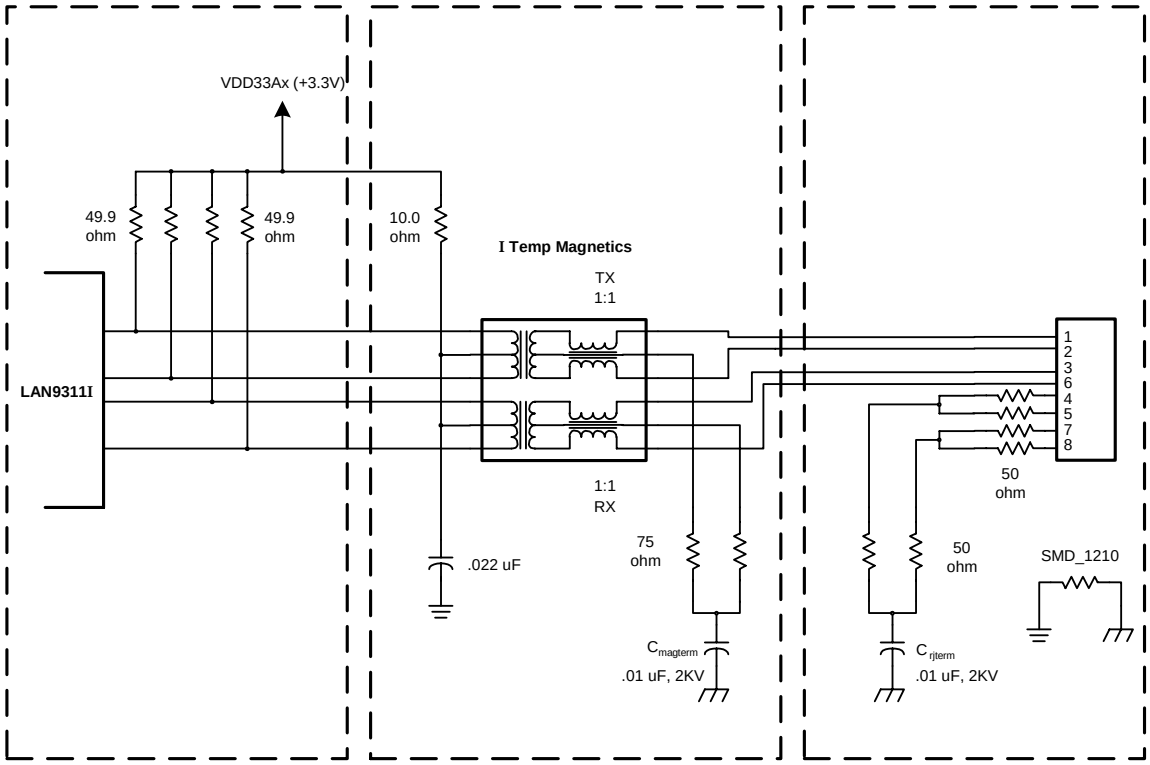

Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TXP & TXN signals placed close to the LAN9311I for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

+3.3V Power Supply Connections:

1. Place the (16) VDD33IO decoupling capacitors for the LAN9311I XVTQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the (2) VDD33A1 decoupling capacitors for the LAN9311I XVTQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the (2) VDD33A2 decoupling capacitors for the LAN9311I XVTQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

4. Place the (1) VDD33BIAS decoupling capacitor for the LAN9311I XVTQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

VDD18CORE:

1. VDD18CORE (pin 74) requires a 0.01 μF bypass capacitor and a low ESR 4.7 μF bulk capacitor placed as close as possible to pin 74.

2. The other (6) VDD18CORE pins only require a 0.01 μF bypass capacitor placed as close as possible to each pin.

3. VDD18PLL (pin 107) requires a 0.01 μF bypass capacitor placed as close as possible to pin 107.

VDD18TX2:

1. VDD18TX2 (pin 121) requires a 0.01 μF bypass capacitor and a low ESR 4.7 μF bulk capacitor placed as close as possible to pin 121.

2. VDD18TX1 (pin 118) requires a 0.01 μF bypass capacitor placed as close as possible to pin 118.

Ground Connections:

1. There are no component placement issues associated with the LAN9311I XVTQFP ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25 MHz crystal, the 1.0 M Ω parallel resistor, the zero ohm series EMI resistor and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN9311I XVTQFP (XI, pin 105 & XO, pin 106) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.

EEPROM Interfaces:

Microwire™ (3-wire) EEPROM Interface:

1. There are no component placement issues associated with the Microwire™ EEPROM Interface supported by the LAN9311I XVTQFP device.

I^2C (2-wire) EEPROM Interface:

1. There are no component placement issues associated with the I^2C EEPROM Interface supported by the LAN9311I XVTQFP device.

EXRES Resistor:

1. Place the EXRES resistor as close to pin 119 of the LAN9311I XVTQFP as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN9311I XVTQFP.

CPU Interface:

1. The design engineer must review placement issues associated with the Host Bus CPU Interface. Specific processor design guidelines should be reviewed in determining the placement of the LAN9311I device with respect to the processor. Address, data and control signal trace lengths must be considered when placing these two devices. Critical timing issues may arise if recommended trace lengths are exceeded.

Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.

2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.