AN4598

SAMA7G54 Hardware Design Considerations

Scope

This document is intended to facilitate the bring-up of any hardware design featuring a SAMA7G54 MPU by providing a short checklist intended for the hardware designer.

Abbreviations

- SDRAM – Synchronous Dynamic Random-Access Memory
- DDR – Double Data Rate
- LP – Low Power
- PCB – Printed Circuit Board
- PMIC – Power Management Integrated Circuit
- MIPI – Mobile Industry Processor Interface

References

Type	Name	Literature No.	Available
Data sheet	SAMA7G5 Series	DS60001765	www.microchip.com/en-us/product/SAMA7G54
Errata	SAMA7G5 Series Silicon Errata and Data Sheet Clarification	DS80001016	www.microchip.com/en-us/product/SAMA7G54
Application note	Microchip MPU Power Solutions Tips and Tricks	AN4298	www.microchip.com/en-us/application-notes/an4298
Board design files	SAMA7G54-EK board design files	–	www.microchip.com/en-us/development-tool/EV21H18A

1. Design Checklists

1.1 Schematic Checklist

- Is the MPU supplied with the correct voltage levels?
- Does the power management IC provide enough current for the system?
- Are the correct power supply power-up and power-down sequences implemented?
- Are the decoupling capacitors adequate?
- Is the MPU configured correctly?
- Is the DDR controller configured correctly?

1.2 Layout Checklist

- Does the board feature an uninterrupted GND plane?
- Is a proper layer stack-up defined?
- Are the decoupling capacitors placed as close as possible to the IC pins?
- Are high-speed signal lengths matched and routed over continuous planes (USB, SDCARD, DDR, etc.)?

2. Schematic Checklist Description and Examples

This section describes each item in the schematic checklist and provides implementation examples.

2.1 Provide Adequate Voltage and Sufficient Current

2.1.1 Requirements

For the power supplies needed to power the MPU, refer to the Power Supply Inputs table, in section “Recommended Operating Conditions” of chapter “Electrical Characteristics” in the SAMA7G5 Series data sheet.

2.1.2 Implementation Example

The MCP16502 and MCP16501 PMICs are specially designed for SAMA7G5 applications, as they can output all the power supply domains required by the MPU.

Refer to the chapter “Microchip Recommended Power Management Solutions” in the SAMA7G5 Series data sheet for a simplified power supply implementation using the MCP16502 and MCP16501 PMICs.

2.1.3 Implementation Hints

- Use pull-up resistors on the reset (nRSTO) and interrupt (nINTO) signals.
- Use a 100k pull-up resistor on the wake-up (nSTRTO) signal, referenced to the back-up power supply, if implemented.
- Refer to the “Microchip MPU Power Solutions Tips and Tricks” application note for solutions that enable and facilitate the use of PMICs.

2.2 Ensure Correct Power-up and Power-down Sequences

2.2.1 Requirements

In the section Recommended Power Supply Sequencing of the chapter “Electrical Characteristics” in the SAMA7G5 Series data sheet, refer to the figures “Recommended Power Sequence at Power-up” and “Recommended Power Sequence at Power-down” for the applicable power supply sequencing.

The Power-up Timing Specification table shows the following:

- There should not be a delay of more than 0.2 ms between the establishment of VDDIN33 and the establishment of VBAT.
- The VDDIN33 rail and periphery group can be established at the same time, or the VDDIN33 rail can be established before the periphery group.
- The periphery group and the core group can be established at the same time, or the periphery group can be established before the core group.
- The NRST signal should be held low for at least 8 ms after the last established supply group.

The Power-down Timing Specification table shows the following:

- NRST should be held low before or at the same time as the first supply turn-off.

The above power-up and power-down requirements are already implemented in the MCP16502/1 PMIC solutions.

2.3 Ensure that the Power Supply Pins have Adequate Decoupling Capacitors

2.3.1 Requirements

Low-impedance decoupling/filtering of the device power supply inputs must be provided. A 100 nF ceramic X7R (or X5R, X7S) capacitor placed very close to each power supply input is a minimum requirement. A 4.7 µF ceramic X7R (or X5R) ceramic capacitor should also be placed on the VDDCPU, VDDUTMI, VDDIN33 and VDDIODDR power

rails, close to the MPU. The VDDCORE power input should have two 4.7 µF ceramic capacitors placed close to the MPU.

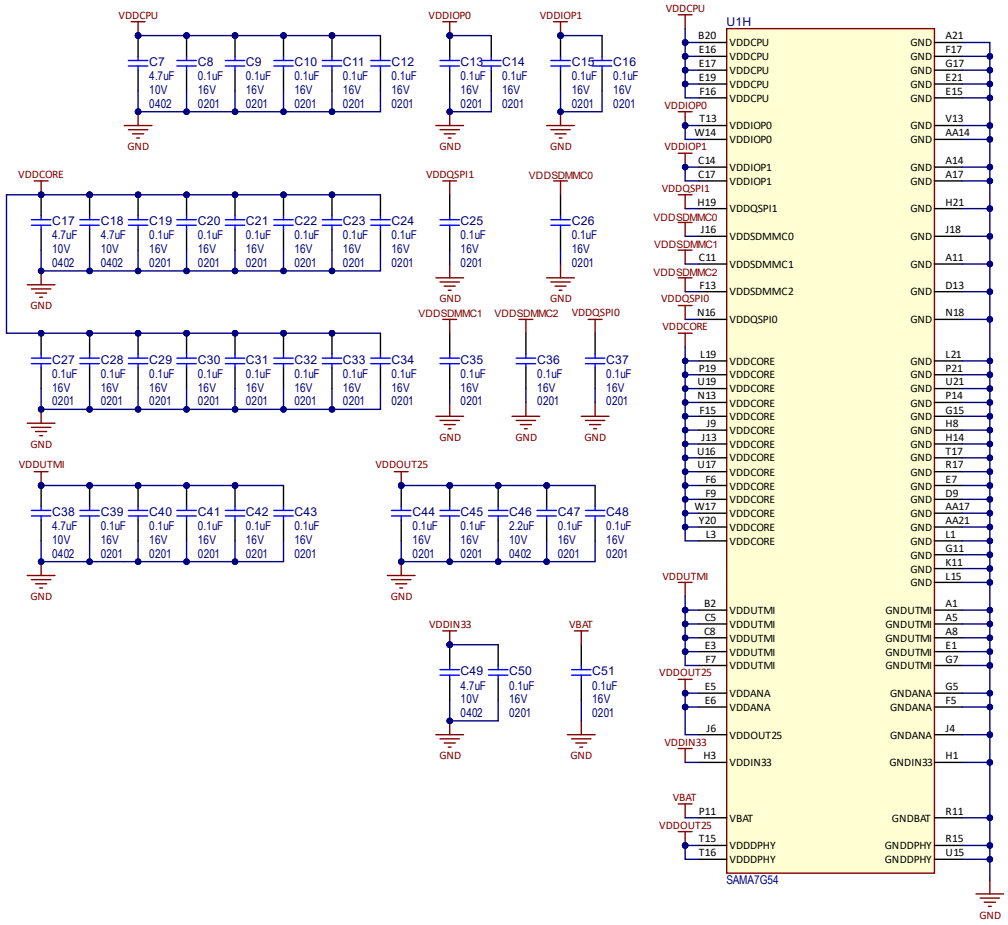
A 2.2 µF X7R (or X5R) ceramic capacitor should also be placed close to the VDDOUT25 power output pin.

The VDDANA and VDDDPHY power inputs should be connected to the VDDOUT25 power output.

In the SAMA7G54-EK design, we opted for 100 nF 0201, X7S rated at 16V and 4.7 µF 0402, X5R rated at 10V multilayer ceramic capacitors with good results. Small sized capacitors provide better decoupling due to reduced inductance.

2.3.2 Implementation Example

Figure 2-1. Processor Power Inputs



2.4 Check MPU Configuration

2.4.1 Requirements

- A 200 Ω tuning resistor is connected to the HHSx_RTUNE pin of each USB port.
  - Refer to “Typical Connection” in chapter “USB 2.0 PHY” of the SAMA7G5 Series data sheet.
- The TST pin is grounded.
- If the design does not need JTAG boundary scan, tie the JTAGSEL pin to GND or leave it floating.
- A tuning resistor is connected to the QSPI0_CAL and SDMMCx_CAL pins of each interface. Use a 20 kΩ resistor for 1.8V QSPI/SDMMC memories or a 16.9 kΩ resistor for 3.3V memories. If the memory device operates in both 1.8V and 3.3V modes, use a 20 kΩ resistor.

- A 4.02 kΩ tuning resistor is connected to the MIPI_REXT pin.
- All resistors connected to calibration inputs should have a tolerance of ±1% or better.
- A 32.768 kHz crystal oscillator is placed between XIN32 and XOUT32.
  - Refer to “32.768 kHz Crystal Oscillator” in chapter “Electrical Characteristics” of the SAMA7G5 Series data sheet.
- A high-frequency clock source is provided either through a crystal oscillator placed between XIN and XOUT or through an external clock generator.
  - Refer to “Main Crystal Oscillator” in chapter “Electrical Characteristics” of the SAMA7G5 Series data sheet if a crystal oscillator is used as main clock source.
- If the clock generator option is chosen, it is recommended to ground XOUT to improve stability.
- Clock sources should be chosen with great care. In chapter “Electrical Characteristics” of the SAMA7G5 Series data sheet:
  - Refer to “Crystal Oscillator Design Considerations” for a list of useful parameters when choosing crystal oscillators.
  - Refer to the formulas in "32.768 kHz Crystal Oscillator" and "Main Crystal Oscillator" to calculate the value of the external load capacitors of the crystal oscillators.

2.4.2 Implementation Example

Figure 2-2. 32.768 kHz Crystal Oscillator Connection

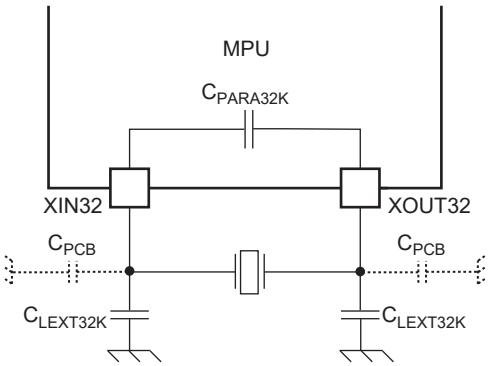


Figure 2-3. Main Crystal Oscillator Connection

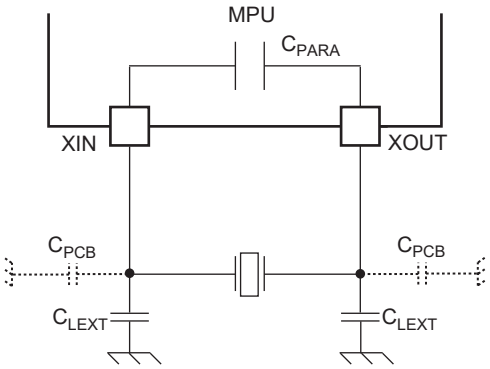
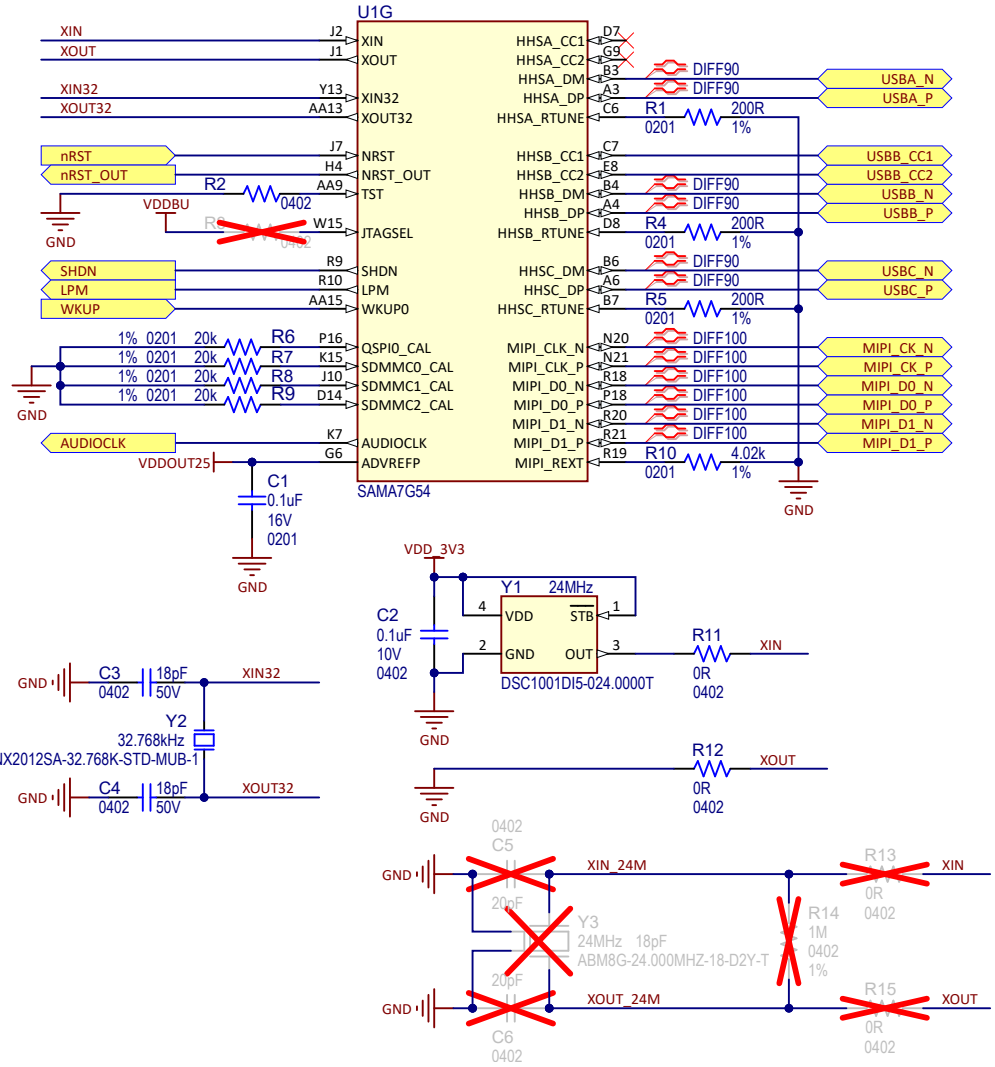


Figure 2-4. Processor Configuration



In the above design schematic, the SAMA7G54 MPU features the 24 MHz DSC1001DI5-024.0000T MEMS oscillator as default main clock source and the NX2012SA-32.768K-STD-MUB-1 crystal loaded with 18 pF capacitors to provide the 32.786 kHz slow clock. Alternatively, by removing the R11 and R12 resistors and populating the corresponding parts associated with Y3, the ABM8G-24.000MHZ-18-D2Y-T 24 MHz crystal oscillator can be used as main clock source.

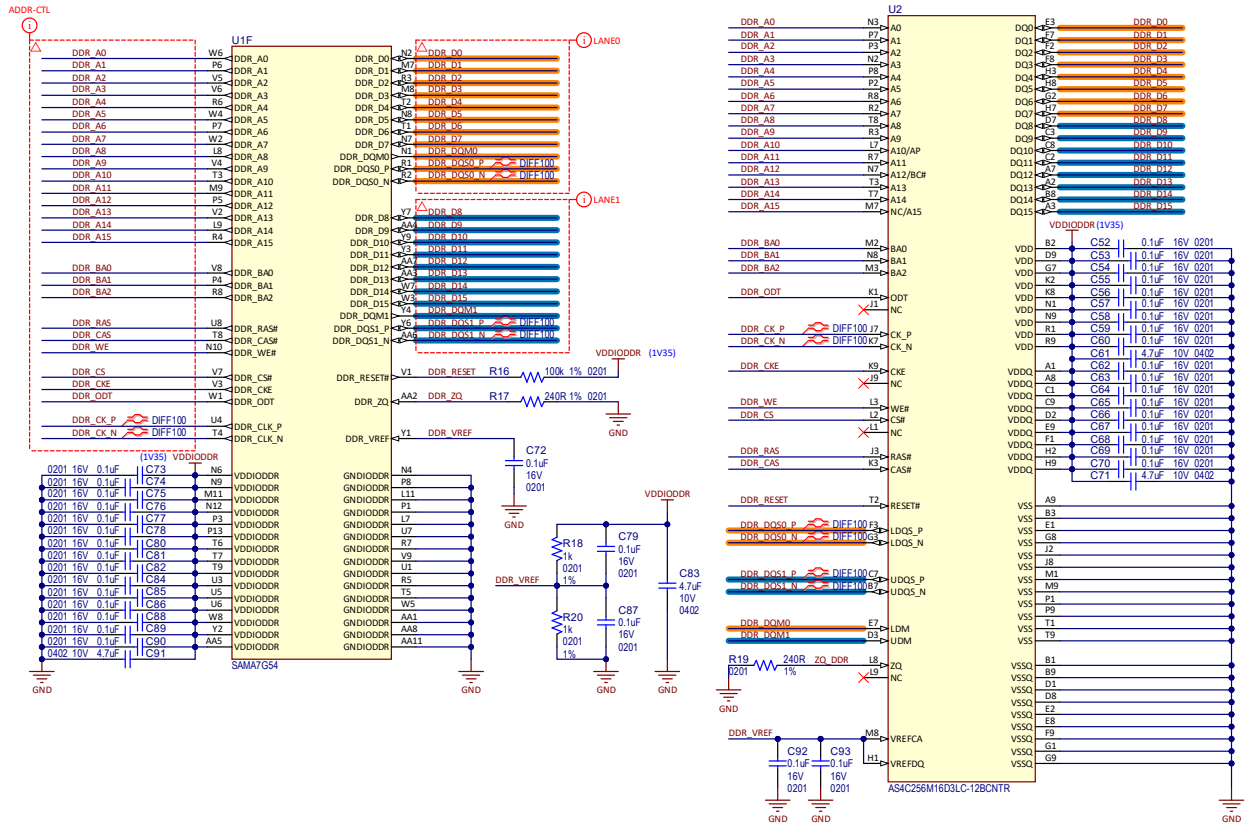
2.5 Check the DDR Controller Configuration

2.5.1 Requirements

- Connect the external memory chosen as required in table “I/O Lines Usage vs. Operating Mode” in chapter “Universal DDR Memory Controller (UDDRC)” of the SAMA7G5 Series data sheet.
- The DDR_ZQ calibration cell input should be connected to ground with a 240 Ω ±1% resistor. The same resistor value is used regardless of the chosen memory device type.
- Use a filtered simple voltage divider made with two 1 kΩ ±1% resistors to generate the DDR_VREF voltage from the VDDIODDR rail. DDR_VREF should be half the voltage of VDDIODDR and should be connected to the DDR_VREF pin of the MPU.

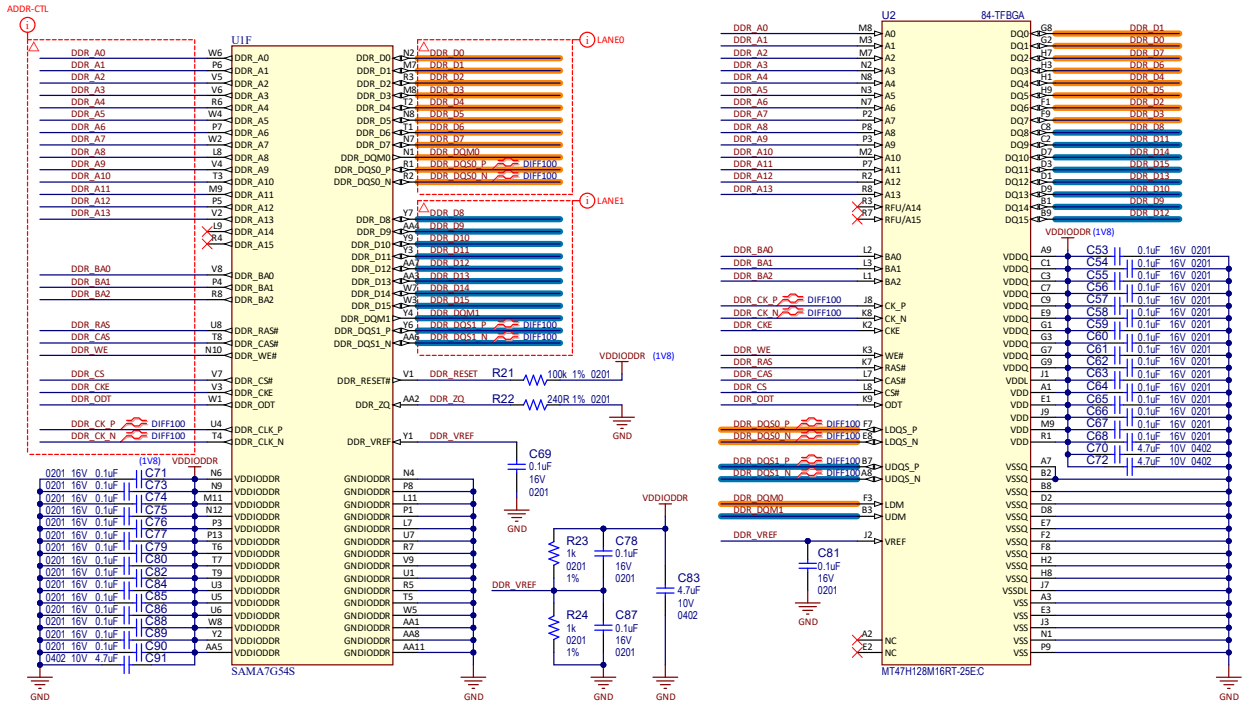
2.5.2 Implementation Example for 16-bit DDR3L

Figure 2-5. 16-bit DDR3L Hardware Configuration



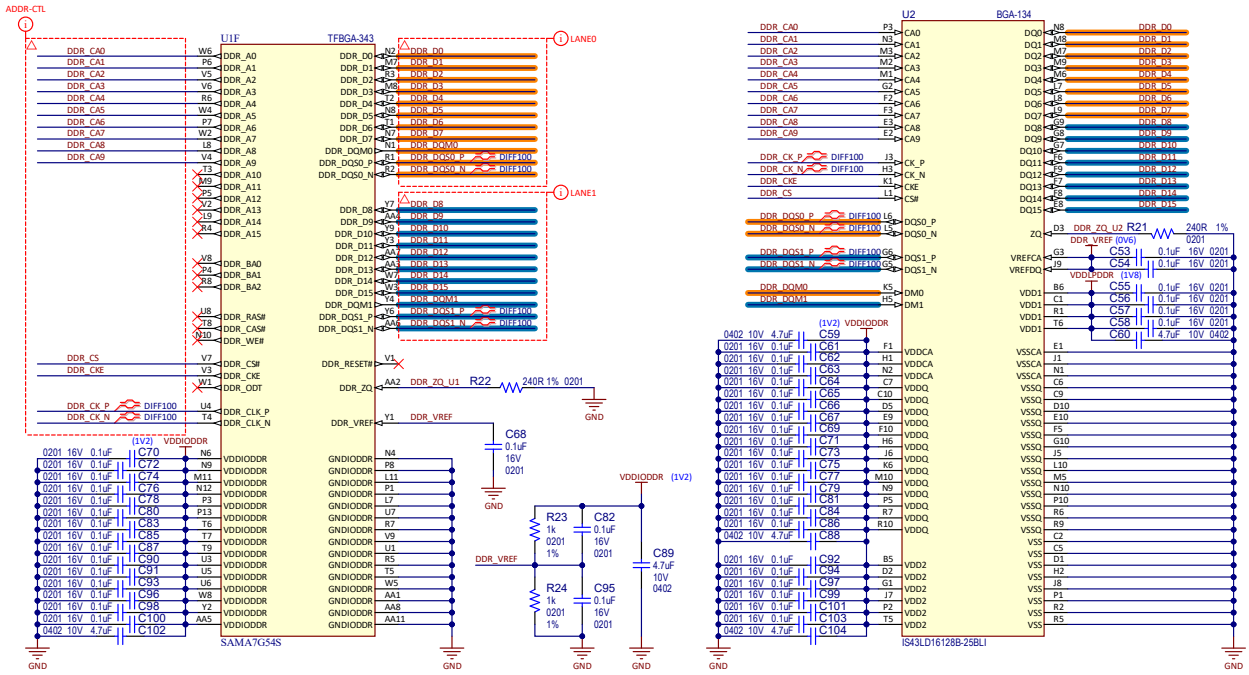
2.5.3 Implementation Example for 16-bit DDR2

Figure 2-6. 16-bit DDR2 Hardware Configuration



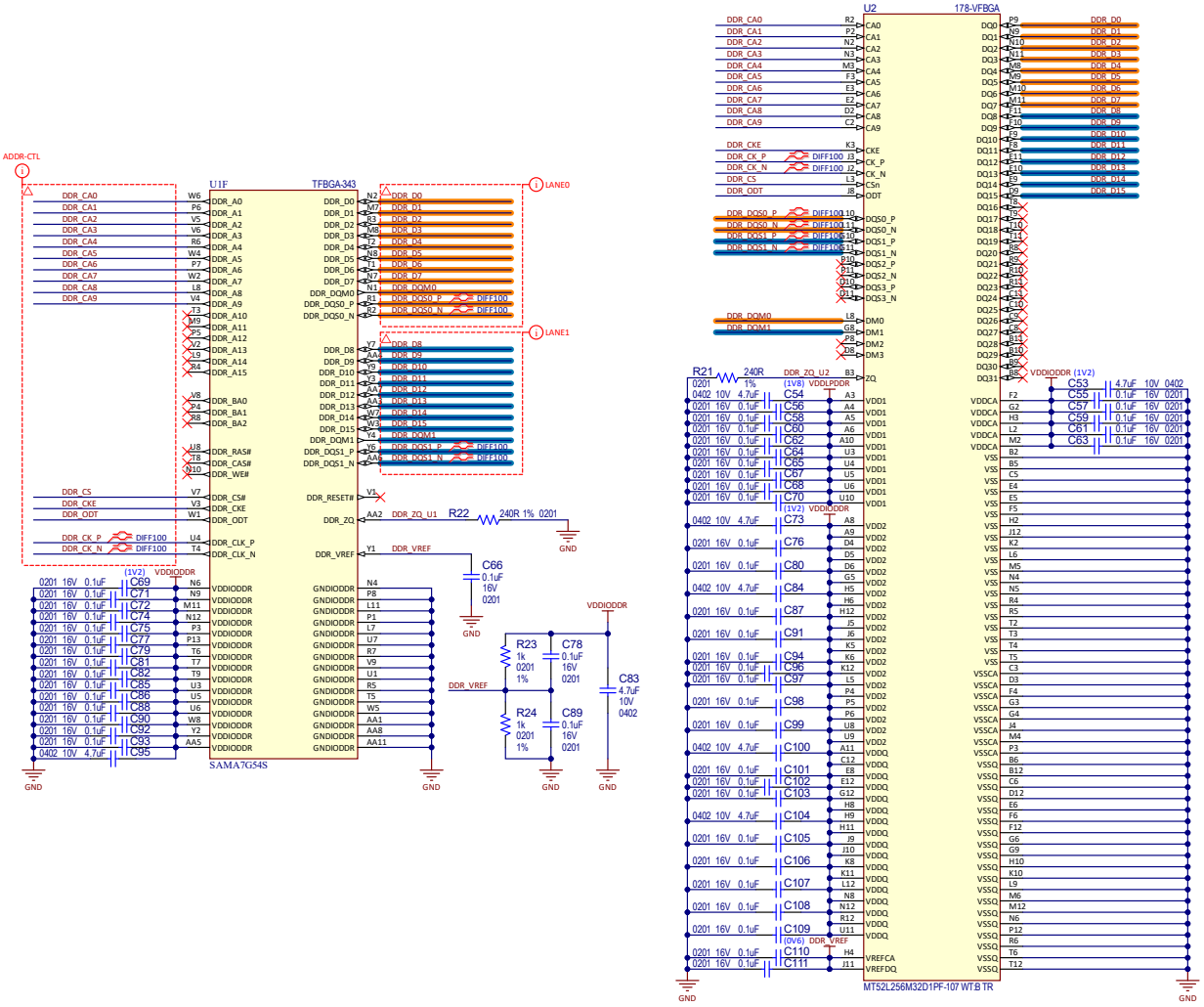
2.5.4 Implementation Example for 16-bit LPDDR2

Figure 2-7. 16-bit LPDDR2 Hardware Configuration



2.5.5 Implementation Example for 16-bit LPDDR3

Figure 2-8. 16-bit LPDDR3 Hardware Configuration



Refer to the CAx LPDDR2 Signal Connections table in chapter “Universal DDR Memory Controller (UDDRC)” of the SAMA7G5 Series data sheet for the correct signal connection of LPDDR2/LPDDR3 devices.

2.6 Check Other Interface Features

2.6.1 Recommendations

- If an Ethernet PHY is connected to the GEMAC0 pins of the MPU, unless the PHY supports adjustable drive strength, it is recommended that series resistors (33 Ω for ex) are placed on the RX lines of the interface, close to the PHY.
- If CMOS-compatible output oscillators are used as clock sources for the MPU, Ethernet PHYs or other devices, their active low standby pin (if present) can be driven low by an N-channel MOSFET controlled by the LPM pin of the MPU. This feature helps reduce power consumption during certain low-power modes, when those clock sources are not used.
- If the application requires current measurement of certain power rails, those rails can be split by shunt resistors.
- The NRST_OUT pin of the MPU can be used as a reset source for other devices used in the design (QSPI memories, Ethernet PHYs, etc.)

- Each SDMMC interface has its own dedicated reset pin (SDMMCx_RSTN). It can be used to reset SDIO devices or to perform power cycles on SD Cards.
- It is recommended to use ports PD16 (FLEXCOM3_IO0 - TX) and PD17 (FLEXCOM3_IO1 - RX) as a serial debug console, since those ports are configured by default for this function at power-up.

3. Layout Checklist Description and Examples

This section describes each item in the layout checklist and provides implementation examples.

The implementation examples are based on the SAMA7G54-EK (Evaluation Kit).

3.1 Check that the Board has an Uninterrupted GND Plane

3.1.1 Requirements

A PCB with a low-impedance ground plane must be provided. A single unbroken ground plane is a minimum requirement.

3.1.2 Implementation Example

Figure 3-1. Correct GND Plane

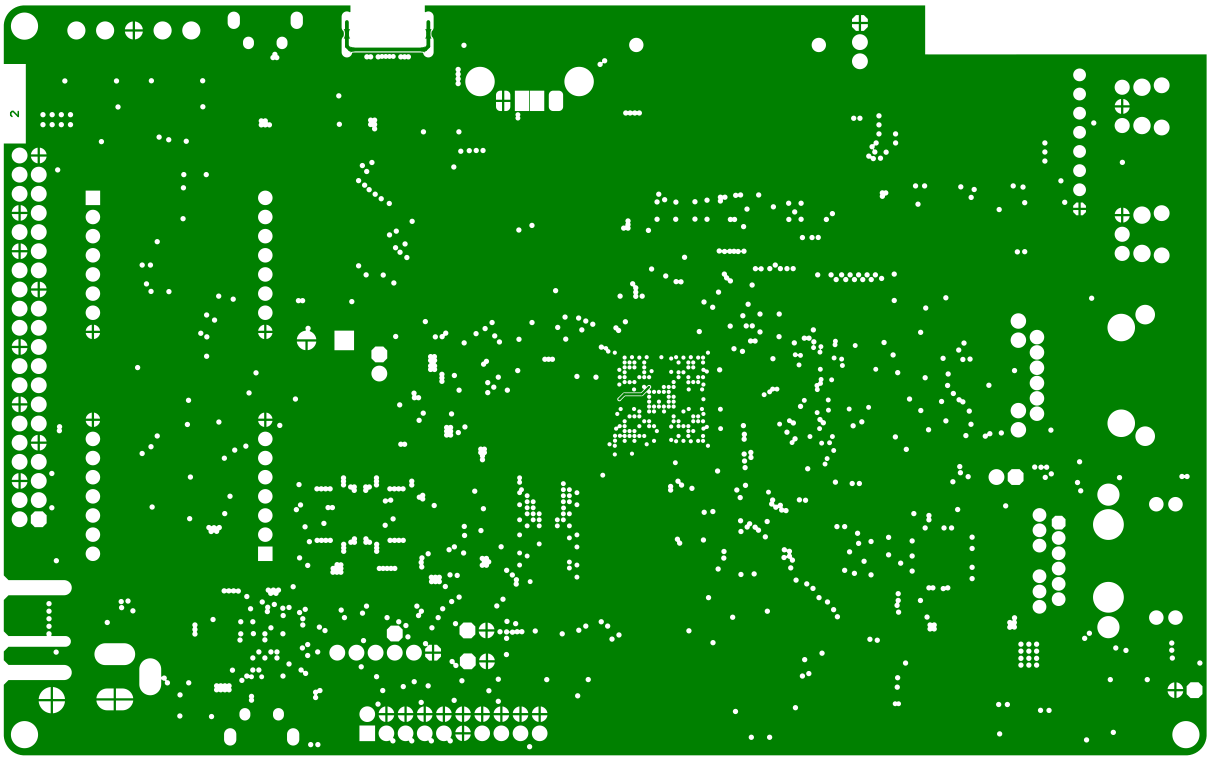


Figure 3-2. Incorrect GND Plane

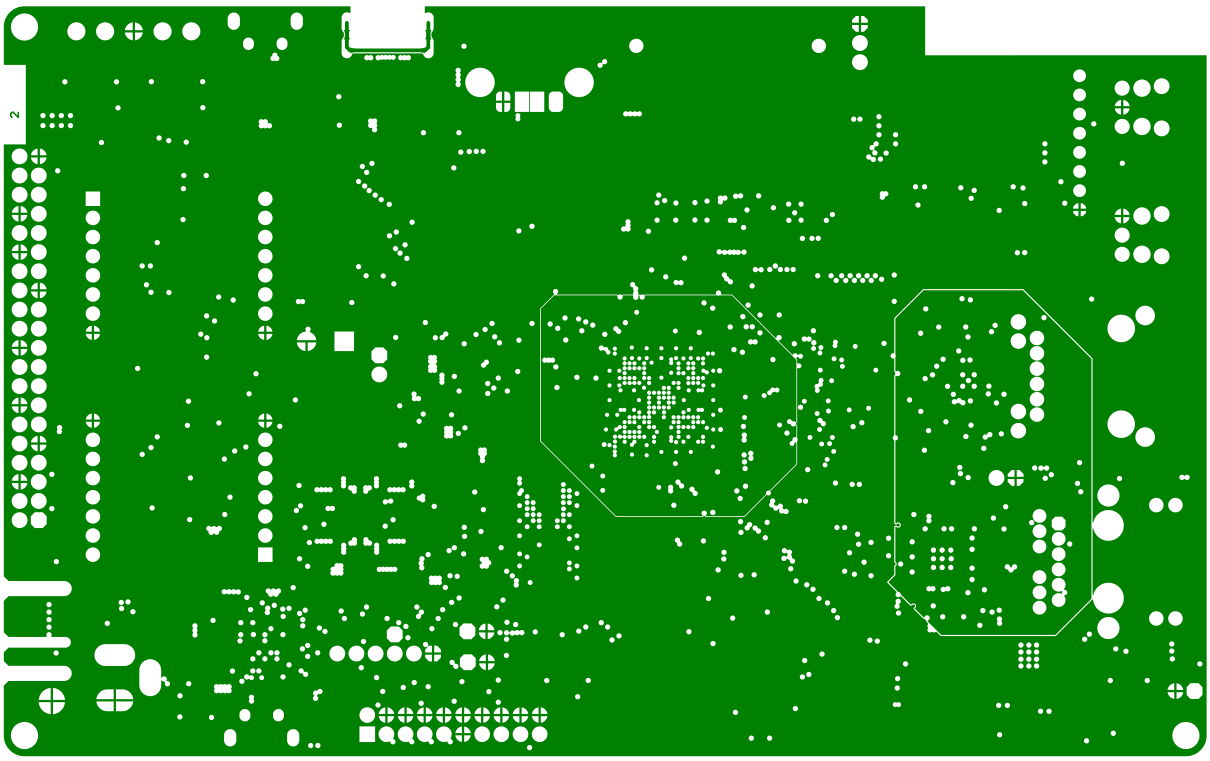


Figure 3-3. GND Plane Split Exception

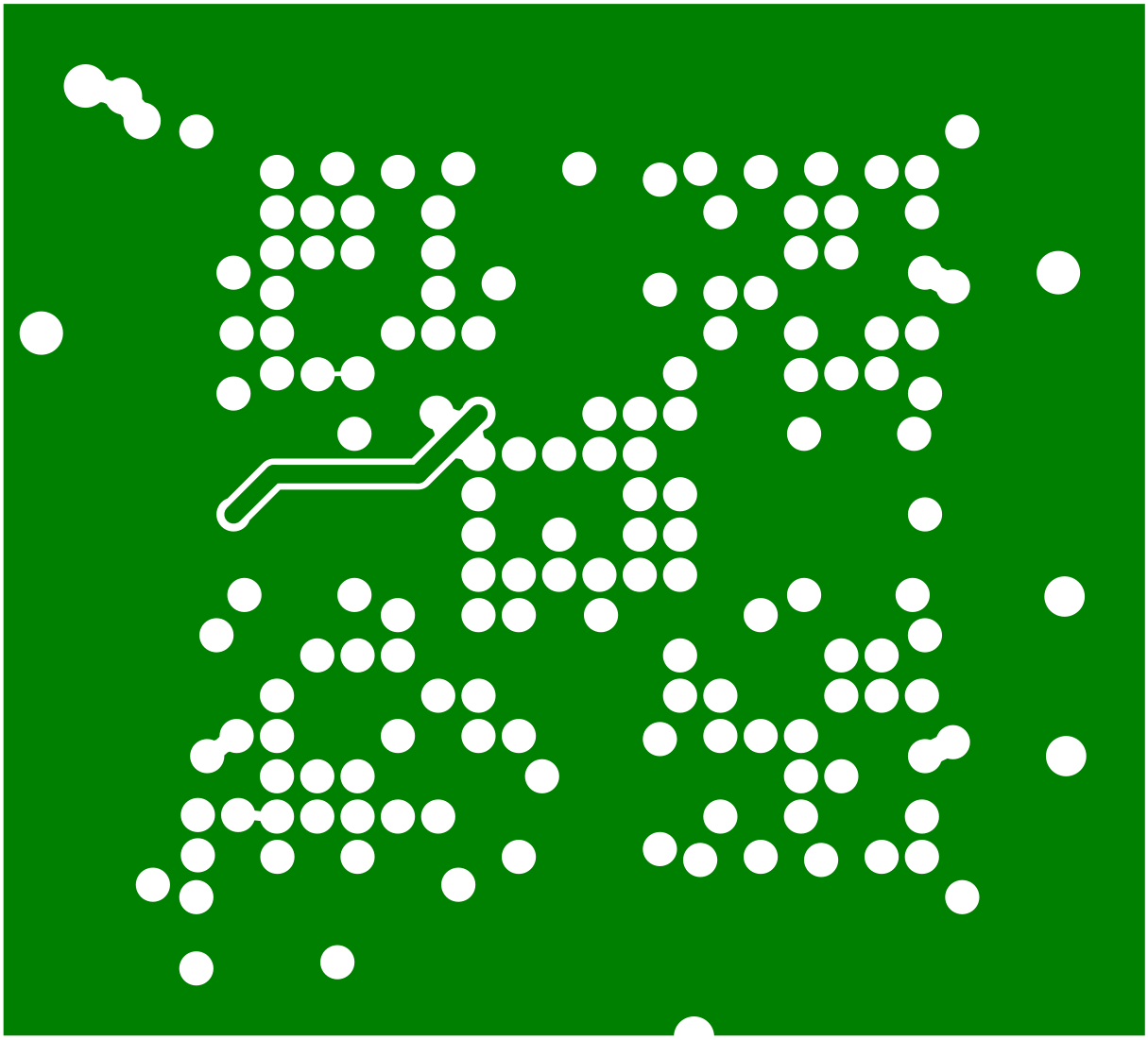


Figure 3-1 depicts a solid/uninterrupted GND plane that stretches all over the board. This is the ideal implementation.

Figure 3-2 shows several cut-outs assigned to a different power supply.

Such arrangement is to be avoided by all means, as it is a proven source of ElectroMagnetic Interference (EMI), therefore prone to failing the EMC compliance tests.

Very small unavoidable plane splits, like the one depicted in Figure 3-3, are permitted if the signals passing the split on an adjacent layer are low speed.

3.2 Define a Layer Stack-up so that Line Impedances are Matched to Driver Impedances

3.2.1 Requirements

Match the PCB line impedances to their corresponding driver impedances to reduce line reflections:

- Single-ended lines should have a 50 Ω +/-10% single-ended impedance.
- USB lines should have a 90 Ω +/-15% differential impedance.

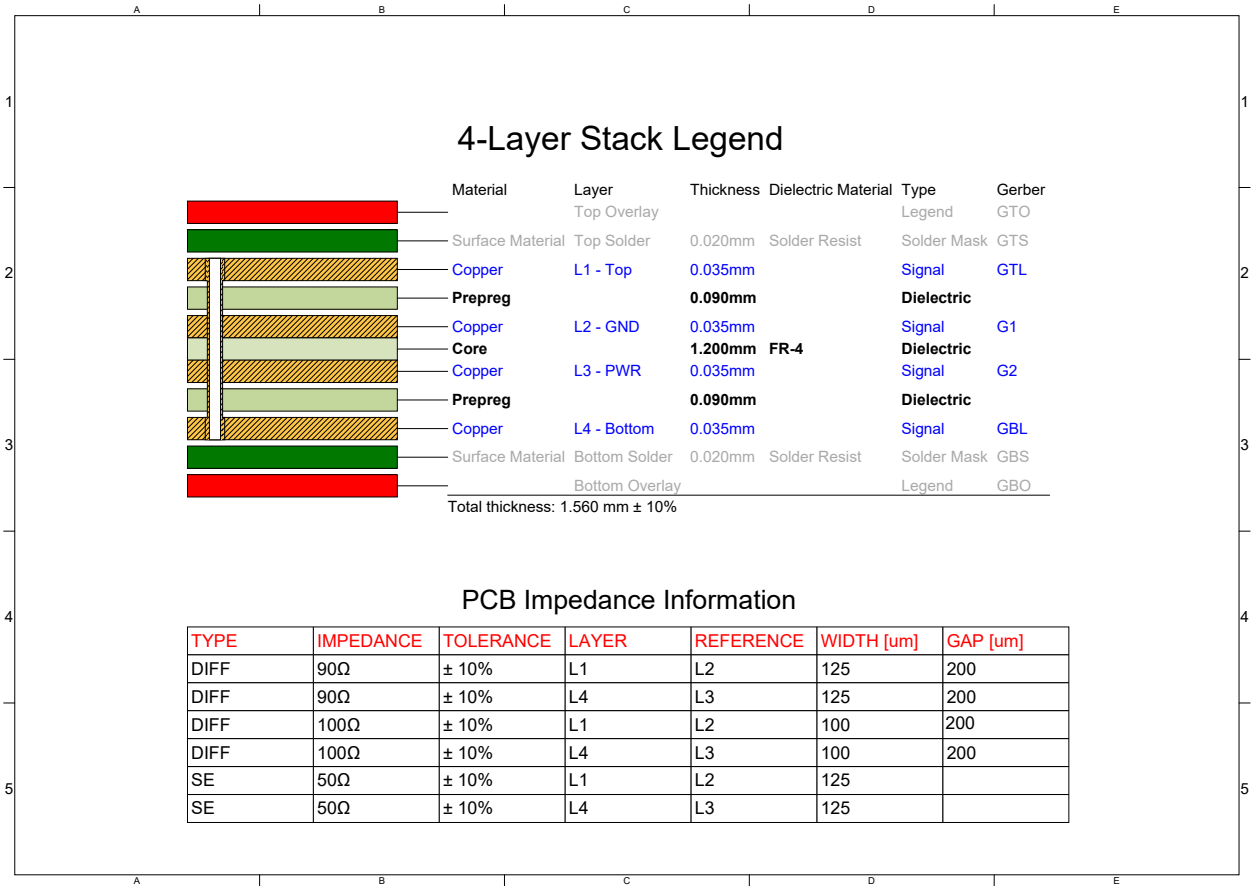
- DDR CLOCK and STROBE lines should have a 100 Ω +/-10% differential impedance.
- Ethernet RX and TX differential lines should have a 100 Ω +/-10% differential impedance.
- MIPI CLOCK and DATA lines should have a 100 Ω +/-10% differential impedance.

3.2.2 Implementation Example

The SAMA7G54 MPU is available in a single 14x14 mm², 0.65 mm pitch, 343-ball TFBGA package, optimized for standard class PCB layout (down to four layers).

To achieve the best performance, we recommend using the following layer stack-ups and line width and clearances.

Figure 3-4. 4-Layer Stack-up

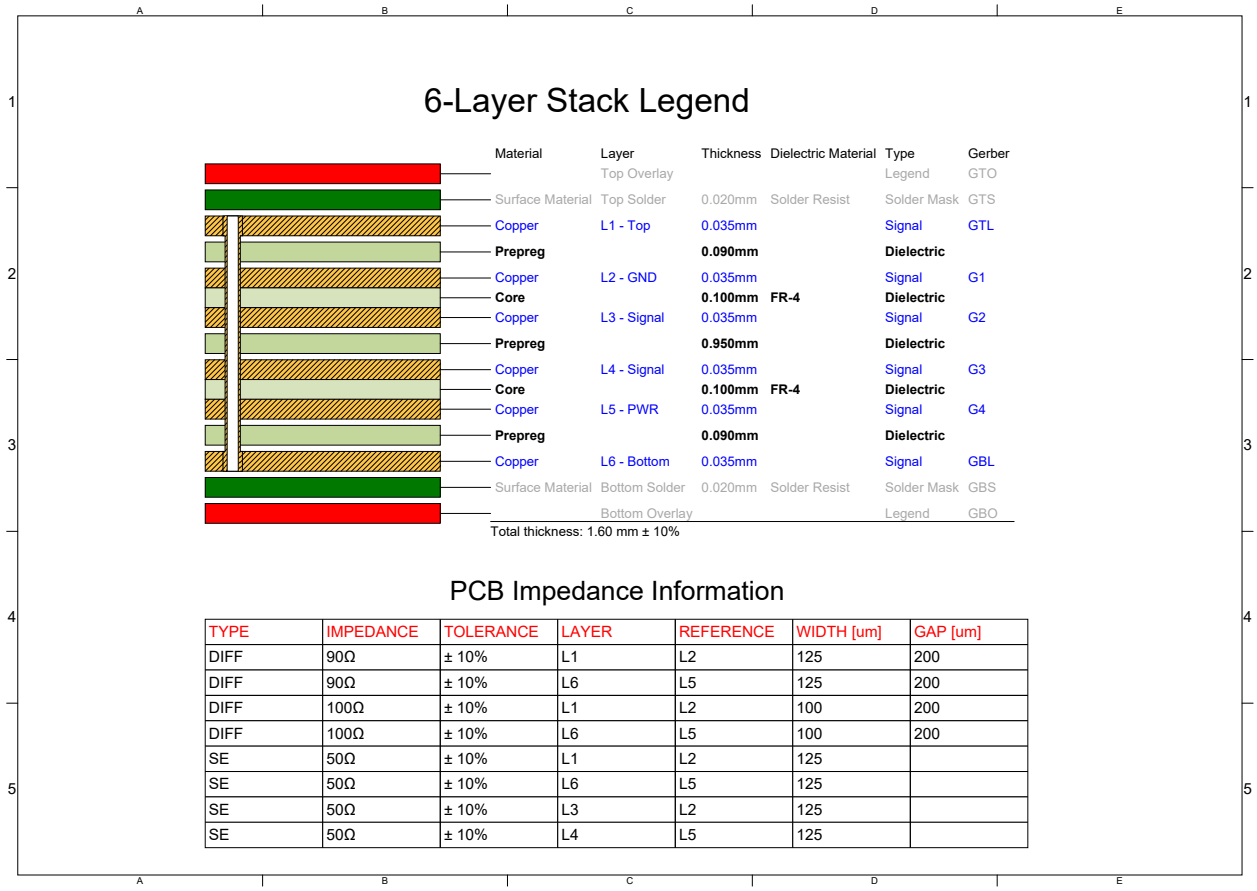


PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L4	L3	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L4	L3	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L4	L3	125	

More complex designs using the SAMA7G54 MPU can be implemented on a PCB with a stack-up of six layers.

Figure 3-5. 6-Layer Stack-up



PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L6	L5	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L6	L5	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L6	L5	125	
SE	50Ω	± 10%	L3	L2	125	
SE	50Ω	± 10%	L4	L5	125	

If the required line characteristic impedance values are met, similar eight-layer (or more) stack-ups can be used.

These stack-ups were chosen because they can provide all the required impedances by using minimum 100 µm-wide traces.

The minimum trace width is 100 µm (~4 mil) which is relatively standard nowadays for PCB manufacturers. This also ensures that the routing does not take much space on the board.

3.2.3 Extra Tips

Important: Make sure that your PCB manufacturer can produce that specific stack-up.

The PCB manufacturer may not have the required materials in stock, and have to order it specifically, which can increase the overall production cost.

Also, the manufacturer can recommend a different layer stack-up that they can produce cheaper with the materials in stock.

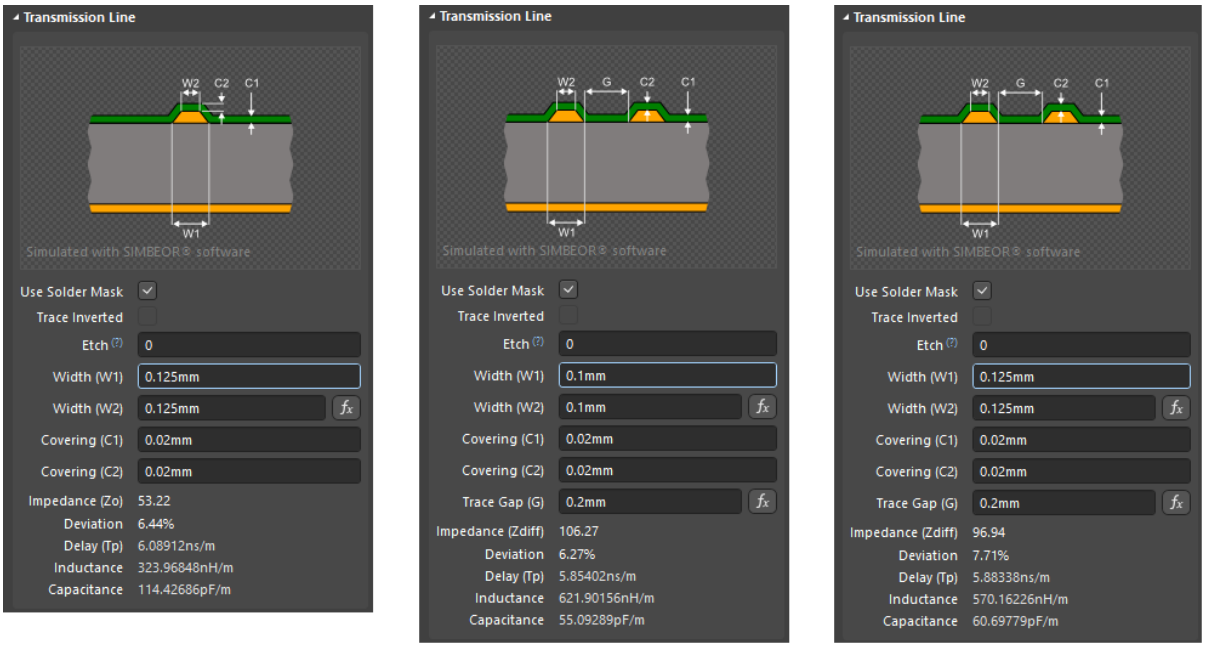
In such cases, you can easily adapt your layout to the proposed stack-up by changing the width of the traces so the required impedances are preserved. With the help of an impedance calculator tool, make sure that the recommendations previously given can still be respected (for example, check that enlarging the traces will satisfy the impedance while not infringing the minimal spacing).

Designing proper transmission lines is easier nowadays with the help of impedance calculators available on the market.

The following example shows the Altium Designer impedance calculator.

Here, after defining the PCB stack-up, you can either use the software to compute the ideal trace width that will yield a specific impedance, or input the trace width so that the tool calculates the resulting impedance.

Figure 3-6. Impedance Calculation



The SAMA7G54-EK was designed on a four-layer PCB so that the final thickness of the board should be 1.6 mm. Designs which require a different board thickness can be obtained only by modifying the central dielectric height. This does not impact the previously calculated trace impedances.

3.3 Place Decoupling Capacitors as Close as Possible to IC Pins

3.3.1 Requirements

Low-impedance decoupling of the device power supply inputs must be provided. 100 nF ceramic X7R (or X5R) capacitors placed very close to each power supply input is a minimum requirement.

3.3.2 Implementation Example

The SAMA7G54 BGA343 MPU is a depopulated 21x21 ball grid array. The selective ball depopulation allows the MPU to be routed on a four-layer PCB, using only two layers for signal routing. The depopulation also facilitates decoupling capacitors placement near the power inputs. Use 0201 sized decoupling capacitors and 0402 sized bulk capacitors.

In Figure 3-7, capacitors are the green rectangles.

The power is supplied through solid copper polygons placed on the inner layer (power layer). These polygons are formed in such a way that the high-speed signals on the bottom layer have their return path through them.

Figure 3-7. SAMA7G54 BGA343 Capacitor Placement

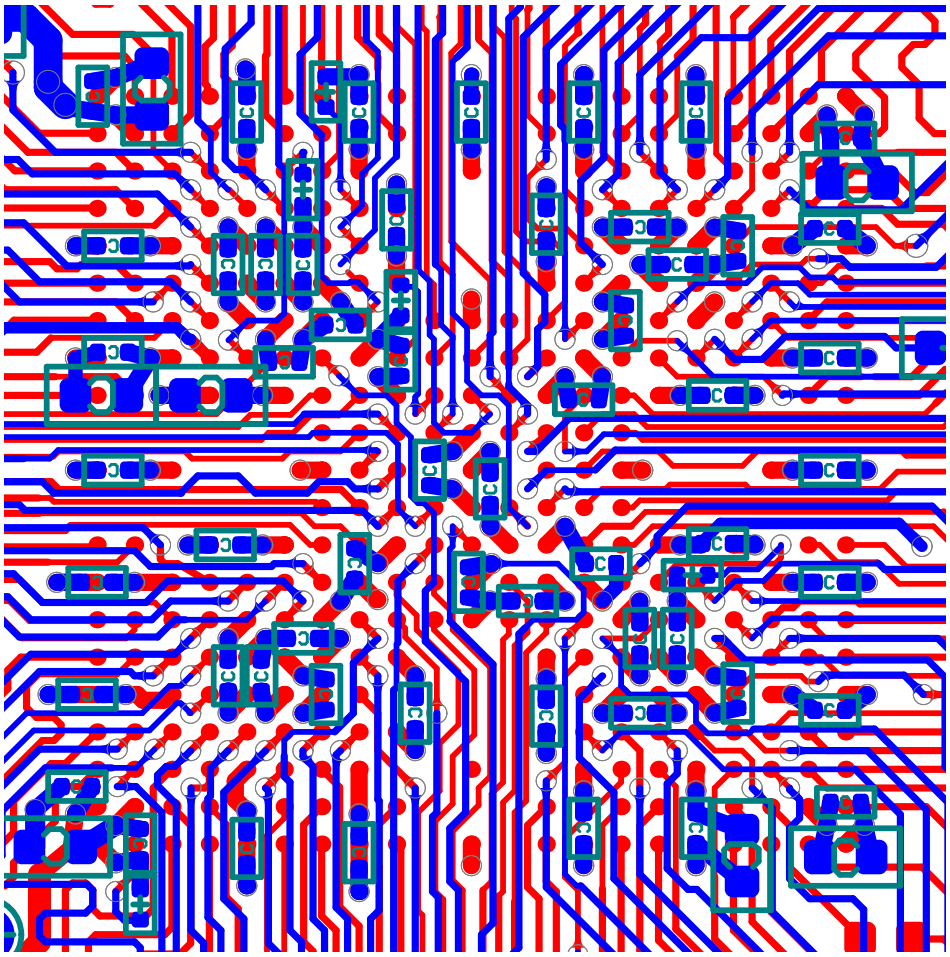
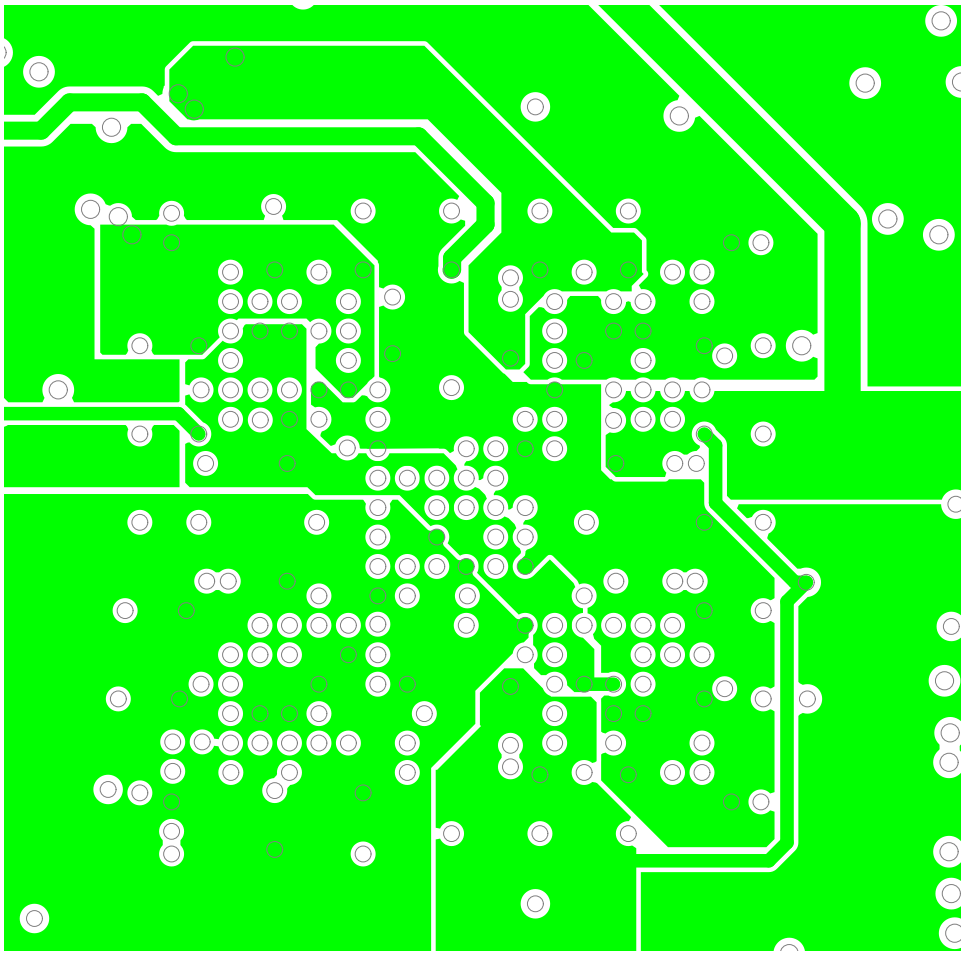


Figure 3-8. SAMA7G54 BGA343 Power Planes



3.4 Length-Match High-Speed Signals

3.4.1 Requirements

High-speed signals must be length-matched and routed over an uninterrupted reference plane (power or ground).

3.4.2 Implementation Example for DDR3L

Figure 3-9. DDR3L Address and Control

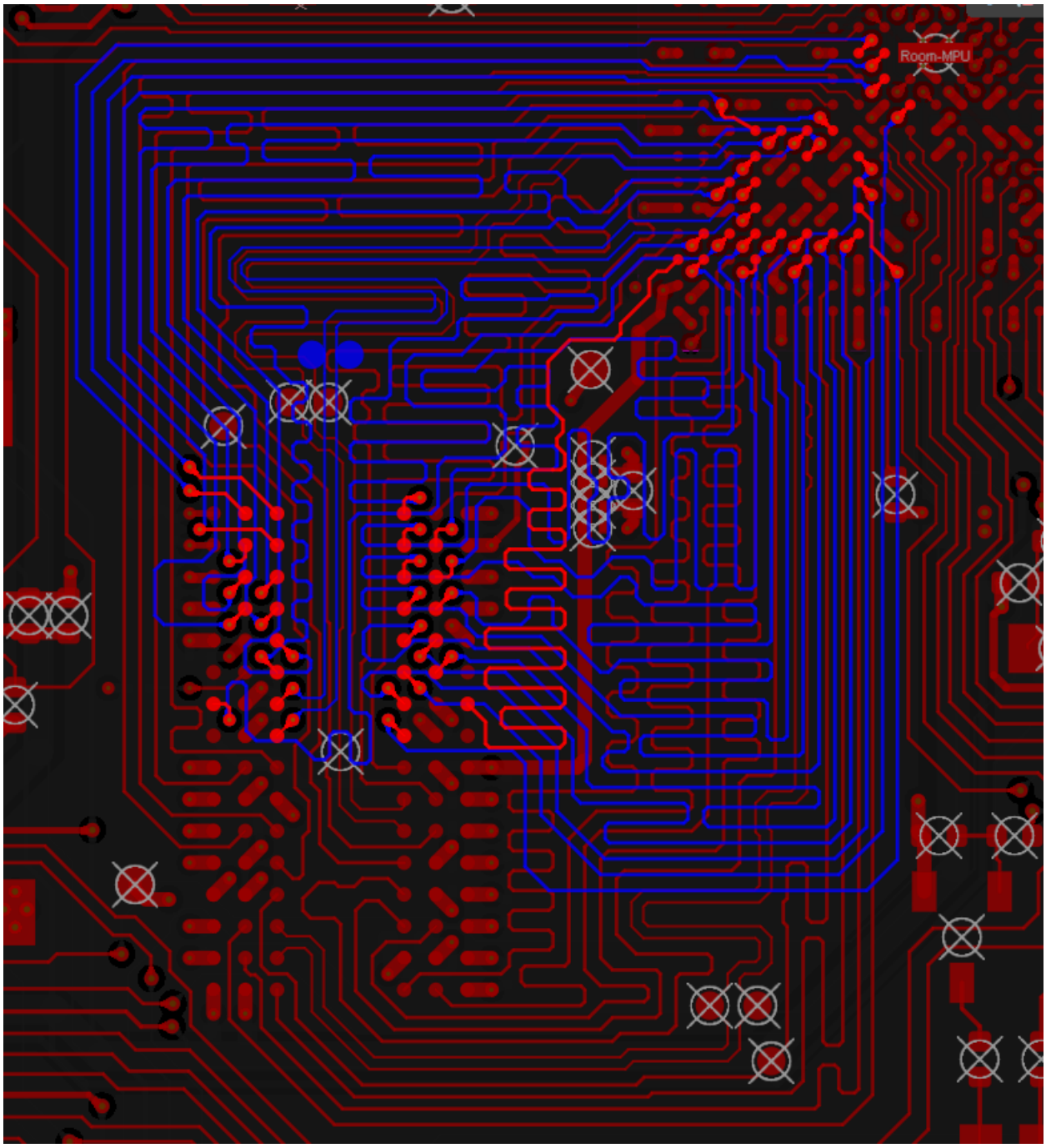
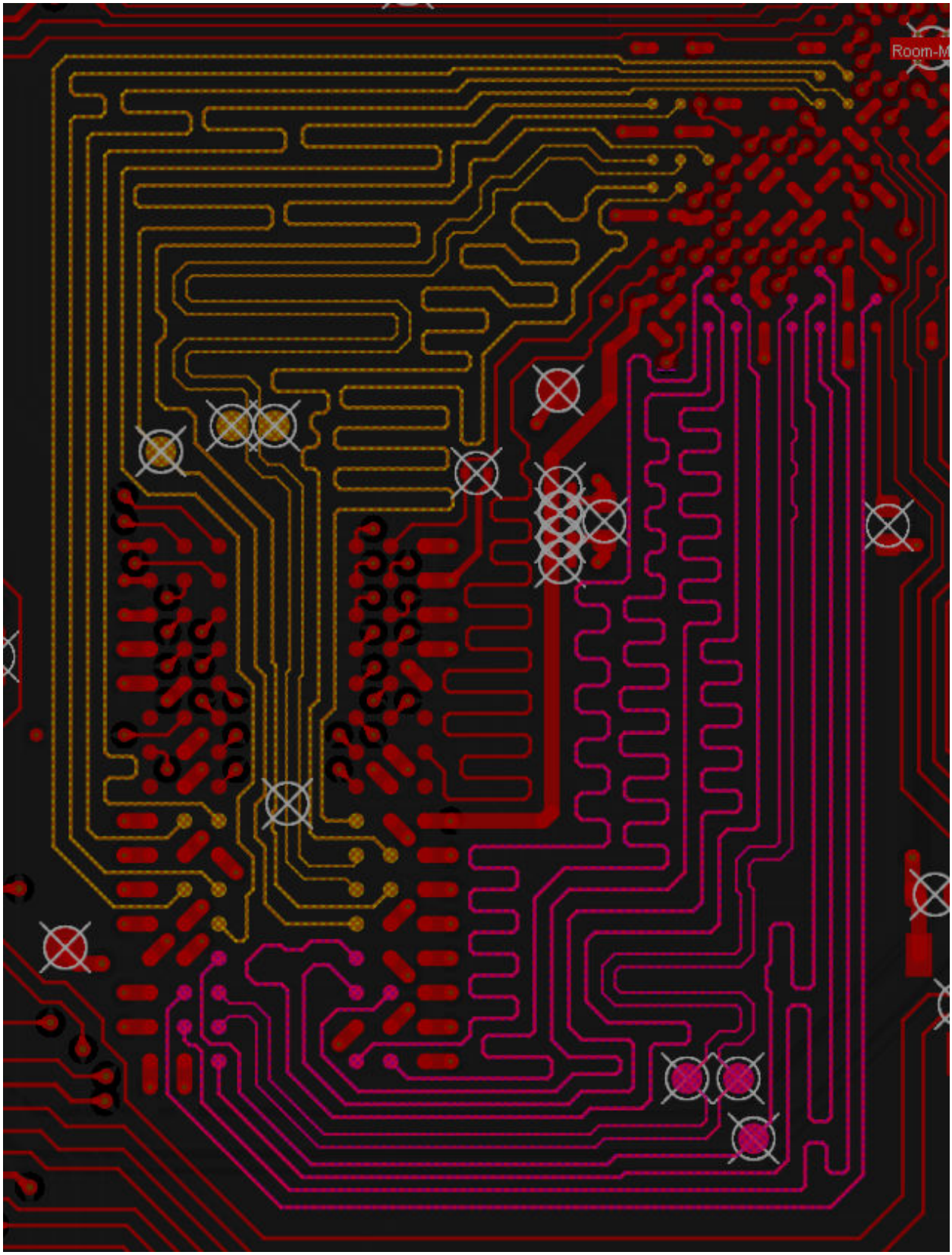


Figure 3-10. DDR3L Data Lanes



When routing a 16-bit bus width DRAM interface, it is recommended to use 16-bit memory devices. The single memory device should be routed in a simple point-to-point topology.

Traces belonging to the address, command and control group should be length-matched within this group.

Traces from each data byte lane should also be matched within its own lane.

It is also good practice to route data signals that belong to the same byte lane on the same layer. Figure 3-10 shows the signal routing of data byte lanes 0 and 1. For the address/command/control signals bus in Figure 3-9, the routing constraints can be more relaxed and the routing can be made on any available signal layer.

It is recommended to route the DRAM clock and DQS differential signals on the top and bottom layers, or on the same layer as the other signals from the same group.

When routing the MIPI signals, a maximum of 0.15 mm length mismatch is allowed within the differential pair and a maximum of 1.5 mm length mismatch is allowed between differential pairs.

It is recommended to match any group of high-speed signals as tightly as possible.

3.5 Manufacturing Constraints

3.5.1 Requirements

The PCB manufacturer should meet or exceed the following capabilities:

- 0.35 mm via diameter
- 0.15 mm via drill
- 0.1 mm trace clearance on any layer
- 0.1 mm trace width on any layer

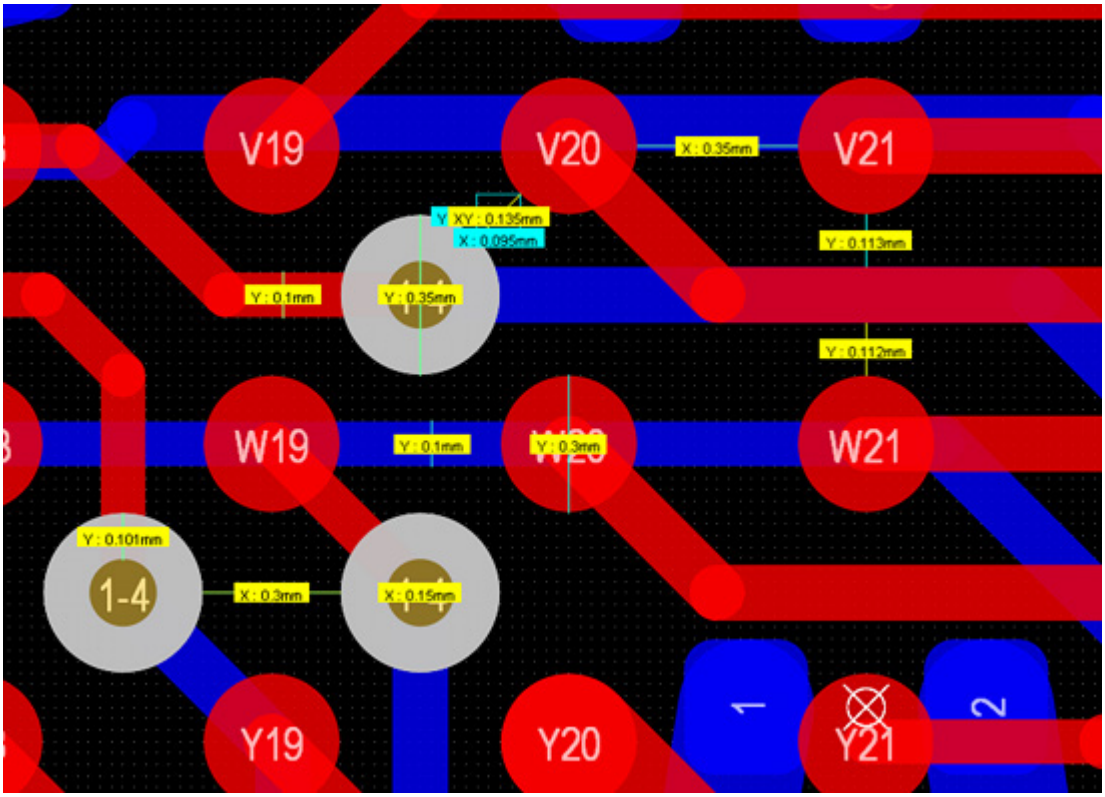
3.5.2 Implementation Example

The following figure shows a section of signal routing inside the MPU footprint, with visible dimensions for traces and vias.

Vias should be centered between the adjacent pads to maintain a consistent clearance.

Traces on top and bottom should also be routed at the midpoint between pads and vias.

Figure 3-11. Via and Trace Routing Example



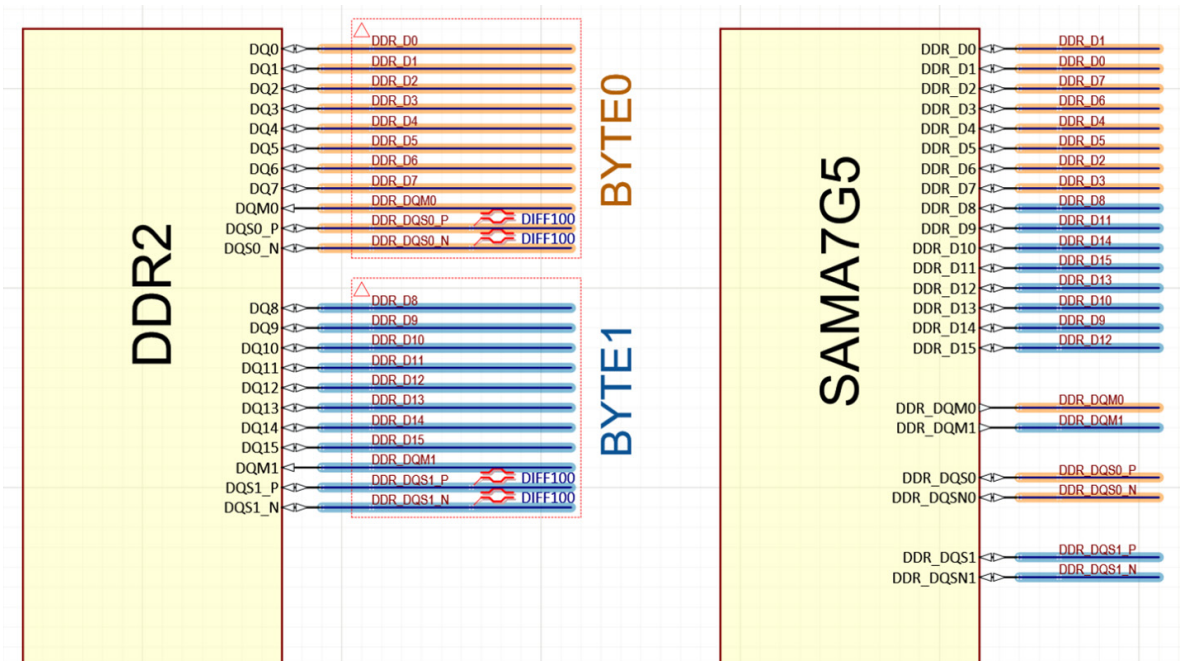
4. Appendix

4.1 Bit and Byte Swapping

DDR2 memories support **bit swapping**, a technique the designer can use to interchange data lines with one another, provided that they correspond to the same byte lane (for example, any bits inside the D[0..7] lane). This is very useful when trying to optimize a DDR layout routing. The SAMA7G54 BGA343 MPU pinout is specifically optimized to match the pinout of DDR3L memory devices, therefore bit or byte swapping may not be needed for DDR3L, but useful for DDR2. LPDDR2 and LPDDR3 devices do not support bit and byte swapping.

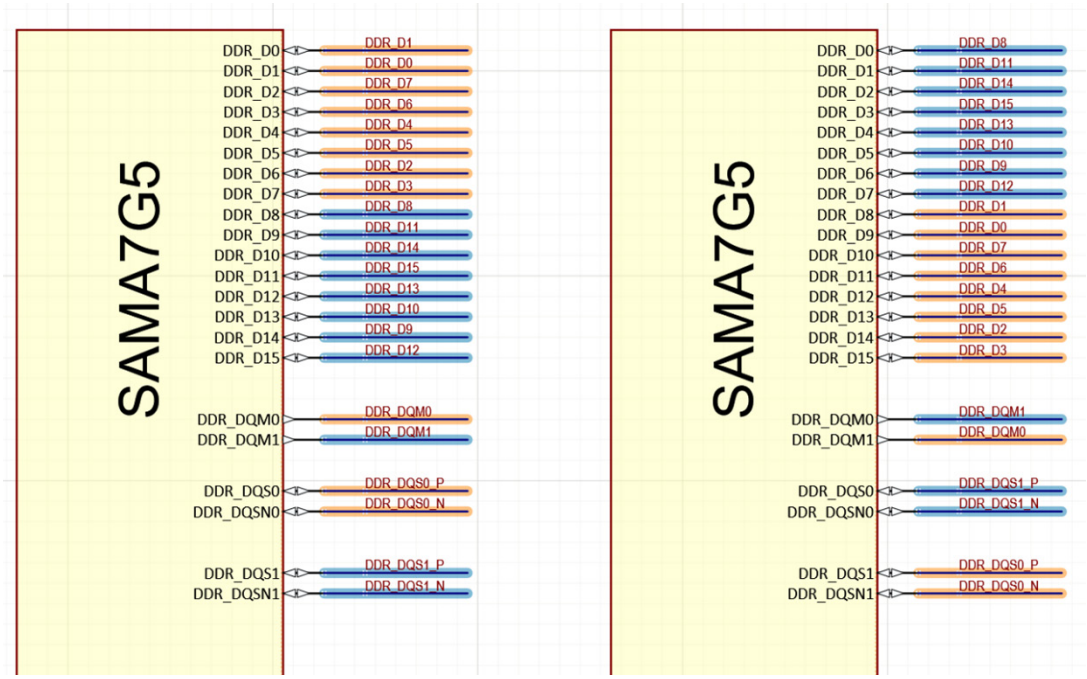
The following figure shows an example of the bit swapping technique which can be implemented in a SAMA7G54 board design.

Figure 4-1. DDR2 Bit Swapping



Byte swapping is another technique that can be used on DDR2 memories. It allows the designer to swap the data lanes with one another, also for the purpose of optimizing the layout. Remember to also swap the DQMx and DQSx signals corresponding to the swapped byte lanes, as illustrated below.

Figure 4-2. DDR2 Byte Swapping



4.2 Good Practices

The following is a list of suggestions for designing with high-speed signals:

- Use controlled impedance PCB traces that match the specified single-ended (50Ω) and differential (100Ω) impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing required to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs, any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- Route CMOS/TTL and differential signals on different layers, which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Use a minimum of 20 mils spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

- Route all traces over continuous planes (VCC or GND), avoiding cross splits or openings in those planes.
- For microstrip or stripline transmission lines, keep the spacing between adjacent signal paths at least twice the line width.
- Keep all traces at least five line widths away from the edge of the board.
- Follow the return path of each signal and keep the width of the return path under each signal path at least as wide, and preferably at least three times as wide, as the signal trace.
- To avoid EMIs, avoid routing switching signals across splits or openings in ground planes. Routing around them is preferable even if it results in longer paths.
- Minimize the loop inductance between the power and ground paths.
- Allocate power and ground planes on adjacent layers with as thin a dielectric as possible to create plane capacitance.
- Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
- Supply voltages must be composed of planes only, not traces. Short connections (≈ 8 mils) are commonly used to attach vias to planes. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance (20 mils trace width).

5. Revision History

5.1 Rev. A - 06/2022

First issue.

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