

KSZ8051 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the KSZ8051 family of devices, which includes the following:

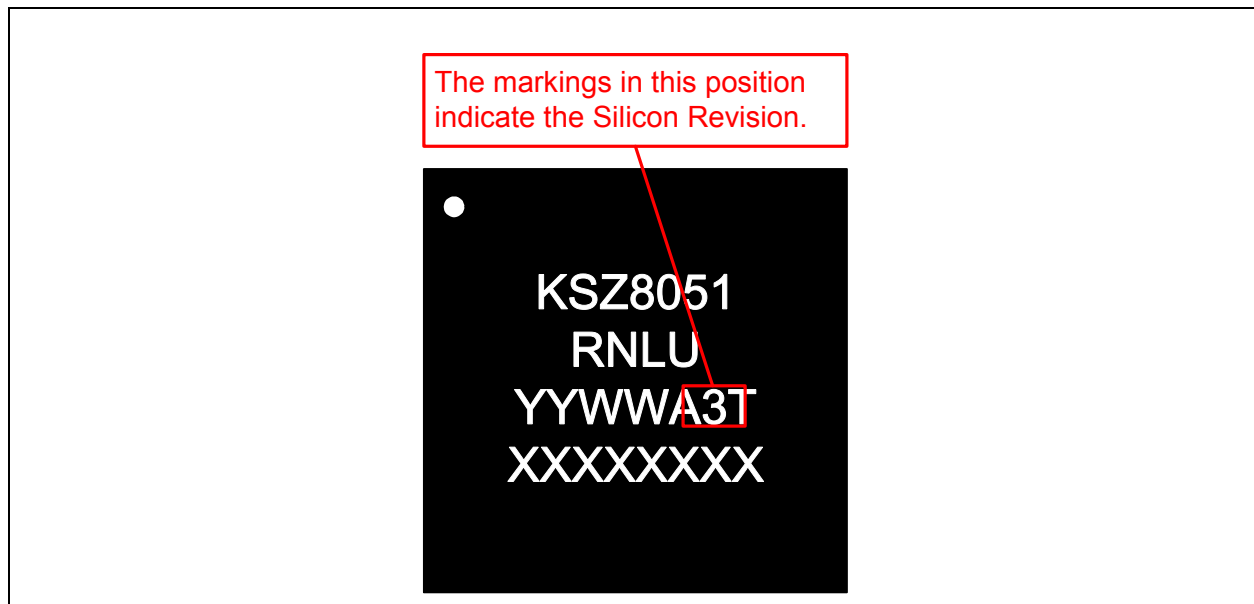
- KSZ8051RNLU (Rev. A)

The silicon errata discussed in this document are for silicon with silicon revisions as listed in [Table 1](#). The silicon revision can be determined by the device's top marking as indicated in [Figure 1](#), or by reading device register 3h bits [3:0] (0x0 for silicon revision A, 0x1 for silicon revision A3). A summary of KSZ8051 silicon errata is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ8051RNLU	A

FIGURE 1: TOP MARKING SILICON REVISION INDICATION



Note: The purpose of [Figure 1](#) is to detail the top markings of an example part and highlight the location of the silicon revision. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	Random RMII transmitter errors can occur in RMII 25MHz clock mode	A (KSZ8051RNLU)

KSZ8051

Silicon Errata Issues

Module 1: Random RMII transmitter errors can occur in RMII 25MHz clock mode

DESCRIPTION

RMII transmit errors can occur internal to the PHY on a minority of A devices. This is due to the internal data clock edges being aligned with the external 25MHz RMII clock. When these two clocks are aligned, the data is not sampled properly into the transmit buffer.

Silicon revision A3 locks the 25/50MHz clock phase at the RMII transmit FIFO to correct this issue.

END USER IMPLICATIONS

When the failure occurs, transmit traffic errors will occur on the line interface. Excessive transit errors will cause multiple data packet re-transmissions at the TCP layer. A customer may observe this as reduced bandwidth in their communication. The physical link will remain operational.

Work Arounds

Microchip recommends that all customers use revision A3 to avoid this issue. For existing designs that cannot change, there are three possible work arounds. In priority order, these are:

Software work around 1:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, toggle register 0h bit [11] from “0” to “1” and back to “0” to configure the PHY to power-down and then power-up. Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be used for normal operation.

Software work around 2:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, set the internal REFCLK register 19h bits [15:12] from their default value of 0x7 to 0x15 (+0.6ns) or 0x00 (-0.6ns) to adjust the REFCLK pad skew. Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be used for normal operation.

Software work around 3:

1. Set register 0h to 0x6100 to enable local digital loopback after power up.
2. Send packets from the processor (MAC) and verify if all packets are looped back without error.
3. If any error occurs during loopback, set register 11h bit [15] to “1” to enable I/O drive current strength adjustment. Set the drive current strength via register 11h bits [14:13] (00=8mA, 01=4mA, 10=14mA, 11=10mA). Repeat step 2.
4. If no error occurs during loopback, set register 0h to the default or desired value. The device can now be used for normal operation.

Manual work around:

If traffic errors occur power-down PHY and then power-up.

PLAN

This erratum has been corrected in silicon revision A3 (KSZ8051RNLUB).

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000710A (09-0616)	All	Initial release

KSZ8051

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