MD1712

High-Speed Integrated Ultrasound Driver IC

Features

- Drives Two Ultrasound Transducer Channels
- Generates a Five-level Waveform
- Drives 12 High-voltage MOSFETs
- ±2A Source and Sink Peak Currents
- Up to 20 MHz Output Frequency
- 12 V/ns Slew Rate
- ±3 ns Matched Delay Times
- Less than –40 dB Second Harmonic
- Two Separate Gate Drive Voltages
- 1.8V to 3.3V CMOS Logic Interface

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-Destructive Testing (NDT)
- Metal Flaw Detection
- Sonar Transmitter

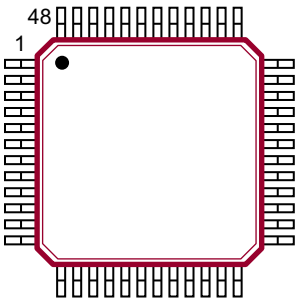
General Description

The MD1712 is a 2-channel, five-level, high-voltage, and high-speed transmitter driver IC. It is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, NDT, and driving piezoelectric transducers.

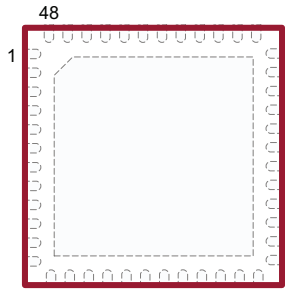
The MD1712 is a two-channel logic controller circuit with low-impedance MOSFET gate drivers. There are two sets of control logic inputs—one for Channel A and one for Channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of the TC6320. The MD1712 drives six TC6320s. Each pair consists of an N-channel and a P-channel MOSFET. They are designed to have the same impedance and can provide peak currents of over 2 amps.

Package Types

48-lead LQFP
(Top view)

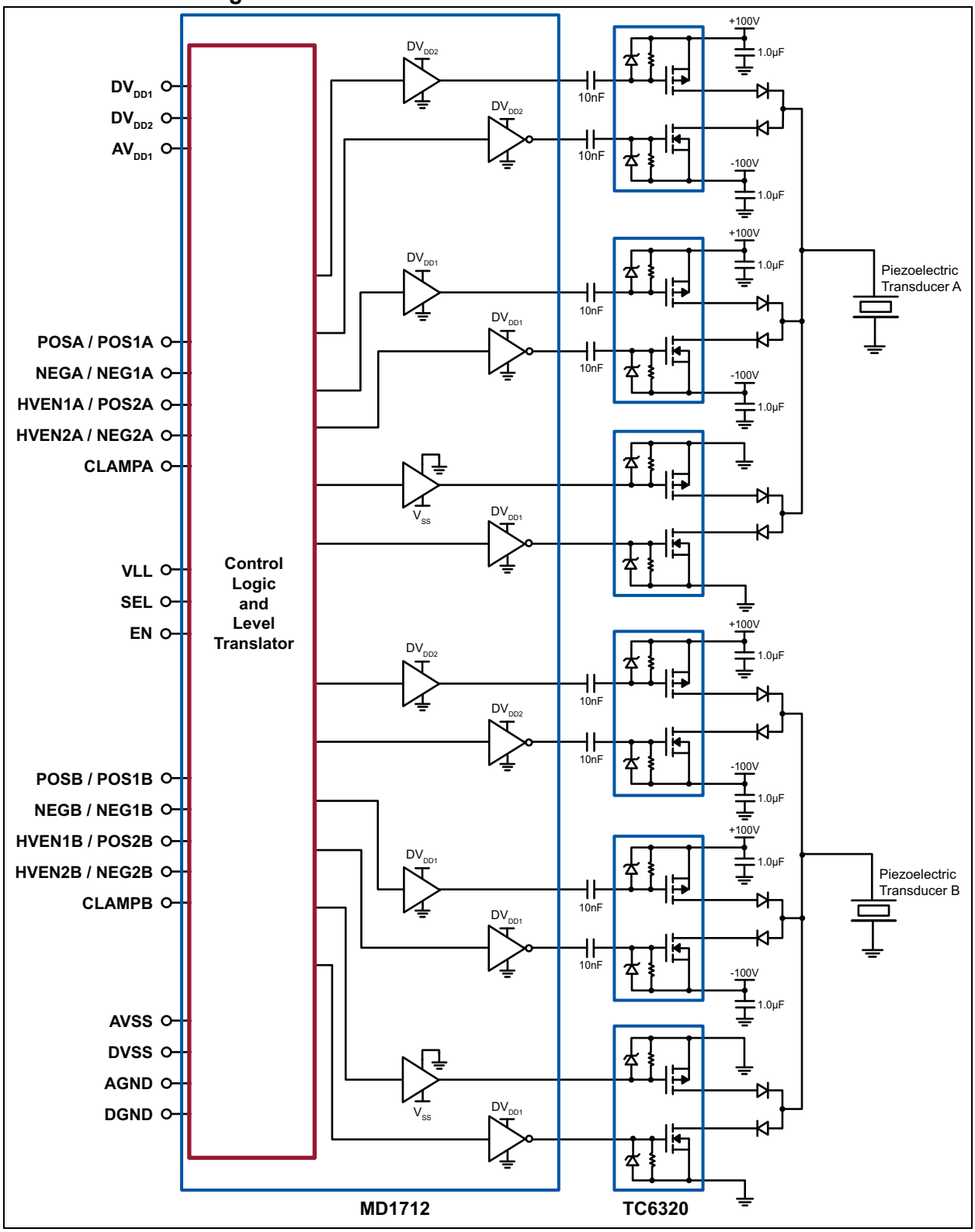


48-lead VQFN
(Top view)

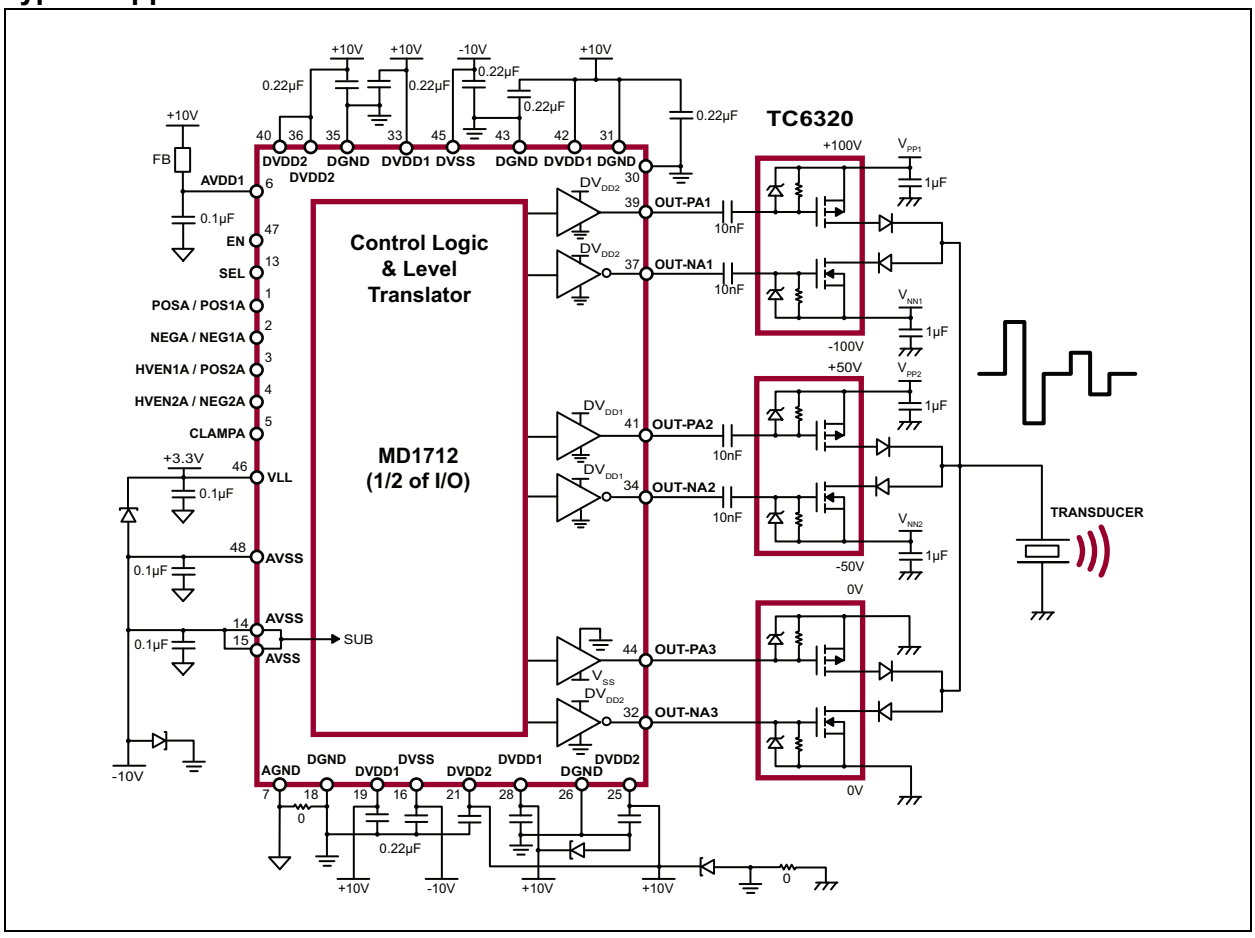


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage, V_{LL} ..... –0.5V to +5.5V
Positive Gate Drive Supply, AV_{DD1}, DV_{DD1}, DV_{DD2} ..... –0.5V to +15V
Negative Gate Drive Supply, AV_{SS}, DV_{SS} ..... –15V to +0.5V
Operating Junction Temperature, T_J ..... 0°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Power Dissipation:
48-lead LQFP 1.2W
48-lead VQFN 1.2W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATING SUPPLY VOLTAGES AND CURRENTS

Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = –10V$, $V_{LL} = 3.3V$, $T_A = 25°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply	V_{LL}	1.8	3.3	5	V	
Positive Drive Bias Supply	AV_{DD1}	8	10	12.6	V	
Positive Gate Drive Supply	DV_{DD1}	4.75	—	12.6	V	
Positive Gate Drive Supply	DV_{DD2}	4.75	—	12.6	V	
Negative Gate Drive and Bias Supply	AV_{SS}, DV_{SS}	–12	–10	–8	V	
Logic Supply Current	I_{VLL}	—	2	—	mA	All channels on at 5 MHz, no load
Positive Bias Current	I_{AVDD1}	—	5	—	mA	
Negative Drive and Bias Supply Currents	I_{AVSS}, I_{DVSS}	—	20	—	mA	
Positive Drive Current 1	I_{DVDD1}	—	55	—	mA	
Positive Drive Current 2	I_{DVDD2}	—	13	—	mA	All channels on at 5 MHz, $DV_{DD2} = 5$, no load
V_{AVDD1} Quiescent Current	I_{AVDD1Q}	—	2	—	mA	EN = low, all inputs low or high
V_{AVSS} Quiescent Current	I_{AVSSQ}	—	0.75	—	mA	
V_{DVDD1} Quiescent Current	I_{DVDD1Q}	—	—	10	µA	
V_{DVDD2} Quiescent Current	I_{DVDD2Q}	—	—	10	µA	
Logic Supply Current	I_{VLLQ}	—	1	—	mA	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = –10V$, $V_{LL} = 3.3V$, $T_A = 0°C$ to $70°C$.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
P-CHANNEL AND N-CHANNEL GATE DRIVER OUTPUTS							
Output Sink Resistance	P-Channel	R_{SINK}	—	—	6	Ω	I_{SINK} = 100 mA
	N-Channel		—	—	10	Ω	I_{SINK} = 100 mA
Output Source Resistance	P-Channel	R_{SOURCE}	—	—	6	Ω	I_{SOURCE} = 100 mA
	N-Channel		—	—	10	Ω	I_{SOURCE} = 100 mA
Peak Output Sink Current	P-Channel	I_{SINK}	—	2	—	A	
	N-Channel		—	1.5	—	A	
Peak Output Source Current	P-Channel	I_{SOURCE}	—	2	—	A	
	N-Channel		—	1.5	—	A	
LOGIC INPUTS							
Input Logic High Voltage		V_{IH}	0.8 V_{LL}	—	V_{LL}	V	
Input Logic Low Voltage		V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Current		I_{IH}	—	—	1	µA	
Input Logic Low Current		I_{IL}	–1	—	—	µA	

AC ELECTRICAL CHARACTERISTICS

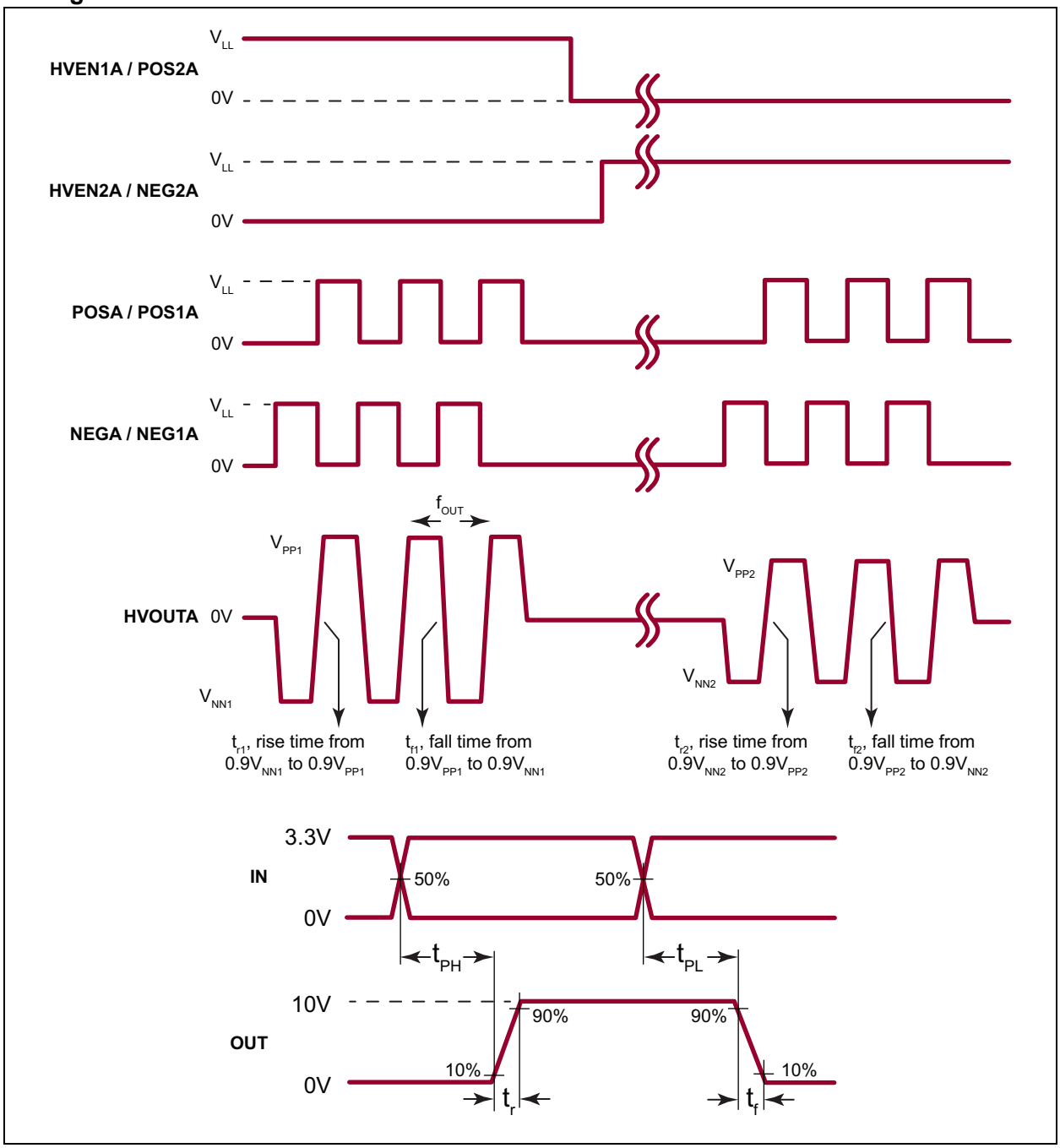
Electrical Specifications: Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = –10V$, $V_{LL} = 3.3V$, $T_A = 0°C$ to $70°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Frequency Range	f_{OUT}	—	—	20	MHz	
Propagation Delay when Output is from Low to High	t_{PH}	—	19	—	ns	No load (See **Timing Waveforms**.)
Propagation Delay when Output is from High to Low	t_{PL}	—	19	—	ns	No load (See **Timing Waveforms**.)
Output Rise Time	t_r	—	8	—	ns	1000 pF load (See **Timing Waveforms**.)
Output Fall Time	t_f	—	8	—	ns	1000 pF load (See **Timing Waveforms**.)
Delay Time Matching	Δt_{DM}	—	—	±3	ns	No load, from device to device
Output Jitter	Δt_{DLAY}	—	30	—	ps	Standard deviation of t_D samples (1 kHz)
Output Slew Rate	SR	—	12	—	V/ns	Measured at TC6320 output with 100Ω load
Second Harmonic Distortion	HD2	—	–40	—	dB	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	0	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
48-lead LQFP	θ_{JA}	—	52	—	°C/W	
48-Lead VQFN	θ_{JA}	—	23	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of MD1712 are listed in Table 2-1. See **Package Types** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	POSA/POS1A	Logic input control for Channel A. When SEL = L, the pin is POSA. When SEL = H, the pin is POS1A.
2	NEGA/NEG1A	Logic input control for Channel A. When SEL = L, the pin is NEGA. When SEL = H, the pin is NEG1A.
3	HVEN1A/POS2A	Logic input control for Channel A. When SEL = L, the pin is HVEN1A. When SEL = H, the pin is POS2A.
4	HVEN2A/NEG2A	Logic input control for Channel A. When SEL = L, the pin is HVEN2A. When SEL = H, the pin is NEG2A.
5	CLAMPA	Used with SEL = H. Logic input control for OUT–PA3 and OUT–NA3. Connect to ground when SEL = L.
6	AVDD1	Supplies analog circuitry portion of the gate driver. Should be at the same potential as DVDD1.
7	AGND	Analog Ground
8	CLAMPB	Used with SEL = H. Logic input control for OUT–PB3 and OUT–NB3. Connect to ground when SEL = L.
9	HVEN2B/NEG2B	Logic input control for Channel B. When SEL = L, the pin is HVEN2B. When SEL = H, the pin is NEG2B.
10	HVEN1B/POS2B	Logic input control for Channel B. When SEL = L, the pin is HVEN1B. When SEL = H, the pin is POS2B.
11	NEGB/NEG1B	Logic input control for Channel B. When SEL = L, the pin is NEGB. When SEL = H, the pin is NEG1B.
12	POSB/POS1B	Logic input control for Channel B. When SEL = L, the pin is POSB. When SEL = H, the pin is POS1B.
13	SEL	Logic input select. See Table 3-2 for SEL = L and Table 3-3 for SEL = H.
14	AVSS	Negative driver supply for OUT–PA3, OUT–PB3, and bias circuits. They are also connected to the IC substrate. They are required to connect to the most negative potential of voltage supplies.
15		
16	DVSS	Gate drive supply voltage for OUT–PA3 and OUT–PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AVSS.
17	OUT–PB3	Output P-channel gate driver for Channel B
18	DGND	Digital Ground
19	DVDD1	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA2, OUT–NA2, OUT–NA3, OUT–PB2, OUT–NB2, and OUT–NB3. Should be at the same potential as AVDD1.
20	OUT–PB2	Output P-channel gate driver for Channel B
21	DVDD2	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA1, OUT–NA1, OUT–PB1, and OUT–NB1. Can be at a different potential than DVDD1.
22	OUT–PB1	Output P-channel gate driver for Channel B
23	NC	No connection
24	OUT–NB1	Output N-channel gate driver for Channel B

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
25	DVDD2	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA1, OUT–NA1, OUT–PB1, and OUT–NB1. Can be at a different potential than DVDD1.
26	DGND	Digital Ground
27	OUT–NB2	Output N-channel gate driver for Channel B
28	DVDD1	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA2, OUT–NA2, OUT–NA3, OUT–PB2, OUT–NB2, and OUT–NB3. Should be at the same potential as AVDD1.
29	OUT–NB3	Output N-channel gate driver for Channel B
30	DGND	Digital Ground
31	DVDD1	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA2, OUT–NA2, OUT–NA3, OUT–PB2, OUT–NB2, and OUT–NB3. Should be at the same potential as AVDD1.
32	OUT–NA3	Output N-channel gate drivers for Channel A
33	DVDD1	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA2, OUT–NA2, OUT–NA3, OUT–PB2, OUT–NB2, and OUT–NB3. Should be at the same potential as AVDD1.
34	OUT–NA2	Output N-Channel gate drivers for Channel A
35	DGND	Digital Ground
36	DVDD2	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA1, OUT–NA1, OUT–PB1, and OUT–NB1. Can be at a different potential than DVDD1.
37	OUT–NA1	Output N-channel gate drivers for Channel A
38	NC	No connection
39	OUT–PA1	Output P-channel gate drivers for Channel A
40	DVDD2	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA1, OUT–NA1, OUT–PB1, and OUT–NB1. Can be at a different potential than DVDD1.
41	OUT–PA2	Output P-channel gate drivers for Channel A
42	DVDD1	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT–PA2, OUT–NA2, OUT–NA3, OUT–PB2, OUT–NB2, and OUT–NB3. Should be at the same potential as AVDD1.
43	DGND	Digital Ground
44	OUT–PA3	Output P-channel gate drivers for Channel A
45	DVSS	Gate drive supply voltage for OUT–PA3 and OUT–PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AVSS.
46	VLL	Logic supply voltage
47	EN	Logic input enable control. When EN = L, all P-channel output drivers are high and all N-channel output drivers are low.
48	AVSS	Negative driver supply for OUT–PA3, OUT–PB3 and bias circuits. They are also connected to the IC substrate. They are required to connect to the most negative potential of voltage supplies.
Center Pad	AVSS	For the QFN package, the center pad is at AVSS potential. It should be externally connected to AVSS.

3.0 FUNCTIONAL DESCRIPTION

TABLE 3-1: POWER-UP SEQUENCE

Step	Connection	Description
1	AV_{SS}, DV_{SS}	Negative gate drive supply and substrate bias
2	V_{LL}, AV_{DD1}, DV_{DD1}, and DV_{DD2}	Logic supply, positive gate drive supply and bias

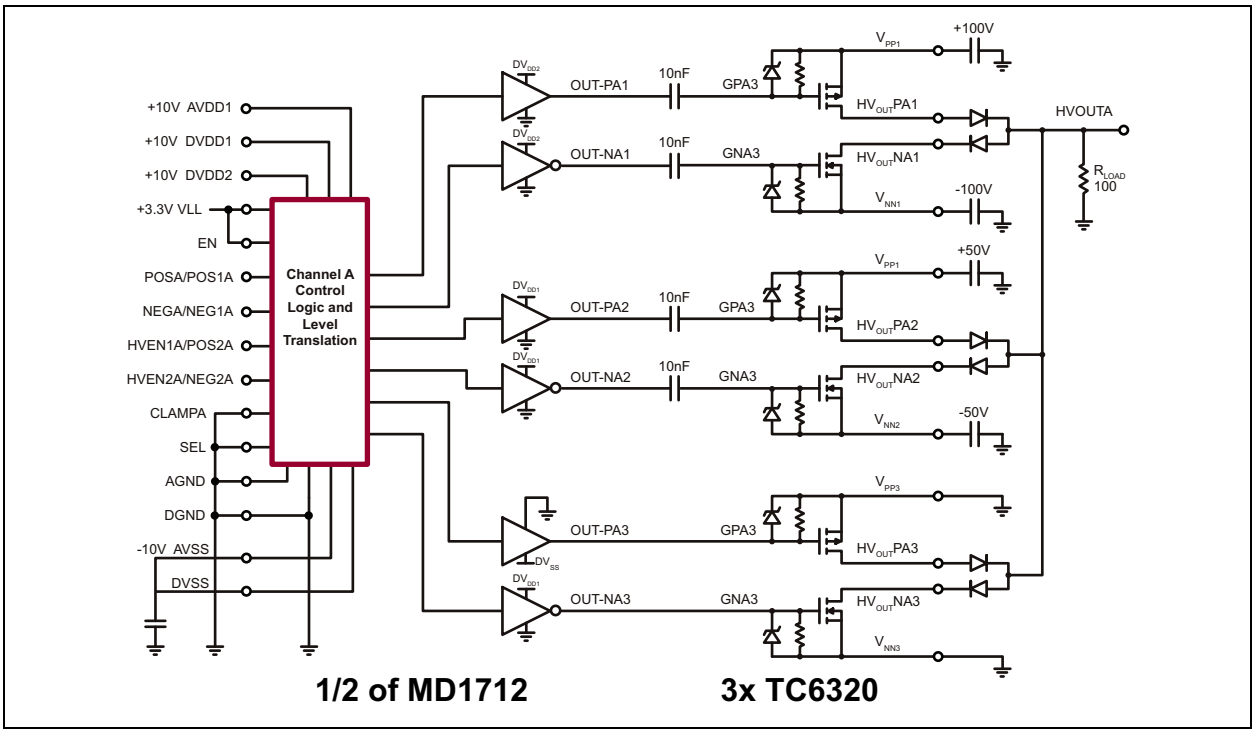


FIGURE 3-1: *Test Circuit for Channel A.*

TABLE 3-2: TRUTH FUNCTION TABLE FOR CHANNELS A AND B (FOR SEL = L)

Logic Control Inputs							V_{PP1} to V_{NN1} Output		V_{PP2} to V_{NN2} Output		V_{PP3} to V_{NN3} Output	
SEL	EN	HVEN1/ POS2	HVEN2/ NEG2	Clamp	POS/ POS1	NEG/ NEG1	$HV_{OUT}P1$	$HV_{OUT}N1$	$HV_{OUT}P2$	$HV_{OUT}N2$	$HV_{OUT}P3$	$HV_{OUT}N3$
0	1	0	0	0	0	0	OFF		OFF		ON	ON
0	1	0	0	0	0	1					ON	ON
0	1	0	0	0	1	0					ON	ON
0	1	0	0	0	1	1					OFF	OFF
0	1	0	0	1	0	0	OFF		OFF		OFF	
0	1	0	0	1	0	1						
0	1	0	0	1	1	0						
0	1	0	0	1	1	1						
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0	1	1	0	1	1	1						
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0	1	1	1	1	1	0						
0	1	1	1	1	1	1						
0	0	X	X	X	X	X	OFF		OFF		OFF	

TABLE 3-3: TRUTH FUNCTION TABLE FOR CHANNELS A AND B (FOR SEL = H)

Logic Control Inputs							V_{PP1} to V_{NN1} Output		V_{PP2} to V_{NN2} Output		V_{PP3} to V_{NN3} Output	
SEL	EN	HVEN1/ POS2	HVEN2/ NEG2	Clamp	POS/ POS1	NEG/ NEG1	$HV_{OUT}P1$	$HV_{OUT}N1$	$HV_{OUT}P2$	$HV_{OUT}N2$	$HV_{OUT}P3$	$HV_{OUT}N3$
1	1	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	
1	1	0	0	0	0	1	OFF	ON				
1	1	0	0	0	1	0	ON	OFF				
1	1	0	0	0	1	1	ON	ON				
1	1	0	0	1	0	0	OFF	OFF	OFF	ON	OFF	
1	1	0	0	1	0	1	OFF	ON				
1	1	0	0	1	1	0	ON	OFF				
1	1	0	0	1	1	1	ON	ON				
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1	1	0	1	0	1	1	ON	ON				
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1	1	0	1	1	0	1	OFF	ON				
1	1	0	1	1	1	0	ON	OFF				
1	1	0	1	1	1	1	ON	ON				
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1	1	1	1	0	1	0	ON	OFF				
1	1	1	1	0	1	1	ON	ON				
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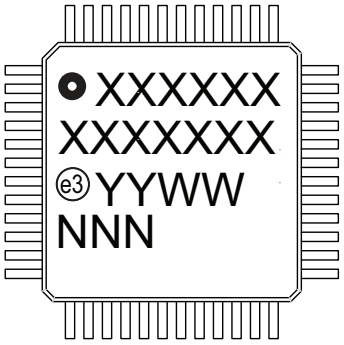
1	1	1	1	1	0	1	OFF	ON				
1	1	1	1	1	1	0	ON	OFF				
1	1	1	1	1	1	1	ON	ON				
1	0	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	

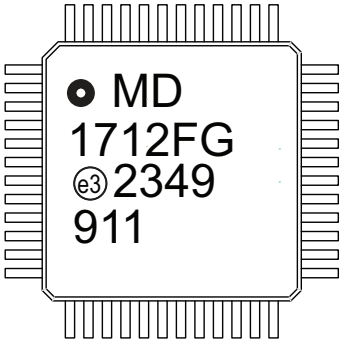
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

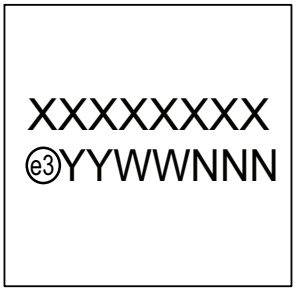
48-lead LQFP



Example



48-lead VQFN



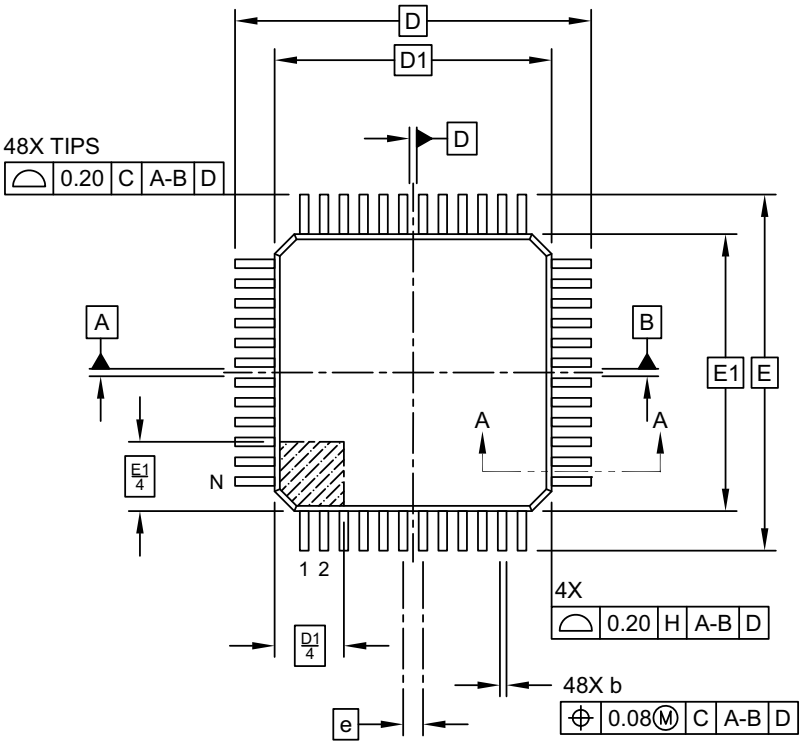
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

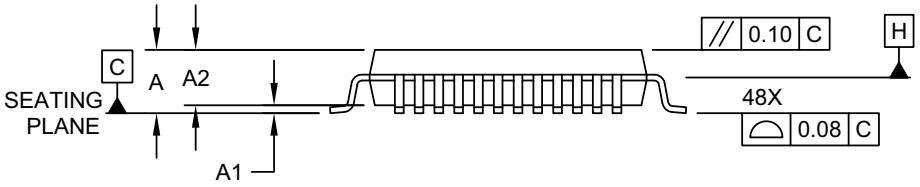
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP]
Supertex Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP]
Supertex Legacy Package

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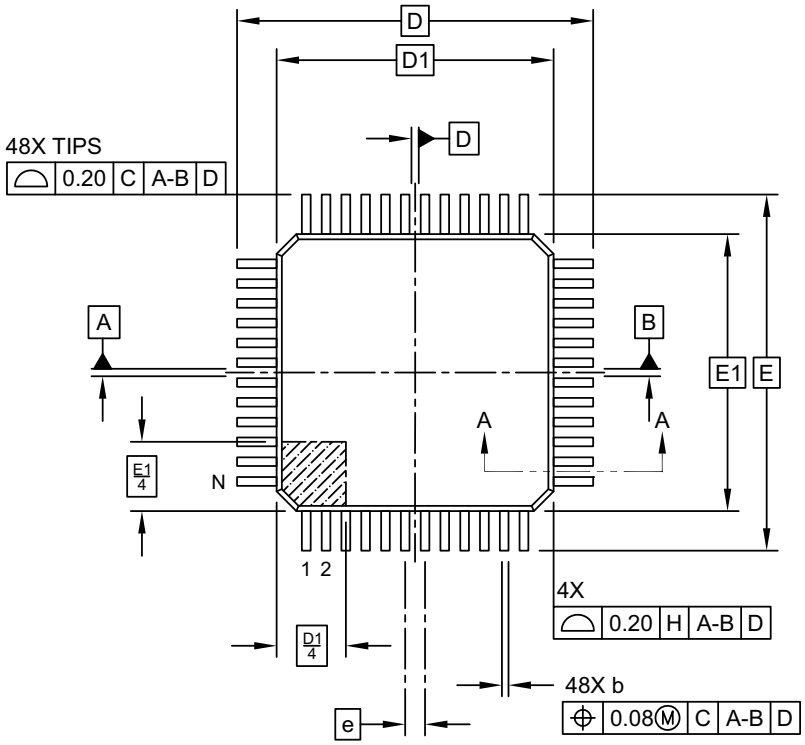
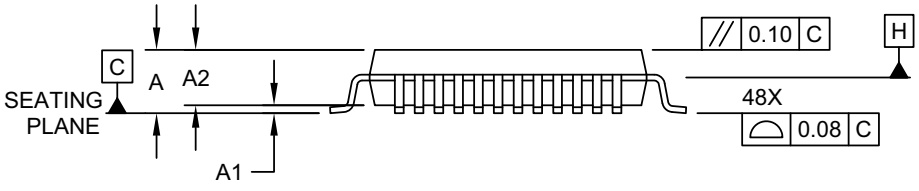


TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

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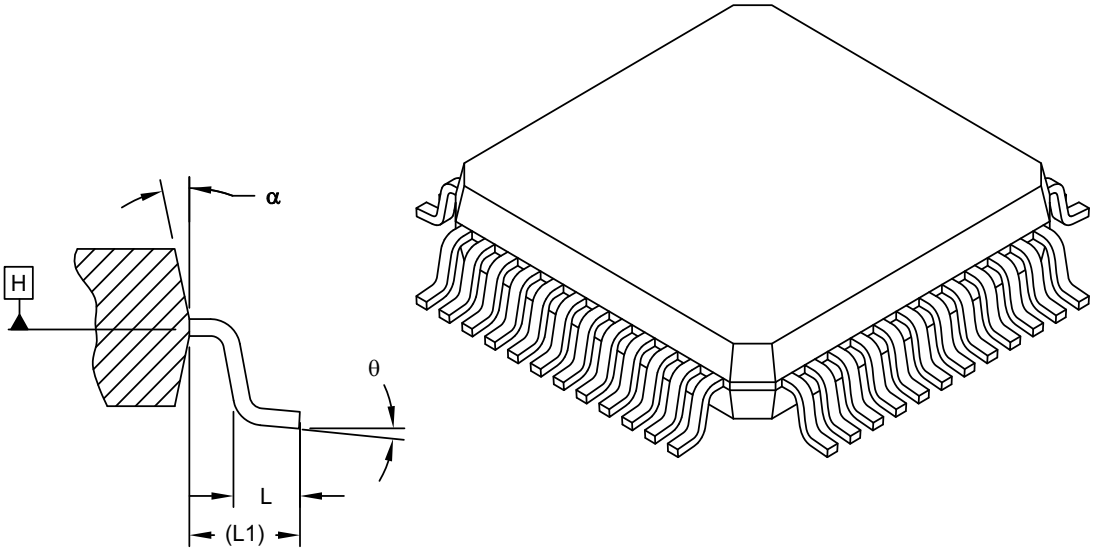


SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

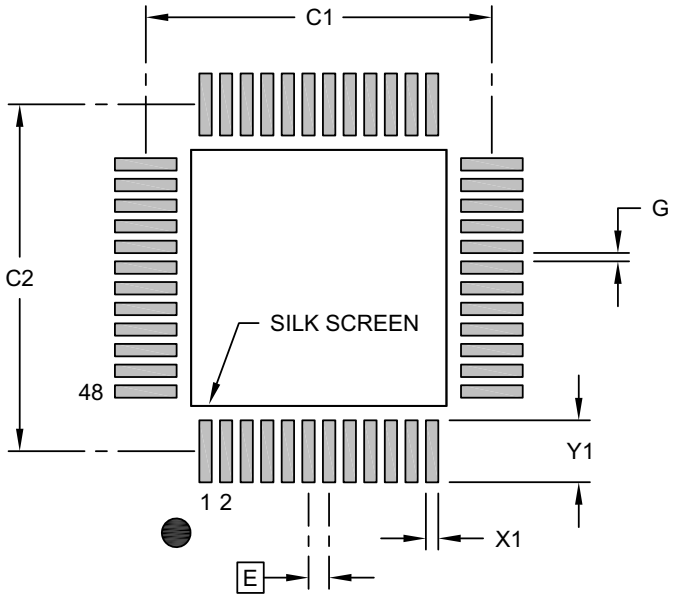
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278 Rev A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

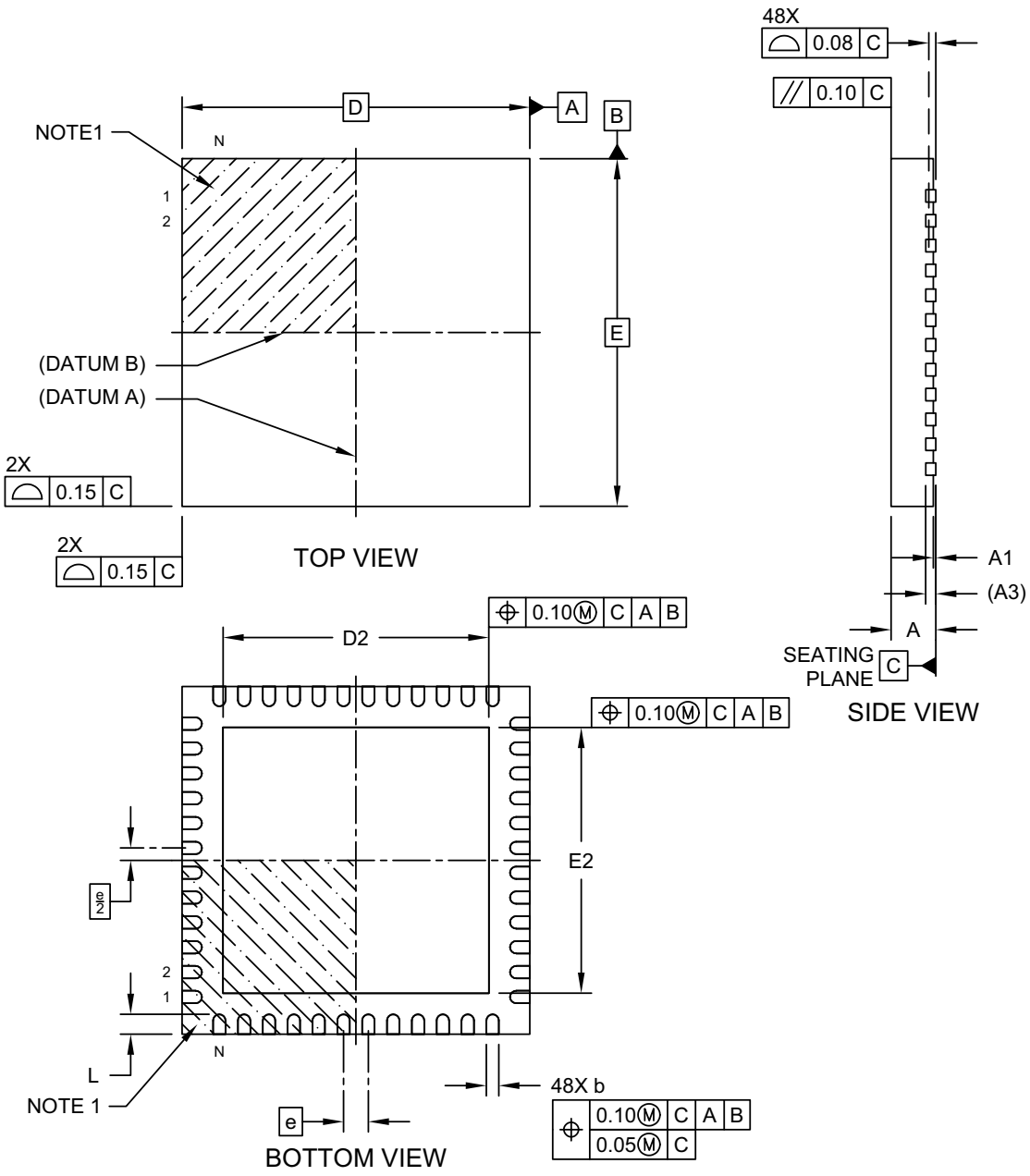
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2278 Rev A

48-Lead Very Thin Plastic Quad Flat, No Lead Package (Y6X) - 7x7x1.0 mm Body [VQFN] With 5.45 mm Exposed Pad; Supertex Legacy Package Code K6

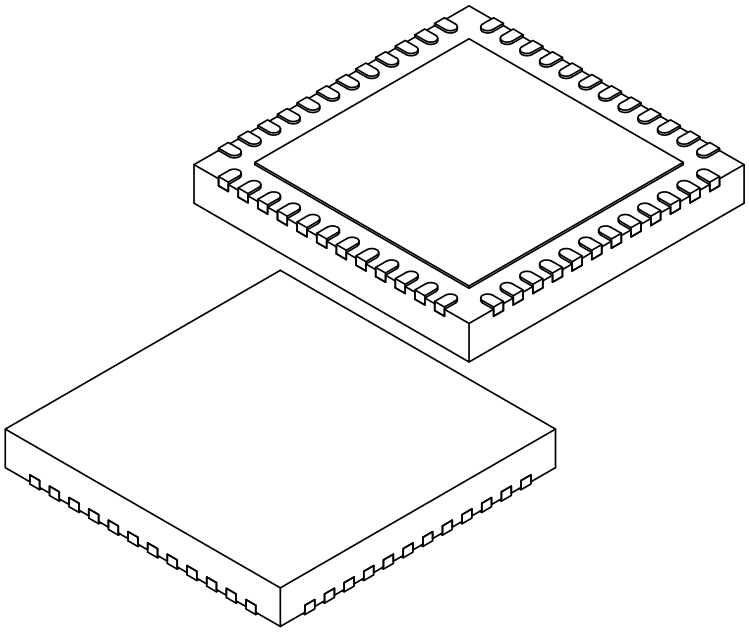
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-266-Y6X Rev A Sheet 1 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (Y6X) - 7x7x1.0 mm Body [VQFN] With 5.45 mm Exposed Pad; Supertex Legacy Package Code K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00.BSC	
Exposed Pad Length	D2	5.25	5.35	5.45
Overall Width	E		7.00.BSC	
Exposed Pad Width	E2	5.25	5.35	5.45
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50

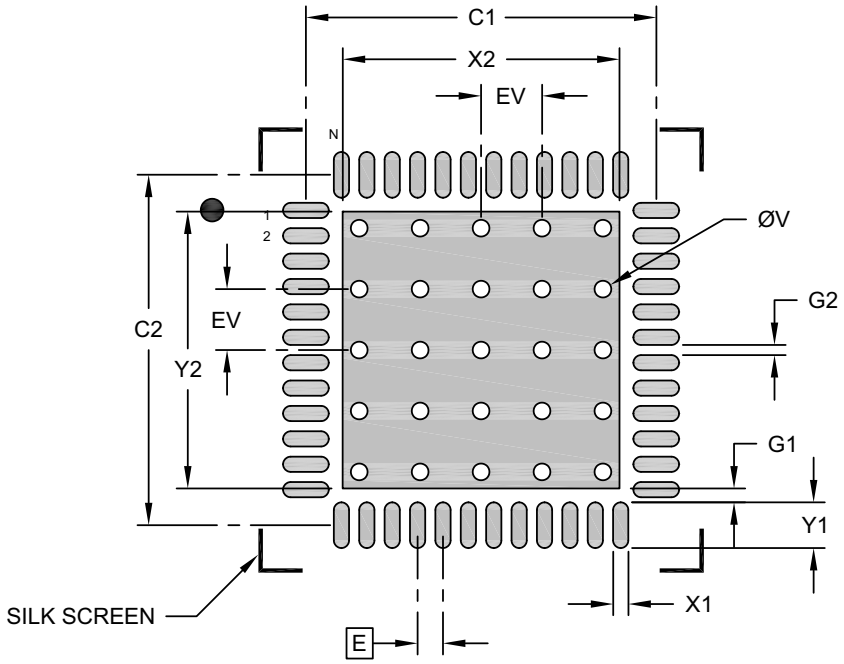
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-266-Y6X Rev A Sheet 2 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (Y6X) - 7x7x1.0 mm Body [VQFN] With 5.45 mm Exposed Pad; Supertex Legacy Package Code K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			5.45
Center Pad Length	Y2			5.45
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.90
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2266-Y6X Rev A

APPENDIX A: REVISION HISTORY

Revision A (June 2023)

- Converted Supertex Doc# DSFP-MD1712 to Microchip DS20005917A
- Changed package marking formats
- Removed the 48-lead LQFP FG M931 media type
- Removed the 48-lead VQFN K6 M933 media type
- Updated the quantity of the 48-lead VQFN K6 package from 250/Tray to 260/Tray to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	MD1712	=	High-Speed Integrated Ultrasound Driver IC
Packages:	FG	=	48-lead LQFP
	K6	=	48-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	250/Tray for an FG Package
		=	260/Tray for a K6 Package

Examples:

a) MD1712FG-G: High-Speed Integrated Ultrasound Driver IC, 48-lead LQFP, 250/Tray

b) MD1712K6-G: High-Speed Integrated Ultrasound Driver IC, 48-lead VQFN, 260/Tray

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