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Component Placement Checklist for the LAN9215, 100-pin LFBGA Package

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Component Placement Checklist for LAN9215

Information Particular for the 100-pin LFBGA Package

LAN9215 LFBGA Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TPO+, pin A10) as close to the LAN9215 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TPO-, pin A11) as close to the LAN9215 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (TPI+, pin A8) as close to the LAN9215 as possible.

4. Place the 49.9 Ω RX termination pull-up (TPI-, pin A9) as close to the LAN9215 as possible.

LAN9215 LFBGA Magnetics:

1. Place the 10.0 Ω TX/RX Channel Center Tap feed resistor as close to the magnetics as possible.

2. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

3. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

RJ45 Connector:

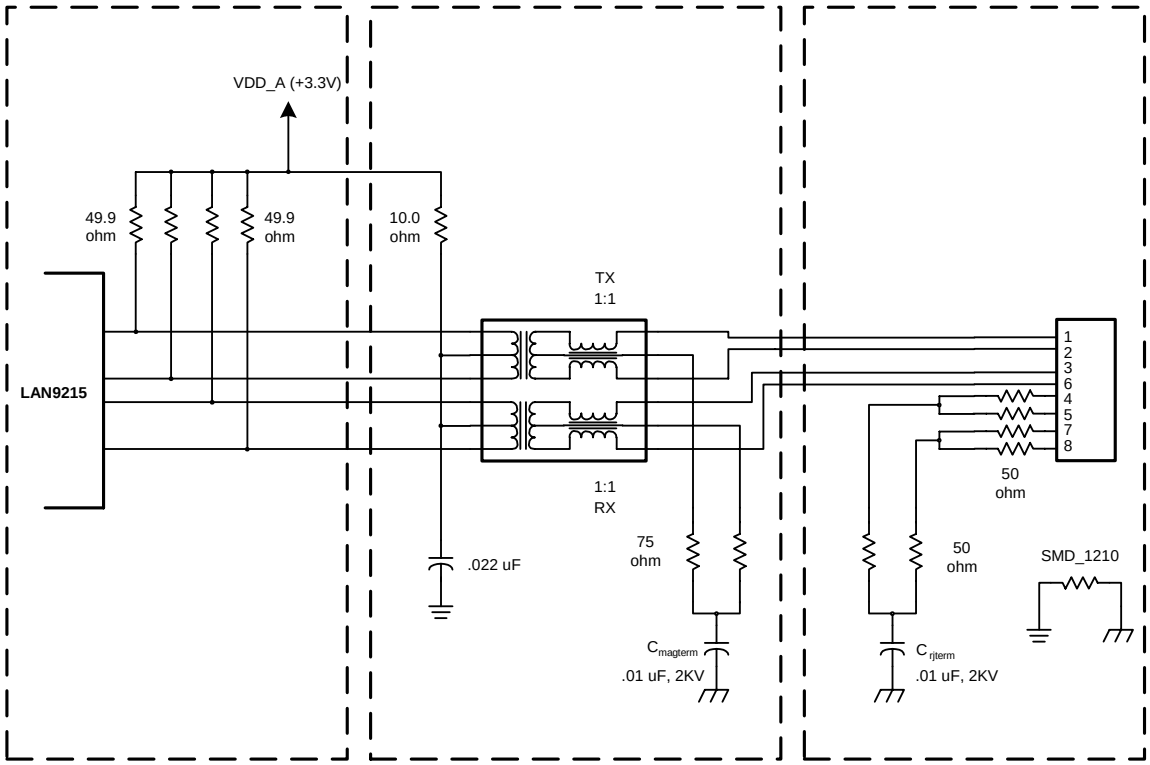
1. Place the RJ45 connector, the magnetics and the LAN9215 LFBGA as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9215 LFBGA.

3. Select and place the magnetics as to set up the best routing scheme from the LAN9215 LFBGA to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

4. Place the Unused Wire Pair termination resistors and the 1000 ρF, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.

5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.



Locate the four 49.9 ohm differential terminations close to the LAN9215

Locate these three resistors and two caps close to the magnetics

Locate all these components close to the RJ45 connector

Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TX+ & TX- signals placed close to the LAN9215 for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

Power Supply Connections:

1. Place the (12) VDD_IO decoupling capacitors for the LAN9215 LFBGA as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the (3) VDD_A decoupling capacitors for the LAN9215 LFBGA as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the (1) VREG decoupling capacitor for the LAN9215 LFBGA as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

4. Place the (1) VDD_REF decoupling capacitor for the LAN9215 LFBGA as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

Ground Connections:

1. There are no component placement issues associated with the LAN9215 LFBGA ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Voltage Reference Inputs:

1. There are no component placement issues associated with the Voltage Reference Inputs.

VDD_CORE:

1. VDD_CORE (pin D3) requires a 0.01 μF bypass capacitor and a low ESR 10 μF bulk capacitor placed as close as possible to pin D3.

2. The other VDD_CORE pins (pins D10, J3 & J10) only require a 0.01 μF bypass capacitor placed as close as possible to each pin.

VDD_PLL:

1. VDD_PLL (pin C2) requires a 0.01 μF bypass capacitor and a low ESR 10 μF bulk capacitor placed as close as possible to pin C2.

Crystal Connections:

1. Place the 25 MHz crystal, the 1.0 M Ω parallel resistor, the zero ohm series EMI resistor and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN9215 LFBGA (XTAL1, pin B1 & XTAL2, pin B2) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all crystal components are referenced to the same reference plane.

EEPROM Interface:

1. There are no component placement issues associated with the EEPROM Interface.

RBIAS Resistor:

1. Place the RBIAS resistor as close to pin E2 of the LAN9215 LFBGA as possible.

EXRES1 Resistor:

1. Place the EXRES1 resistor as close to pin A7 of the LAN9215 LFBGA as possible.

MII Interface:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN9215 LFBGA.

CPU Interface:

1. The design engineer must review placement issues associated with the Host Bus CPU Interface. Specific processor design guidelines should be reviewed in determining the placement of the LAN9215 device with respect to the processor. Address, data and control signal trace lengths must be considered when placing these two devices. Critical timing issues may arise if recommended trace lengths are exceeded.

Miscellaneous:

1. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.

2. Bulk capacitors for each power plane can reside anywhere on the plane they serve.