

APPLICATION NOTE

ATA5279 Application Hints

ATAN0003

Features

- General information
- Boost converter calculation and practical hints
- Antenna current regulation
- Oscillator aspects

Description

Most applications work with the components suggested by the typical applications in the datasheet. Nevertheless, this note includes design hints and considerations which may help in understanding the circuitry alignment.

An important feature of the antenna driver is the integrated boost converter, the antenna current regulation and its related dynamic behavior. Special attention must be given to thermal considerations in system design. Therefore, please refer to the related application note on the Atmel[®] Web site:

http://www.atmel.com/dyn/resources/prod_documents/doc9168.pdf

|| 10nF D V_{out} C_{in} PGND ATA5279 VDS Boost Control 댇 Driver Stage I_{ANT} AxP Sine wave Generator V_{ANT} Control AxN Current Keturn Line Switch Regulation V_{RLS} VSHF I_{ANT} Zero Cross VSHS DAC Detection Sample and Hold $\mathrm{V}_{\mathrm{RSH}}$ CINT RGND RSH C_{INT}

Figure 1. Function Principle of the Antenna Current Regulation Loop

1. Boost Converter

The boost converter is operated in PWM switch mode at a fixed frequency of typically 125kHz derived from a 8MHz resonator. It is able to generate an output voltage up to 40V providing the required supply voltage VDS for the driver stage. The antenna current regulator provides the required control voltage for the boost converter for driving the programmed current into the antenna. Thus the antenna current is largely independent of the antenna impedance and battery voltage (see Figure 1).

1.1 Theoretical Dependency of Boost Output Voltage

Ideally the converter output voltage depends on duty cycle (D) of the PWM control only.

However, in the real application the power conversion and thus the output voltage is reduced due to the losses of the affected components (NMOS, L, D, C) expressed by the efficiency factor η .

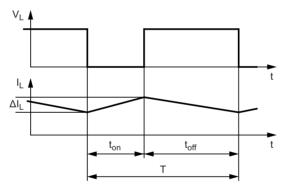
For converters operated in Continuous Conducting Mode (CCM) the output voltage is determined as follows:

$$V_{\text{out}} = V_{\text{in}} \times \frac{1}{1 - D} \times \eta$$
 (1)

or D =
$$1 - \frac{V_{in}}{V_{out}} \times \eta$$
 (2)

whereas D =
$$\frac{t_{on}}{T}$$
 (3)

Figure 1-1. Ripple Current through Inductance over Duty Cycle of VL Switch



Because the boost converter of the Atmel[®] ATA5279 is controlled within the antenna current regulation loop, the duty cycle and thus the output voltage are automatically set to the required value to achieve the programmed antenna current.

1.2 Inductance and Resulting Ripple Current for CCM Operation

In general, the inductance of the boost coil determines the ripple current through the related components, as inductance itself, the decoupling diode, and the smoothing capacitor at output. Seen from this standpoint, high inductance should be selected.

But, due to the stability of the antenna current regulation and the startup time of the Atmel ATA5279 application, the selection of the inductance is restricted (see also Section 3. "Practical Hints for Boost Converter Alignment" on page 7).

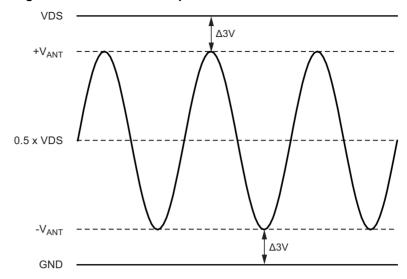
For a selected choke inductance, the ripple current results from the frequency and voltage relations:

$$\Lambda I_{L} = \frac{1}{f} \times (V_{out} - V_{in}) \times \frac{V_{in}}{V_{out}} \times \frac{1}{L}$$
 (4)

The output voltage V_{out} = VDS to be provided by the boost converter is determined by the sinusoidal driver voltage which is needed to drive the programmed antenna current through the impedance of the antenna used (see Figure 1-2). At the same time the boost output voltage should be increased according to the sine wave rail margin of typical 3V.



Figure 1-2. Sinusoidal Signal of Antenna Driver Output



$$V_{out} = VDS = 2 \times [I_{ant p} \times (Z_{ant} + R_{Shunt} + 2 \times R_{DSon}) + 3V]$$
 (5)

The average inductor input current I_{in} can be determined with a power balance calculation.

$$V_{\text{in_min}} \times I_{\text{in}} = \frac{1}{\eta} \times V_{\text{out_max}} \times I_{out}$$
 (6)

or
$$I_{in} = \frac{V_{out_max} \times I_{out}}{V_{in\ min} \times \eta}$$
 (7)

1.3 Calculation Example Based on the Atmel ATAB5279 Evaluation Board

 $L = 68 \mu H/2.3 A_{avg}$ **Boost inductance** Antenna impedance max $Z_{ant} = 12.5\Omega$ Shunt resistor $R_{Shunt} = 1\Omega$ $R_{DSon} = 0.6\Omega$ Driver stage Antenna peak current (max) $I_{ant} = 1Ap$ Input voltage (nominal) $I_{in} = 12V$

Efficiency of boost converter (assumed) $n = 0.70^{(1)}$

Note: Efficiency is decreased due to the lowered switching rise time due to EMC requirements.

The assumed values come to:

• Boost output voltage (5)
$$V_{out} = VDS = 2 \times [1Ap \times (12.5 + 1 + 2 \times 0.6)\Omega + 3V] = 35.4V$$

• Average output current
$$I_{out} = I_{ant} \times \frac{1}{\pi} = 0.318A$$

• Average input current (7)
$$I_{in} = \frac{34.5V \times 0.318A}{12V \times 0.70} = 1.3A$$

Inductor ripple current (4)
$$\Delta I_L = \frac{1}{125 \text{kHz}} \times (35.4 \text{V} - 12 \text{V}) \times \frac{12 \text{V}}{35.4 \text{V}} \times \frac{1}{68 \text{uH}} = 0.933 \text{A}$$

• Input peak current
$$I_{in_P} = I_{in} + \frac{1}{2} \times \Delta I_L = 1.3A + \frac{1}{2} \times 0.933A = 1.76A$$

1.4 Selection of the Boost Inductor

Typically the size of the inductor is determined by the required inductance and rated current.

However, in typical passive entry applications with a short operation cycle time the power dissipation of the inductor is not a key concern. Thus, diverging from the calculation, the next lower current rate can be selected (smaller size). However, consideration has been given to the fact that the effective inductance is reduced in relation to the specified value if the coil current is higher than the specified saturation current.

So for the Atmel® ATAB5279 evaluation board a larger inductor size (68µH/2.3A_{avg}) is selected so that stress test conditions are also covered. But in a typical PE application with a low operation cycle, a smaller size is normally acceptable.

1.5 Selecting the Output Decoupling Diode

Use of a schottky diode is recommended to minimize power dissipation. It is suitable in terms of forward voltage drop and recovery time. Switching losses can be ignored because these are small compared to conductivity losses.

The power dissipation and peak current can be roughly calculated as:

$$P_D \approx V_E \times I_{out}$$

(8) in the worst case

$$I_{D_P} \approx I_{out} \times \frac{V_{out}}{V_{in}}$$

9) in the worst case

$$I_{D_{-}P} \approx 0.318A \times \frac{40V}{12V} \approx 1.06A$$

A Schottky diode rated at 1A/60V would satisfy the requirement for the power dissipation and peak current calculated. Nevertheless, the voltage drop and thus the power loss are reduced if a higher current rate is chosen.

1.6 Selecting the Output Capacitor

Based on the required load current the output ripple voltage depends in two ways on the capacitor. One portion is effected by the discharge of the capacitor when loading during the conduction phase (D = t_{on}/T) of the boost transistor. A second part is generated during the complementary time phase (1-D) during which the charge current generates a voltage drop at the impedance ESR of the capacitor.

$$\Delta V_{out} = \frac{I_{out} \times D}{f \times C}$$

$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{12V}{40V} = 0.7$$

$$\Delta V_{\text{out}} = \text{ESR} \times \left(\frac{I_{\text{out}}}{1 - D} + \frac{\Delta I_{\text{L}}}{2} \right)$$

A high capacitor value should be selected to reduce ripple voltage. Even bigger capacitors result in lower ESR values. But, in a typical PE application a fast startup of the driver voltage VDS is required, thereby limiting the output capacitor value. Finally it must be determined if the selected capacitor is suitable for the resulting ripple current. RMS value $I_{C\ RMS}$.

$$I_{C_RMS} \ge I_{out} \times \sqrt{\frac{D}{1-D}}$$

With the calculated values above I_{out} =0.318A and D = 0.7 the capacitor load current results in $I_{C,RMS}$ = 0.485mA

The new ceramic capacitors on the market are characterized by ultra low ESR values which allow high RMS current load. For example, on the evaluation board ATAB5279 the selected ceramic capacitor $10\mu\text{F}/50\text{V}$ is specified with an ESR of <10m Ω . So the temperature rise of this capacitor is less than 10°C at a RMS current of 4 A.



2. Selecting the Input LC Filter

The input current becomes a continuous triangular shape if an inductor L_{in} is used at the boost converter input. In addition, it serves to smooth the ripple current into the input capacitor C_{in} .

A line input inductor may be needed to achieve EMC approval for automotive applications. Usually, the required inductance depends on the specific application and design specification and cannot be defined precisely in advance. To minimize the components variety, it is useful to select the same inductor used for the boost section (for example 68μ H/2.3A_{avq}).

The input capacitor provides a low impedance source to force the boost converter and prevents any impedance interaction with the battery power supply. Depending on the acceptable ripple voltage, recommended values range from $47\mu\text{F}$ to $220\mu\text{F}$. Make sure that the allowable rms ripple current of the selected capacitor is higher than the equivalent rms of the boost inductor ripple current ΔIL .

$$I_{Cin_rms} = \frac{\Delta I_L}{\sqrt{3}} \text{ applied to the example } I_{Cin_rms} = \frac{0.933A}{\sqrt{3}} = 0.538A$$

The capacitor C_{in} used with the 220 μ F/50V evaluation board has an rms current capability of 1290mA at 105°C, thus complying with the above-mentioned requirement.



3. Practical Hints for Boost Converter Alignment

As already mentioned before, the inductance of the boost coil determines the ripple current through the related components, as inductance itself, the decoupling diode, and the smoothing capacitor at the output.

Considered from this perspective, a higher inductance helps smooth the ripple current and reduces the thermal load, especially of the internal power NMOS.

Not only does higher inductance require a larger coil and cost more, it can also negatively impact boost control stability. This occurs in particular with a low current load when the boundary from CCM to DCM operating mode has been reached. Furthermore, higher inductance values lead to an increased oscillation effect on the NMOS switch (VL) if the converter switches to DCM operation.

Figure 3-1. Continuous Conduction Mode CCM

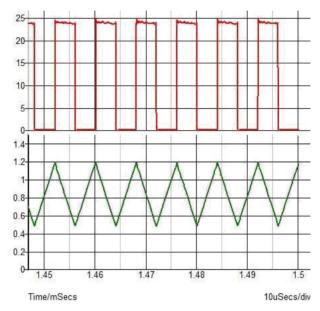


Figure 3-2. Discontinuous Conduction Mode DCM

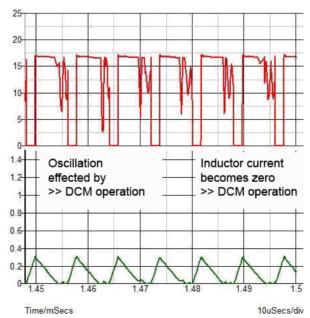
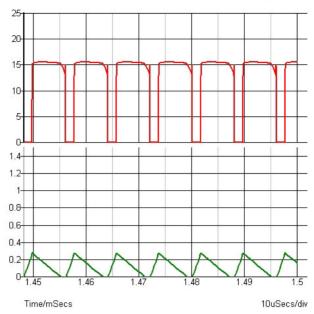




Figure 3-3. Discontinuous Conduction Mode DCM with RC in Parallel to Output Diode D



Here, the selection of the inductor value involves a trade-off between low ripple current and stable operation of the boost converter. Atmel therefore recommends basing the inductor selection on the specific load conditions of the driver supply voltage VDS which is needed to force the required antenna current through the antenna used. Table 3-1 provides guideline values for selecting a suited inductance for the boost converter.

Table 3-1. Guideline Values

| | Higher Load Range | Lower Load Range |
|----------------------------|-------------------|------------------|
| Driver Supply Voltage VDS | 25 to 40V | Up to 25V |
| Suggested Boost Inductance | 47 to 100μH | 22 to 47μH |

Applications which also need to cover low loads have to be run in DCM operating mode. The resulting oscillation on the NMOS switch output VL may be undesirable due to EMC requirements.

As seen in simulations, this oscillation can be suppressed by RC circuitry in parallel to the decoupling diode D with 10nF in series with 47Ω (see Figure 1 on page 2).

4. Antenna Current Regulator CINT Circuitry

The internal current regulator is designed like a transconductance op-amp and provides sink/source output current at the CINT pin. A typical application has the capacitor CINT connected to ground so that the regulator has a pure integration property. The resulting voltage at the CINT pin supplies the internal control for the driver sine wave amplitude as well for the boost converter unit.

Selecting the CINT capacitor involves a trade-off between rise time and overshoot of antenna current. However, it is difficult to calculate or simulate this value because the dynamic behavior of the antenna regulation loop also depends on the antenna Q factor and the boost converter circuitry. Selecting an appropriate CINT value through practical measurements is therefore recommended. For reference, the graphs in Figure 4-1 depict the impact of the CINT value on the dynamic behavior of the antenna current. The measurements were done in combination with the Atmel[®] ATAB5279 antenna driver board on which CINT = 10nF is typically used.

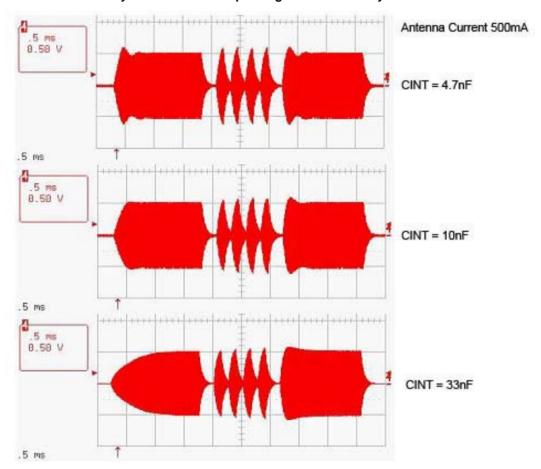


Figure 4-1. Antenna Current Dynamic Behavior Depending on CINT Circuitry



5. Oscillator Aspects

The Atmel[®] ATA5279 oscillator circuit is based on the principle of a *Pierce oscillator*. It consists of an inverter circuit characterized by its output resistance R_{OSCO} and a feedback resistance R_{FB} used for running it in linear mode. To achieve secure and faster startup the output resistance is reduced during the switch-on phase.

For typical applications an 8MHz ceramic oscillator is used for clocking and deriving the 125kHz driver frequency. If higher accuracy is required, it can also be operated using an appropriate crystal; however startup times up to 10 times longer must be taken into account. Alternatively, ceramic resonators with a tolerance of 0.1% are also available.

The circuit in Figure 5-1 shows the generic inverter in combination with the equivalent circuit of the ceramic resonator used.

Figure 5-1. Equivalent Oscillator Circuitry

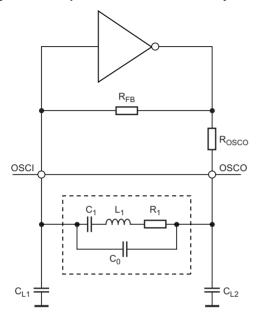
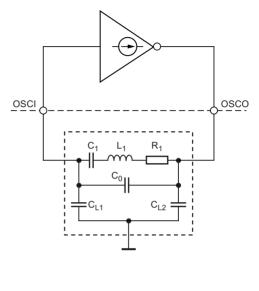


Figure 5-2. Inverter with Transconductance Characteristic



Internal Parameters Specified on the Atmel ATA5279 Datasheet:

Driver resistance during startup R_{OSCO} 0.9k Ω to 2.2k Ω (See datasheet parameter 3.4) Driver resistance during operation R_{OSCO} 1.8k Ω to 4.4k Ω (See datasheet parameter 3.5) Feedback resistance R_{FB} 220k Ω to 340k Ω (See datasheet parameter 3.6)

Parameters of 8MHz Ceramic Resonator cstce8M00G55A (Murata):

 $L_1 = 257\mu H$; $R_1 = 6.7\Omega$ (max. 40Ω); $C_1 = 1.61pF$; $C_0 = 13.07pF$; $C_{L1} = 10pF$; $C_{L2} = 10pF$

The Atmel ATAB5279 application board has been approved by the resonator manufacturer in terms of oscillator startup and frequency stability.

An important aspect in terms of the oscillator start-up time is the negative resistance –R of the active network.

According to Barkhausen stability criterion, oscillation occurs if the negative resistance exceeds the effective resistance of the oscillator branch.

 $|-R| \ge R_e$



Crystal manufacturers recommend selecting negative resistance 5 to 10 times greater than the effective resistance to overcome the effects of tolerances and temperature.

The margin for oscillation startup should be: $\frac{|-R|}{R} \approx 5$ to 10

To estimate the margin of the oscillator startup, the resistance -R and Re can be calculated by using the approximation formula based on the Barkhausen stability criterion.

Negative resistance of active network:

$$|-R| = \frac{g_{m}}{(2 \times \pi \times f)^{2} \times C_{L1} \times C_{L2}} = \frac{0.6 \mu A/mV}{(2 \times \pi \times 125 \text{kHz})^{2} \times 10 \text{pF} \times 10 \text{pF}} = 2375 \Omega$$

 g_m (min) = 0.6 μ A/mV (design parameter 3.9) Transconductance of the inverter

 $C_{1,1}/C_{1,2} = 10pF$ Load capacity of resonator

 $C_{L} = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = \frac{10pF \times 10pF}{10pF + 10pF} = 5pF$ Effective load capacity of resonator:

 $R_e = R_1 \times \left(1 + \frac{C_0}{C_1}\right)^2 = 6.7\Omega \times \left(1 + \frac{13.07pF}{5pF}\right)^2 = 87,51\Omega$ Effective resistance of resonator:

 $m = \frac{|-R|}{R_o} = \frac{2975\Omega}{87,51\Omega} = 27.1$ Margin for oscillation startup:

Concluding Note Regarding Resonator Selection:

With respect to the assumed oscillator parameters, the calculated margin for oscillation startup fulfills the recommended relation

 $|-R|/R_e$ to fall in a range between 5 and 10.

However, regardless of that estimate, it is advisable to have resonator qualification carried out as offered by most manufacturers. This service involves a check of the customer's original PCB and provides a recommendation on the right type of resonator and suitable external circuits.



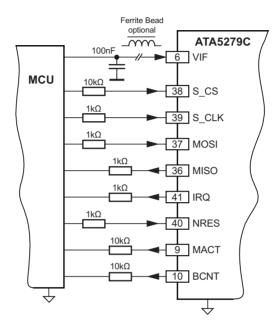
6. SPI Control

The Atmel® ATA5279 SPI slave interface allows to be operated by a clock frequency of up to 2MHz. The insertion of series resistors into the control lines may help for decoupling to the microcontroller and limiting the dynamic current rise.

Particular care has to be taken to the VIF supply input. Therefore, at least a blocking capacitor to AGND (e.g. 100nF) has to be placed close to the device to minimize the noise generated by the internal 8MHz clock frequency.

An enhanced suppression can be achieved when filtering the VIF noise by an additional inline ferrite bead according to Figure 6-1.

Figure 6-1. SPI Interface



7. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|-----------------|-------------------------------------|
| 9271B-RKE-04/15 | Put document in the latest template |











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