Silicon Errata and Data Sheet Clarifications

ATmega329P/ATmega3290P

Introduction

The ATmega329P/3290P devices you have received conform functionally to the current device data sheet (ww1.microchip.com/downloads/en/DeviceDoc/Atmel-8021-AVR-ATmega329P-3290P_Datasheet.pdf), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega329P/3290P devices.

Note:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous and current

1. Silicon Issue Summary

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		ATmega329P/3290P		
		Rev. A (1)	Rev. B	Rev. C
Device	2.2.1. Using BOD Disable Will Make the Device Reset	X	-	-
Timer	2.3.1. Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Using BOD Disable Will Make the Device Reset

If the device enters sleep with the BOD turned off with the BOD disable option enabled, a BOD reset will be generated at wakeup, and the device will reset.

Work Around

Do not use BOD disable.

Affected Silicon Revisions

ATmega329P/3290P		
Rev. A	**Rev. B**	**Rev. C**
X	**-**	**-**

2.3 Timer

2.3.1 Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer

The interrupt will be lost if writing a timer register that is a synchronous timer clock when the asynchronous Timer/Counter register (TCNTx) is `0x00`.

Work Around

Always check that the asynchronous Timer/Counter register neither has the value `0xFF` nor `0x00` before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

Affected Silicon Revisions

ATmega329P/3290P		
Rev. A	**Rev. B**	**Rev. C**
X	**X**	**X**

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS4000XXXX).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATmega329P/3290P* (this document).

See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Power Management and Sleep Modes

3.2.1 Power Management and Sleep Modes

A clarification has been made to the *Active clock domains and wake-up sources in the different sleep modes* table to make the headings visible.

Table 10-1. Active Clock Domains and Wake-Up Sources in the Different Sleep Modes

	Active Clock Domains					Oscillators		Wake-up Sources							
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT0 and Pin Change	USI Start Condition	LCD Controller	Timer2	SPM/ EEPROM Ready	ADC	Other I/O	Software BOD Disable
Idle			X	X	X	X	X(2)	X	X	X	X	X	X	X	
ADC NRM				X	X	X	X(2)	X(3)	X	X(2)	X(2)	X	X		
Power-down								X(3)	X						X
Power-save					X		X	X(3)	X	X	X				X
Standby(1)						X		X(3)	X						X

Notes:

1. Only recommended with external XTAL or resonator selected as clock source.
2. If either the LCD controller or Timer/Counter2 is running in asynchronous mode.
3. For INT0, only level interrupt.

3.3 Interrupts

3.3.1 Interrupt Vectors in ATmega329P/3290P

A clarification for the source names of the Interrupt vectors has been made to comply with the header file naming convention.

Table 3-1. Reset and Interrupt Vectors in ATmega329P

Vector No	Program Address(2)	Source	Interrupts definition
1	0x0000(1)	RESET	External pin, Power-on Reset, Brown-out Reset, Watchdog System Reset and JTAG AVR Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	PCINT0	Pin Change Interrupt Request 0
4	0x0006	PCINT1	Pin Change Interrupt Request 1
5	0x0008	**TIMER2_COMP**	Timer/Counter2 Compare Match
6	0x000A	**TIMER2_OVF**	Timer/Counter2 Overflow
7	0x000C	**TIMER1_CAPT**	Timer/Counter1 Capture Event
8	0x000E	**TIMER1_COMPA**	Timer/Counter1 Compare Match A
9	0x0010	**TIMER1_COMPB**	Timer/Coutner1 Compare Match B
10	0x0012	**TIMER1_OVF**	Timer/Counter1 Overflow
11	0x0014	**TIMER0_COMP**	Timer/Counter0 Compare Match
12	0x0016	**TIMER0_OVF**	Timer/Counter0 Overflow
13	0x0018	**SPI_STC**	SPI Serial Transfer Complete
14	0x001A	**USART0_RX**	USART Receive complete
15	0x001C	**USART0_UDRE**	USART Data Register Empty
16	0x001E	**USART0_TX**	USART Transmit complete
17	0x0020	**USI_START**	USI Start Condition
18	0x0022	**USI_OVERFLOW**	USI Overflow
19	0x0024	**ANALOG_COMP**	Analog Comparator
20	0x0026	ADC	ADC Conversion complete
21	0x0028	**EE_READY**	EEPROM Ready
22	0x002A	**SPM_READY**	Store Program Memory Ready
23	0x002C	LCD	LCD Start of Frame

Notes:

1. When the BOOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See "*Boot Loader Support – Read-While-Write Self- Programming*".
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

The table below shows the Reset and Interrupt Vectors placement for the various combinations of the BOOTRST and IVSEL settings. If the program never enables an interrupt source, the Interrupt Vectors are unused, and regular program codes can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa.

Table 3-2. Reset and Interrupt Vectors Placement

BOOTRST(1)	IVSEL	Reset Address	Interrupt Vectors Start Address
1	0	0x000	0x002
1	1	0x000	Boot Reset Address + 0x0002
0	0	Boot Reset Address	0x002
0	1	Boot Reset Address	Boot Reset Address + 0x0002

Note: 1. For the BOOTRST Fuse, "1" means unprogrammed, while "0" means programmed.

The most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address   Labels    Code    Comments
0x0000              jmp      RESET              ; Reset Handler
0x0002              jmp      INT0               ; IRQ0 Handler
0x0004              jmp      PCINT0             ; PCINT0 Handler
0x0006              jmp      PCINT1             ; PCINT1 Handler
0x0008              jmp      TIMER2_COMP        ; Timer2 CompareA Handler
0x000A              jmp      TIMER2_OVF         ; Timer2 Overflow Handler
0x000C              jmp      TIMER1_CAPT        ; Timer1 Capture Handler
0x000E              jmp      TIMER1_COMPA       ; Timer1 CompareA Handler
0x0010              jmp      TIMER1_COMPB       ; Timer1 CompareB Handler
0x0012              jmp      TIMER1_OVF         ; Timer1 Overflow Handler
0x0014              jmp      TIMER0_COMP        ; Timer0 Compare Handler
0x0016              jmp      TIMER0_OVF         ; Timer0 Overflow Handler
0x0018              jmp      SPI_STC            ; SPI Transfer Complete Handler
0x001A              jmp      USART0_RX          ; USART RX Complete Handler
0x001C              jmp      USART0_UDRE        ; USART UDR Empty Handler
0x0020              jmp      USI_START          ; USI Start Condition Handler
0x0022              jmp      USI_OVERFLOW       ; USI Overflow Handler
0x0024              jmp      ANALOG_COMP        ; Analog Comparator Handler
0x0026              jmp      ADC                ; ADC Conversion Complete Handler
0x0028              jmp      EE_READY           ; EEPROM Ready Handler
0x002A              jmp      SPM_READY          ; SPM Ready Handler
0x002C              jmp      LCD                ; LCD Start of Frame Handler

;
0x0034    RESET:    ldi      r16,high(RAMEND)   ; Main program start
0x0035              out      SPH,r16            ; Set Stack Pointer to top of RAM
0x0036              ldi      r16,low(RAMEND)
0x0037              out      SPL,r16
0x0038              sei                         ; Enable interrupts
0x0039              <instr>  xxx
...       ...       ...                            ...
```

When the BOOTRST Fuse is unprogrammed, the Boot section size is set to 2 KB, and the MCUCR.IVSEL is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address   Labels     Code                       Comments
0x0000    RESET:     ldi      r16,high(RAMEND)  ; Main program start
0x0001               out      SPH,r16           ; Set Stack Pointer to top of RAM
0x0002               ldi      r16,low(RAMEND)
0x0003               out      SPL,r16
0x0004               sei                        ; Enable interrupts
0x0005               <instr> xxx
;
.org 0x1C02
0x1C02               jmp      EXT_INT0          ; IRQ0 Handler
0x1C04               jmp      EXT_INT1          ; IRQ1 Handler
...                           ...      ...              ;
0x1C32               jmp      SPM_RDY           ; SPM Ready Handler
```

When the BOOTRST Fuse is programmed and the Boot section size is set to 2 KB, the most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address   Labels     Code                       Comments
.org 0x0002
0x0002               jmp      EXT_INT0          ; IRQ0 Handler
0x0004               jmp      EXT_INT1          ; IRQ1 Handler
...                  ...      ...               ;
0x0032               jmp      SPM_RDY           ; SPM Ready Handler
;
.org  0x1C00
0x1C00    RESET:    ldi      r16,high(RAMEND)  ; Main program start
0x1C01              out      SPH,r16           ; Set Stack Pointer to top of RAM
0x1C02              ldi      r16,low(RAMEND)
0x1C03              out      SPL,r16
0x1C04              sei                        ; Enable interrupts
0x1C05              <instr>  xxx
```

When the BOOTRST Fuse is programmed, the Boot section size is set to 2 KB and the MCUCR.IVSEL is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address    Labels    Code                          Comments
;
.org 0x1C00
0x1C00               jmp      RESET                ; Reset handler
0x1C02               jmp      EXT_INT0             ; IRQ0 Handler
0x1C04               jmp      EXT_INT1             ; IRQ1 Handler
...                  ...      ...                  ;
0x1C32               jmp      SPM_RDY              ; SPM Ready Handler
;
0x1C34    RESET:     ldi      r16,high(RAMEND)     ; Main program start
0x1C35               out      SPH,r16              ; Set Stack Pointer to top of RAM
0x1C36               ldi      r16,low(RAMEND)
0x1C37               out      SPL,r16
0x1C38               sei                           ; Enable interrupts
0x1C39              <instr>  xxx
```

Table 3-3. Reset and Interrupt Vectors in ATmega3290P

Vector No	Program Address(2)	Source	Interrupts definition
1	0x0000(1)	RESET	External pin, Power-on Reset, Brown-out Reset, Watchdog Reset and JTAG AVR Reset.
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	PCINT0	Pin Change Interrupt Request 0
4	0x0006	PCINT1	Pin Change Interrupt Request 1
5	0x0008	**TIMER2_COMP**	Timer/Counter2 Compare Match
6	0x000A	**TIMER2_OVF**	Timer/Counter2 Overflow
7	0x000C	**TIMER1_CAPT**	Timer/Counter1 Capture Event
8	0x000E	**TIMER1_COMPA**	Timer/Counter1 Compare Match A
9	0x0010	**TIMER1_COMPB**	Timer/Counter1 Compare Match B
10	0x0012	**TIMER1_OVF**	Timer/Counter1 Overflow
11	0x0014	**TIMER0_COMP**	Timer/Counter0 Compare Match
12	0x0016	**TIMER0_OVF**	Timer/Counter0 Overflow
13	0x0018	**SPI_STC**	SPI Serial Transfer Complete
14	0x001A	**USART0_RX**	USART0 Receive complete
15	0x001C	**USART0_UDRE**	USART Data Register Empty
16	0x001E	**USART0_TX**	USART Transmit complete
17	0x0020	**USI_START**	USI Start condition
18	0x0022	**USI_OVERFLOW**	USI Overflow
19	0x0024	**ANALOG_COMP**	Analog Comparator
20	0x0026	ADC	ADC Conversion complete
21	0x0028	**EE_READY**	EEPROM Ready
22	0x002A	**SPM_READY**	Store Program Memory Ready
23	0x002C	LCD	LCD Start of Frame
24	0x002E	PCINT2	Pin Change Interrupt Request 2
25	0x0030	PCINT3	Pin Change Interrupt Request 3

Notes:

1. When the BOOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See "*Boot Loader Support – Read-While-Write Self- Programming*".
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

The most typical and general program setup for the Reset and Interrupt Vector Addresses is:

```
Address   Labels    Code                        Comments
0x0000              jmp     RESET               ; Reset Handler
0x0002              jmp     INT0                ; IRQ0 Handler
0x0004              jmp     PCINT0              ; PCINT0 Handler
0x0006              jmp     PCINT1              ; PCINT1 Handler
0x0008              jmp     TIMER2_COMP         ; Timer2 CompareA Handler
0x000A              jmp     TIMER2_OVF          ; Timer2 Overflow Handler
0x000C              jmp     TIMER1_CAPT         ; Timer1 Capture Handler
0x000E              jmp     TIMER1_COMPA        ; Timer1 CompareA Handler
0x0010              jmp     TIMER1_COMPB        ; Timer1 CompareB Handler
0x0012              jmp     TIMER1_OVF          ; Timer1 Overflow Handler
0x0014              jmp     TIMER0_COMP         ; Timer0 Compare Handler
0x0016              jmp     TIMER0_OVF          ; Timer0 Overflow Handler
0x0018              jmp     SPI_STC             ; SPI Transfer Complete Handler
0x001A              jmp     USART0_RX           ; USART RX Complete Handler
0x001C              jmp     USART0_UDRE         ; USART UDR Empty Handler
0x0020              jmp     USI_START           ; USI Start Condition Handler
0x0022              jmp     USI_OVERFLOW        ; USI Overflow Handler
0x0024              jmp     ANALOG_COMP         ; Analog Comparator Handler
0x0026              jmp     ADC                 ; ADC Conversion Complete Handler
0x0028              jmp     EE_READY            ; EEPROM Ready Handler
0x002A              jmp     SPM_READY           ; SPM Ready Handler
0x002C              jmp     LCD                 ; LCD Start of Frame Handler
0x002E              jmp     PCINT2              ; PCINT2 Handler Handler
0x0030              jmp     PCINT3              ; PCINT3 Handler Handler
;
0x0034    RESET:    ldi     r16,high(RAMEND)    ; Main program start
0x0035              out     SPH,r16             ; Set Stack Pointer to top of RAM
0x0036              ldi     r16,low(RAMEND)
0x0037              out     SPL,r16
0x0038              sei                         ; Enable interrupts
0x0039              <instr>  xxx
...       ...       ...                            ...
```

3.4 Electrical Characteristics – TA = -40°C to 85°C

3.4.1 Analog Input Offset Voltage (T_A = -40°C to 85°C)

A clarification has been made for the "*Analog Comparator Input Offset Voltage*".

Table 3-4. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage, except XTAL1 pin	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	-0.5 -0.5		$0.2V_{CC}$(1) $0.3V_{CC}$(1)	V
V_{IL1}	Input low voltage, XTAL1 pin	V_{CC} = 1.8-5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IH}	Input high voltage, except XTAL1 and $\overline{\text{RESET}}$ pins	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	$0.7V_{CC}$(2) $0.6V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH1}	Input high voltage, XTAL1 pin	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	$0.8V_{CC}$(2) $0.7V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH2}	Input high voltage, $\overline{\text{RESET}}$ pin	V_{CC} = 1.8-5.5V	$0.85V_{CC}$(2)		V_{CC} + 0.5	
V_{OL}	Output low voltage(3), Port A, C, D, E, F, G, H, J	I_{OL} = 10 mA, V_{CC} = 5V I_{OL} = 5 mA, V_{CC} = 3V			0.9 0.6	
V_{OL1}	Output low voltage(3), Port B	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.9 0.6	
V_{OH}	Output high voltage(4), Port A, C, D, E, F, G, H, J	I_{OH} = -10 mA, V_{CC} = 5V I_{OH} = -5 mA, V_{CC} = 3V	4.2 2.3			
V_{OH1}	Output high voltage(4), Port B	I_{OH} = -20 mA, V_{CC} = 5V I_{OH} = -10 mA, V_{CC} = 3V	4.2 2.3			
I_{IL}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin high (absolute value)			1	

.....continued						
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{RST}	Reset pull-up resistor		20		100	kΩ
R_{PU}	I/O Pin pull-up resistor		20		100	kΩ
V_{ACIO}	Analog comparator input offset voltage	V_{CC} = 5V V_{in} = V_{CC}/2		< 10	40	mV
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} < 3.6V** **V_{in} < 0.5V**		**<15**	**60[5]**	**mV**
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} > 3.6V** **V_{in} < 0.5V**		**<15**	**500[5]**	**mV**
I_{ACLK}	Analog comparator	V_{CC} = 5V V_{in} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low.
2. "Min" means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all I_{OL} may not exceed 400 mA for all ports.
     ii. The sum of all I_{OL} may not exceed 100 mA for ports A0 - A7, C4 - C7, and G2.
     iii. The sum of all I_{OL} may not exceed 100 mA for ports B0 - B7, E0 - E7, and G3 - G5.
     iv. The sum of all I_{OL} may not exceed 100 mA for ports D0 - D7, C0 - C3, and G0 - G1.
     v. The sum of all I_{OL} may not exceed 100 mA for ports F0 - F7.

     If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all I_{OH} may not exceed 400 mA for all ports.
     ii. The sum of all I_{OH} may not exceed 100 mA for ports A0 - A7, C4 - C7, and G2.
     iii. The sum of all I_{OH} may not exceed 100 mA for ports B0 - B7, E0 - E7, and G3 - G5.
     iv. The sum of all I_{OH} may not exceed 100 mA for ports D0 - D7, C0 - C3, and G0 - G1.
     v. The sum of all I_{OH} may not exceed 100 mA for ports F0 - F7.

     If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not ensured to source current higher than the listed test condition.
5. **These values are based on characterization. The maximum limit in production can, therefore, not be assured.**

3.4.2 Power-Down Specification Limit (T_A = -40°C to 85°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Table 3-5. ATmega329P DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.5	0.75	mA
		Active 4 MHz, V_{CC} = 3V		2.6	3.5	
		Active 8 MHz, V_{CC} = 5V		9.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.14	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.75	1.5	
		Idle 8 MHz, V_{CC} = 5V		2.9	5.0	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		1.0		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.7	15.0	
		WDT disabled, V_{CC} = 3V		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' **on page 43**.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 3-6. ATmega3290P DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.5	0.75	mA
		Active 4 MHz, V_{CC} = 3V		2.6	3.5	
		Active 8 MHz, V_{CC} = 5V		9.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.14	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.75	1.5	
		Idle 8 MHz, V_{CC} = 5V		2.9	5.0	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		1.0		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.7	15.0	
		WDT disabled, V_{CC} = 3V		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' **on page 43**.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

3.5 Electrical Characteristics – TA = -40°C to 105°C

3.5.1 Analog Input Offset Voltage (T_A = -40°C to 105°C)

A clarification has been made for the "*Analog Comparator Input Offset Voltage*" in the following table.

Table 3-7. T_A = -40°C to 105°C, VCC = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage except XTAL1 and $\overline{\text{RESET}}$ pins	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	-0.5 -0.5		$0.2V_{CC}$(1) $0.3V_{CC}$(1)	V
V_{IL1}	Input low voltage XTAL1 pins	V_{CC} = 1.8-5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IL2}	Input low voltage, $\overline{\text{RESET}}$ pins	V_{CC} = 1.8-5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IH}	Input high voltage except XTAL1 and $\overline{\text{RESET}}$ pins	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	$0.7V_{CC}$(2) $0.6V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH1}	Input high voltage, XTAL1 pin	V_{CC} = 1.8-2.4V V_{CC} = 2.4-5.5V	$0.8V_{CC}$(2) $0.7V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH2}	Input high voltage, $\overline{\text{RESET}}$ pins	V_{CC} = 1.8-5.5V	$0.9V_{CC}$(2)		V_{CC} + 0.5	
V_{OL}	Output low voltage(3), Port A, C, D, E, F, G	I_{OL} = 10 mA, V_{CC} = 5V I_{OL} = 5 mA, V_{CC} = 3V			0.7/1.0(5) 0.5/0.7(5)	
V_{OL1}	Output low voltage(3), Port B	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.7/1.0(5) 0.5/0.7(5)	
V_{OH}	Output high voltage(4), Port A, C, D, E, F, G	I_{OH} = -10 mA, V_{CC} = 5V I_{OH} = -5 mA, V_{CC} = 3V	4.2 2.3			
V_{OH1}	Output high voltage(4), Port B	I_{OH} = -20 mA, V_{CC} = 5V I_{OH} = -10 mA, V_{CC} = 3V	4.2 2.3			
I_{IL}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin high (absolute value)			1	
R_{RST}	Reset pull-up resistor		20		60	kΩ
R_{PU}	I/O Pin pull-up resistor		20		50	
V_{ACIO}	Analog comparator input offset voltage	V_{CC} =5V V_{in} = V_{CC}/2		< 10	40	mV
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} < 3.6V** **V_{in} < 0.5V**		**<15**	**60(6)**	**mV**
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} > 3.6V** **V_{in} < 0.5V**		**<15**	**500(6)**	**mV**
I_{ACLK}	Analog comparator	V_{CC} = 5V V_{in} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low.
2. "Min" means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC}= 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), the following must be observed.
   - TQFP and QFN/MLF Package:
     i. The sum of all I_{OL} may not exceed 400 mA for all ports.
     ii. The sum of all I_{OL} may not exceed 100 mA for ports A0 - A7, C4 - C7, and G2.
     iii. The sum of all I_{OL} may not exceed 100 mA for ports B0 - B7, E0 - E7, and G3 - G5.
     iv. The sum of all I_{OL} may not exceed 100 mA for ports D0 - D7, C0 - C3, and G0 - G1.
     v. The sum of all I_{OL} may not exceed 100 mA for ports F0 - F7.

     If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all I_{OH} may not exceed 400 mA for all ports.
     ii. The sum of all I_{OH} may not exceed 100 mA for ports A0 - A7, C4 - C7, and G2.
     iii. The sum of all I_{OH} may not exceed 100 mA for ports B0 - B7, E0 - E7, and G3 - G5.
     iv. The sum of all I_{OH} may not exceed 100 mA for ports D0 - D7, C0 - C3, and G0 - G1.
     v. The sum of all I_{OH} may not exceed 100 mA for ports F0 - F7.

     If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not ensured to source current higher than the listed test condition.
5. Largest value for ATmega329P and ATmega3290P.
6. **These values are based on characterization. The maximum limit in production can, therefore, not be assured.**

3.5.2 Power-Down Specification Limit (T_A = -40°C to 105°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Table 3-8. Current Consumption ATmega329P T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.4	0.85	mA
		Active 4 MHz, V_{CC} = 3V		2.3	3.8	
		Active 8 MHz, V_{CC} = 5V		9.0	14.0	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.3	
		Idle 4 MHz, V_{CC} = 3V		0.8	1.65	
		Idle 8 Hz, V_{CC} = 5V		3.1	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.6	1.8	µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.9	3.0	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7	20	
		WDT disabled, V_{CC} = 3V		0.2	5.0	

Notes:

1. All bits are set in the 'Power Reduction Register' **on page 43**.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 3-9. Current Consumption ATmega3290P T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.4	0.85	mA
		Active 4 MHz, V_{CC} = 3V		2.3	3.8	
		Active 8 MHz, V_{CC} = 5V		9.0	14.0	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.3	
		Idle 4 MHz, V_{CC} = 3V		0.8	1.65	
		Idle 8 MHz, V_{CC} = 5V		3.1	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.6	1.8	µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.9	3.0	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.0	20	
		WDT disabled, V_{CC} = 3V		0.2	5.0	

Notes:

1. All bits are set in the 'Power Reduction Register' **on page 43**.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	4/2023	Initial document release. • Content moved from the data sheet and restructured to the new document template • Updated the die revision list to reflect die revisions in production Silicon Errata added: • 2.2.1. Using BOD Disable Will Make the Device Reset • 2.3.1. Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer Data Sheet Clarifications added: • The Errata section in the data sheet is no longer valid • 3.2.1. Power Management and Sleep Modes • 3.3.1. Interrupt Vectors in ATmega329P/3290P • Electrical Characteristics – TA = -40°C to 85°C – 3.4.1. Analog Input Offset Voltage (TA = -40°C to 85°C) – 3.4.2. Power-Down Specification Limit (TA = -40°C to 85°C) • Electrical Characteristics – TA = -40°C to 105°C – 3.5.1. Analog Input Offset Voltage (TA = -40°C to 105°C) – 3.5.2. Power-Down Specification Limit (TA = -40°C to 105°C)

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ISBN: 978-1-6683-2349-6

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