

Product Overview

900 V, 80 A Power MOS 8 punch-through (PT) IGBT with co-packaged anti-parallel SiC diode, T-MAX®

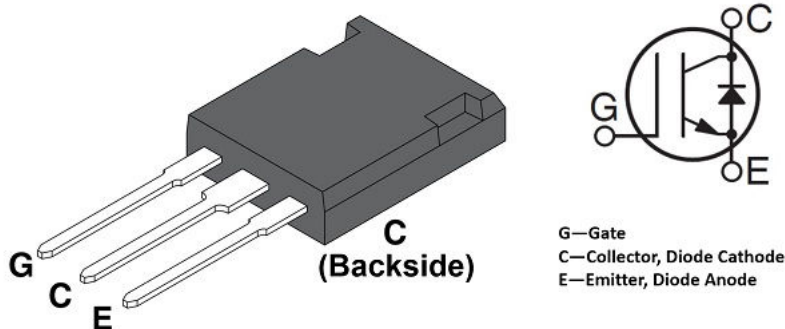


Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media	Qualification
APT80GA90B2SC50	T-MAX	Tube	Industrial

Features

- Low conduction loss and saturation voltage
- Low gate charge
- Ultrafast tail current shutoff
- No reverse recovery
- High operating frequency
- Switching safe operating area (SSOA) rated
- RoHS compliant
- Zero E_{on} switching loss from co-packaged, anti-parallel diode

1. Device Specifications: IGBT

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-emitter voltage	900	V
V_{GE}	Gate-emitter voltage	± 30	
I_{C1}	Continuous collector current ($T_C = 25\text{ }^\circ\text{C}$)	145	A
I_{C2}	Continuous collector current ($T_C = 110\text{ }^\circ\text{C}$)	80	
I_{CM}	Pulsed collector current ¹ ($T_C = 150\text{ }^\circ\text{C}$)	239	
SSOA	Switching safe operating area ($T_J = 150\text{ }^\circ\text{C}$, 900 V)	239	
P_D	Total power dissipation	625	W

Note:

1. Repetitive rating: Pulse width and case temperature limited by the maximum junction temperature.

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance (IGBT)			0.14	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-case thermal resistance (diode)		0.24	0.35	
T_J, T_{STG}	Operating and storage junction temperature range	-55		150	$^\circ\text{C}$
T_L	Lead temperature for 10 seconds			300	
Wt	Package weight		6.2		g

1.3 Electrical Performance

The following table shows the static characteristics of this device. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}, I_G = 1.0\text{ mA}$	900			V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 1.0\text{ mA}$	3	4.5	6	V
$V_{CE(on)}$	Collector-emitter on voltage	$V_{GE} = 15\text{ V}, I_C = 47\text{ A}$		2.5	3.1	
		$V_{GE} = 15\text{ V}, I_C = 47\text{ A}, T_J = 125\text{ }^\circ\text{C}$		2.2		
I_{CES}	Collector cut-off current ¹	$V_{CE} = 900\text{ V}, V_{GE} = 0\text{ V}$			450	μA
		$V_{CE} = 900\text{ V}, V_{GE} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			2000	
I_{GES}	Gate-emitter leakage current	$V_{GE} = \pm 30\text{ V}$			± 100	nA

Note:

1. I_{CES} includes both IGBT and diode leakages.

The following table shows the dynamic characteristics of this device. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit	
C_{ies}	Input capacitance	$V_{GE} = 0\text{ V}, V_{CE} = 450\text{ V}, f = 1\text{ MHz}$		4560		pF	
C_{res}	Reverse transfer capacitance			62			
C_{oes}	Output capacitance			411			
V_{GEP}	Gate-to-emitter plateau voltage			6			V
Q_G	Total gate charge ¹	$V_{GE} = 15\text{ V}, V_{CE} = 50\text{ V}, I_C = 47\text{ A}$		200		nC	
Q_{GE}	Gate-emitter charge			30			
Q_{GC}	Gate-collector ("Miller") charge			72			
SSOA	Switching safe operating area	$T_J = 150\text{ }^\circ\text{C}, R_G = 4.7\text{ }\Omega, V_{GE} = 15\text{ V}, V_{CE} = 900\text{ V}, L = 100\text{ }\mu\text{H}$	239			A	
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}, V_{GE} = 15\text{ V}, I_C = 47\text{ A}, R_G = 4.7\text{ }\Omega, T_J = 25\text{ }^\circ\text{C}$		18		ns	
t_r	Current rise time			29			
$t_{d(off)}$	Turn-off delay time			149			
t_f	Current fall time			85			
E_{on}	Turn-on switching energy ²			1322			μJ
E_{off}	Turn-off switching energy ³			1389			
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}, V_{GE} = 15\text{ V}, I_C = 47\text{ A}, R_G = 4.7\text{ }\Omega, T_J = 125\text{ }^\circ\text{C}$		18		ns	
t_r	Current rise time			31			
$t_{d(off)}$	Turn-off delay time			192			
t_f	Current fall time			128			
E_{on}	Turn-on switching energy ²			1337			μJ
E_{off}	Turn-off switching energy ³			2082			

Notes:

1. See MIL-STD-750 Method 3471.
2. E_{on} is the clamped inductive turn-on-energy of this device; there is no contribution to E_{on} from the SiC diode. (See Figures 1-21, 1-22.)
3. E_{off} is the clamped inductive turn-off energy measured in accordance with JEDEC standard JESD24-1. (See Figures 1-21, 1-23.)

1.4 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Output Characteristics

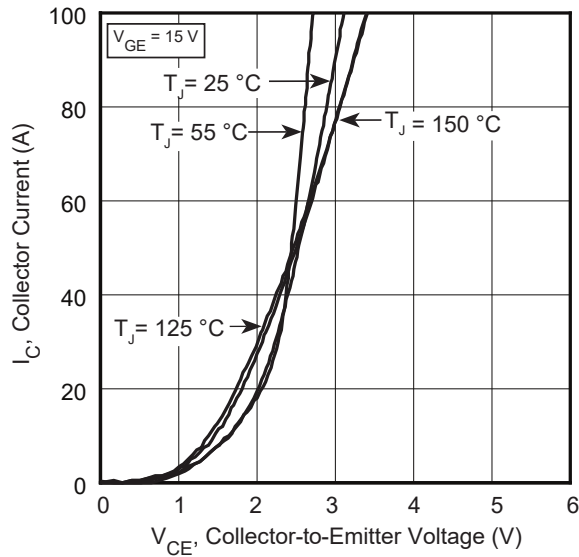


Figure 1-2. Output Characteristics

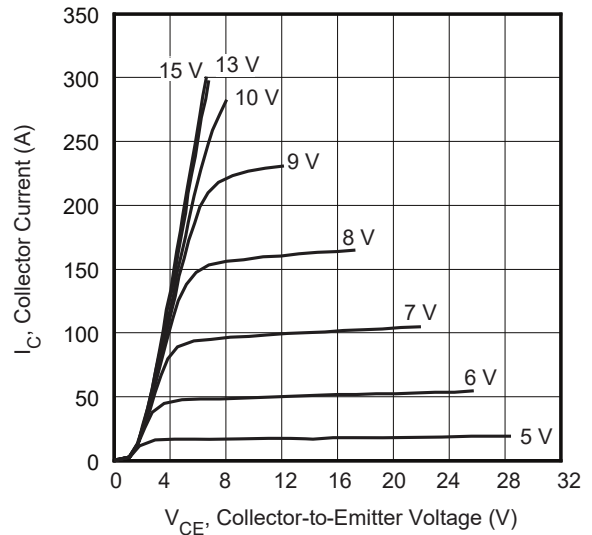


Figure 1-3. Transfer Characteristics

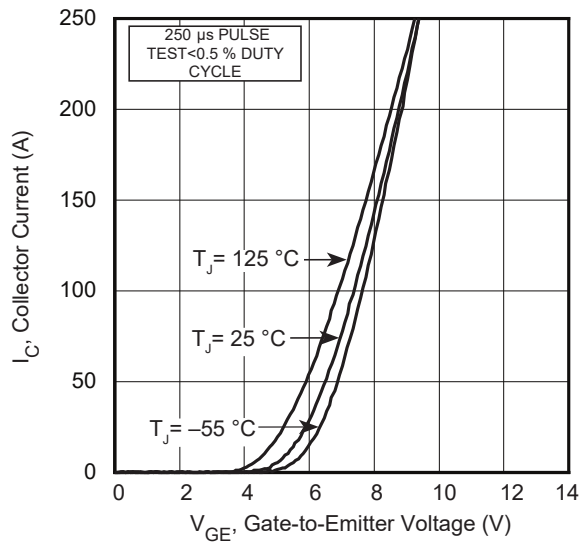


Figure 1-4. Gate Charge

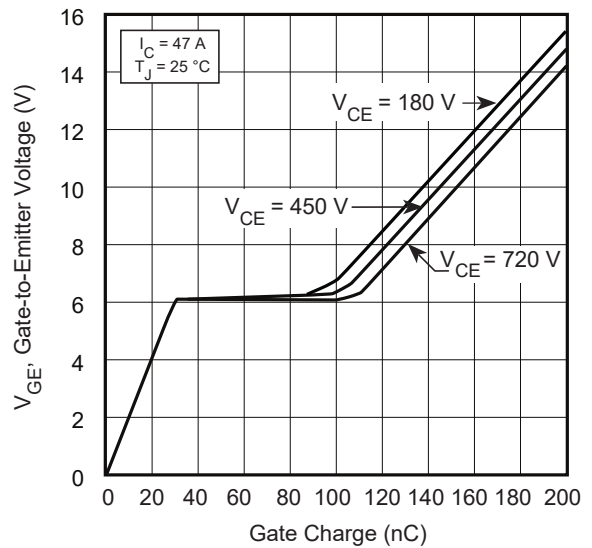


Figure 1-5. On-State Voltage vs. Gate-to- Emitter Voltage

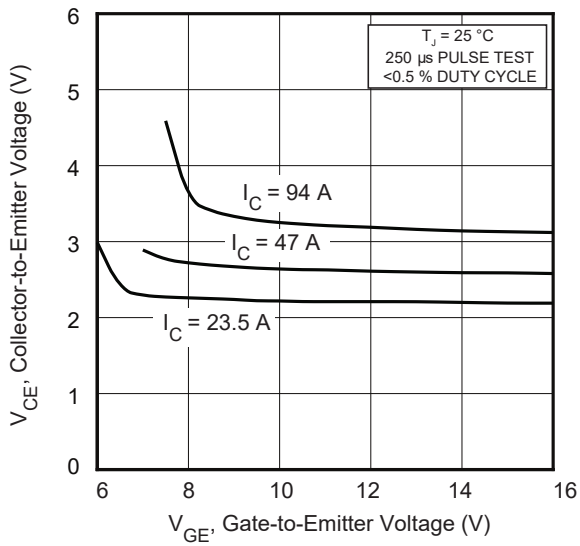


Figure 1-6. On-State Voltage vs. Junction Temperature

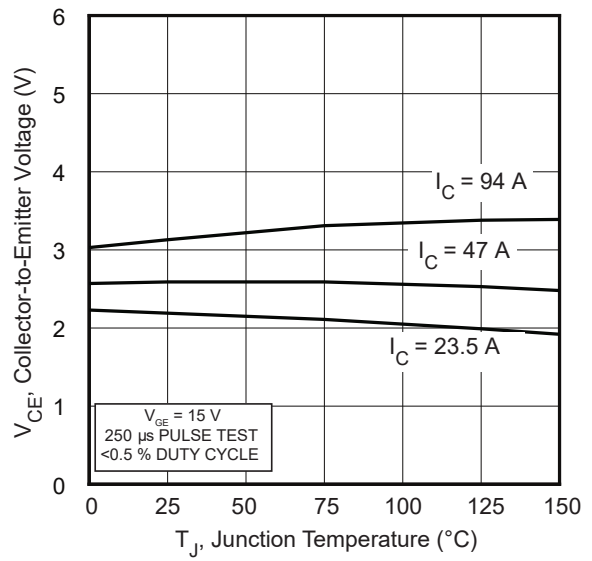


Figure 1-7. Threshold Voltage vs. Junction Temperature

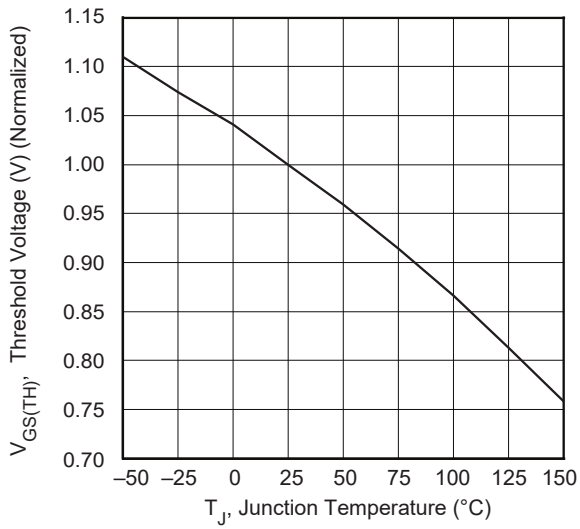


Figure 1-8. DC Collector Current vs. Case Temperature

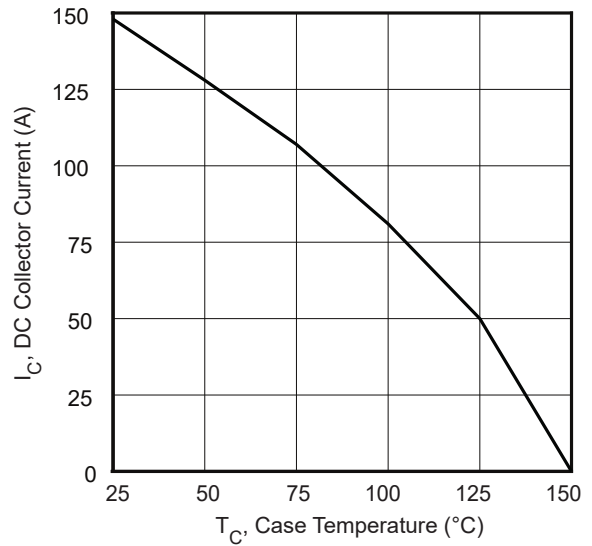


Figure 1-9. Turn-On Delay Time vs. Collector Current

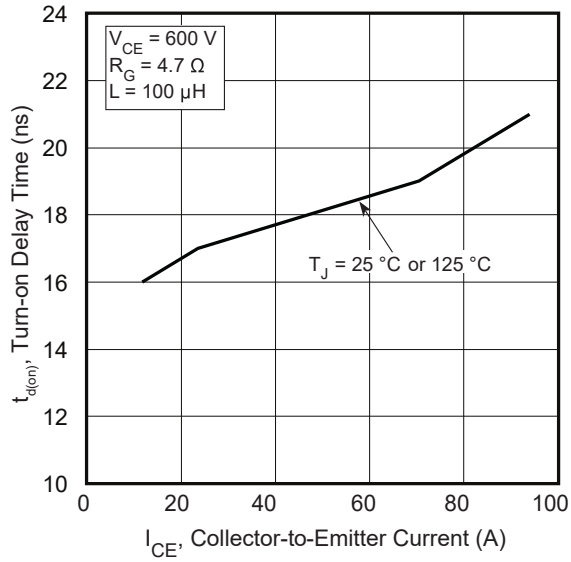


Figure 1-10. Turn-Off Delay Time vs. Collector Current

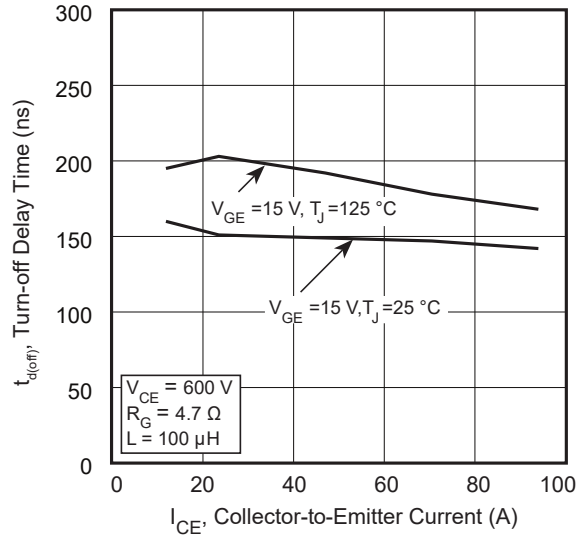


Figure 1-11. Current Rise Time vs. Collector Current

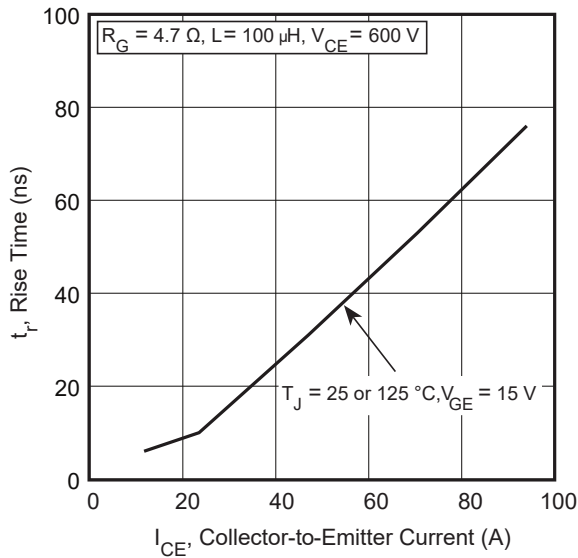


Figure 1-12. Current Fall Time vs. Collector Current

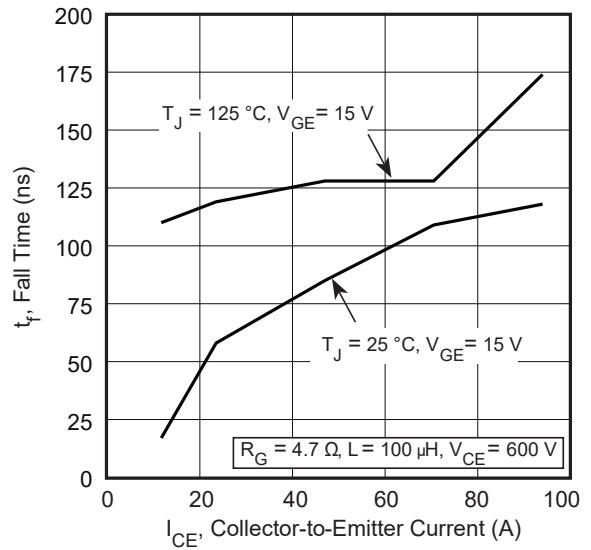


Figure 1-13. Turn-On Energy Loss vs. Collector Current

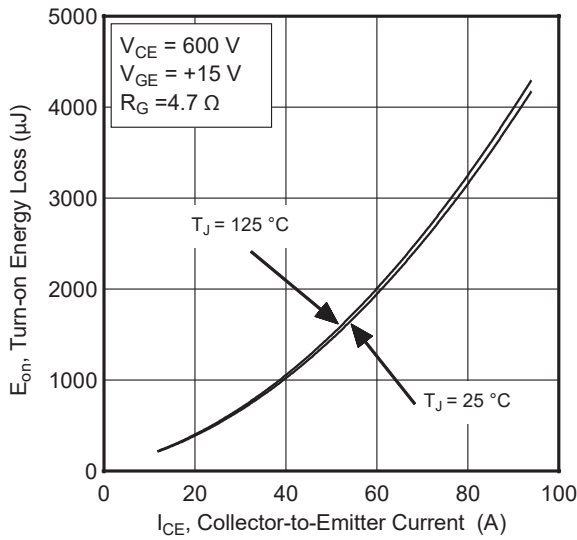


Figure 1-14. Turn-Off Energy Loss vs. Collector Current

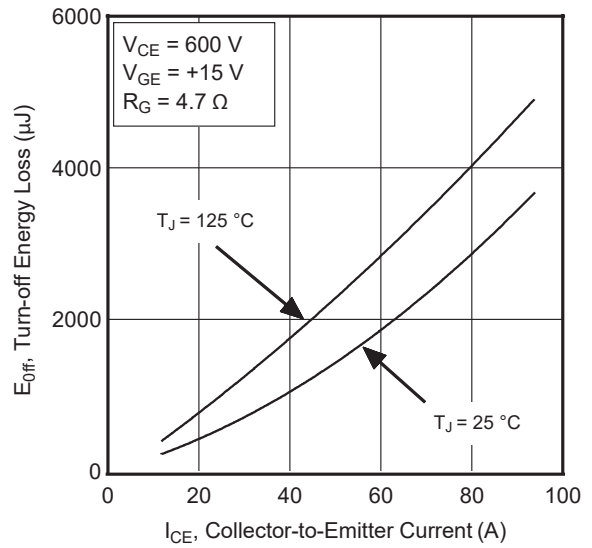


Figure 1-15. Switching Energy Losses vs. Gate Resistance

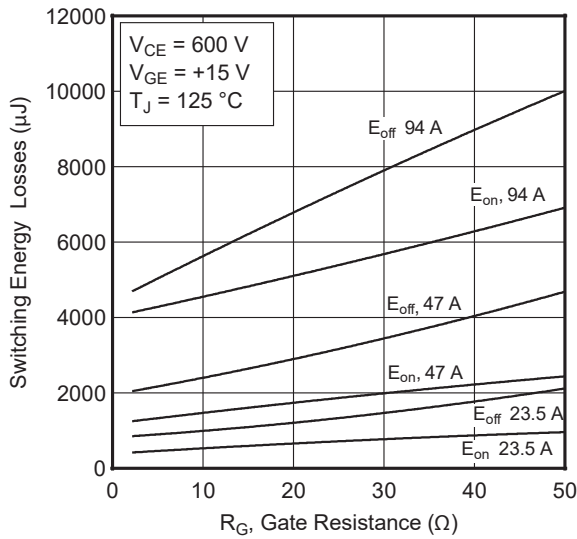


Figure 1-16. Switching Energy Losses vs. Junction Temperature

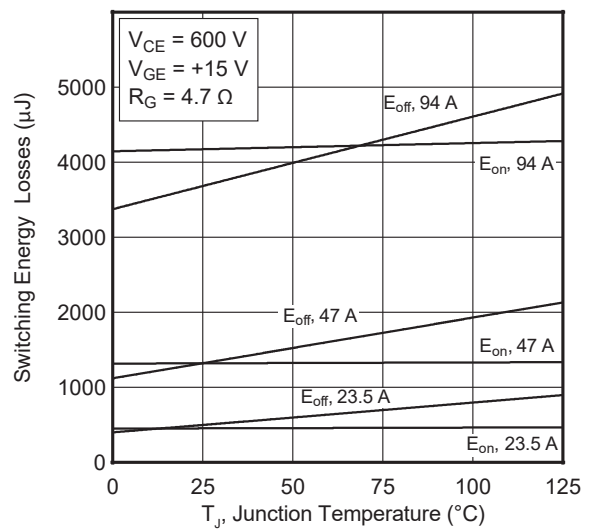


Figure 1-17. Capacitance vs. Collector-To-Emitter Voltage **Figure 1-18. Switching Safe Operating Area**

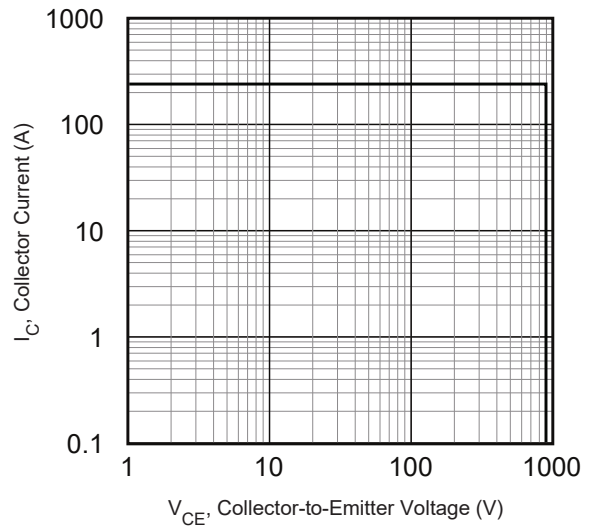
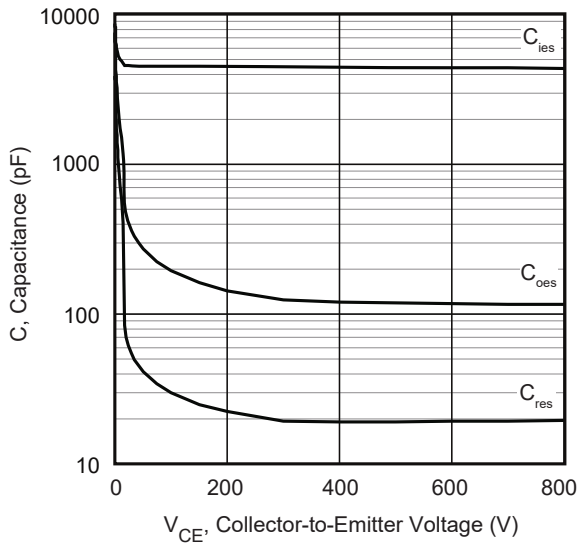


Figure 1-19. Maximum Transient Thermal Impedance

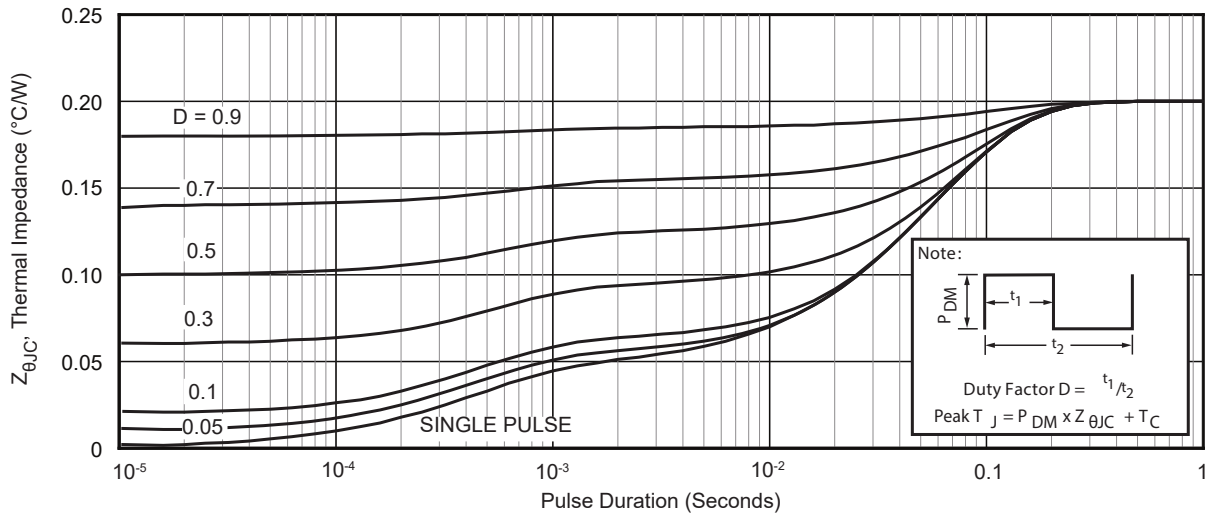


Figure 1-20. Transient Thermal Impedance Model

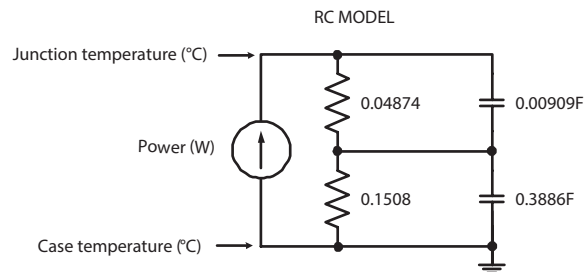


Figure 1-21. Inductive Switching Test Circuit

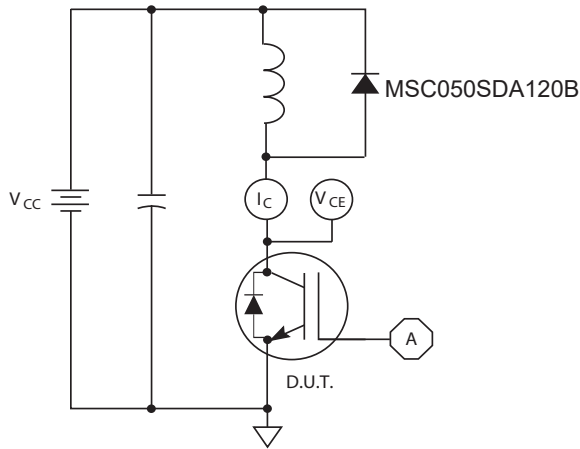


Figure 1-22. Turn-on Switching Waveform and Definitions

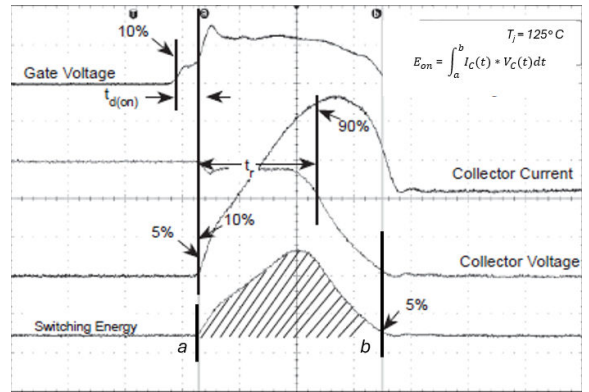
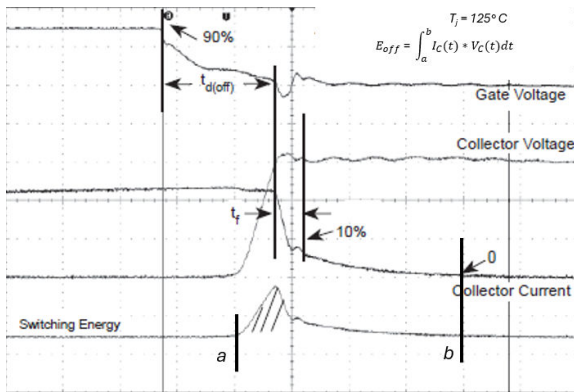


Figure 1-23. Turn-off Switching Waveform and Definitions



2. Device Specifications: Zero-Recovery SiC Anti-Parallel Diode

This section shows the specifications of the co-packaged, anti-parallel diode.

2.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the anti-parallel diode. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_F	Maximum DC forward current ($T_C = 25\text{ }^\circ\text{C}$)	109	A
	Maximum DC forward current ($T_C = 135\text{ }^\circ\text{C}$)	49	
	Maximum DC forward current ($T_C = 145\text{ }^\circ\text{C}$)	41	
I_{FRM}	Repetitive peak forward surge current ($t_p = 8.3\text{ ms}$, half sine wave)	154	
I_{FSM}	Non-repetitive forward surge current ($t_p = 8.3\text{ ms}$, half sine wave)	290	
P_{TOT}	Total power dissipation ($T_C = 25\text{ }^\circ\text{C}$)	429	W
	Total power dissipation ($T_C = 110\text{ }^\circ\text{C}$)	186	

2.2 Electrical Performance

The following table shows the static characteristics of the anti-parallel diode.

Table 2-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_F	Forward voltage	$I_F = 50\text{ A}$, $T_J = 25\text{ }^\circ\text{C}$		1.5	1.8	V
		$I_F = 50\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$		2.1		

2.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 2-1. Maximum Transient Thermal Impedance

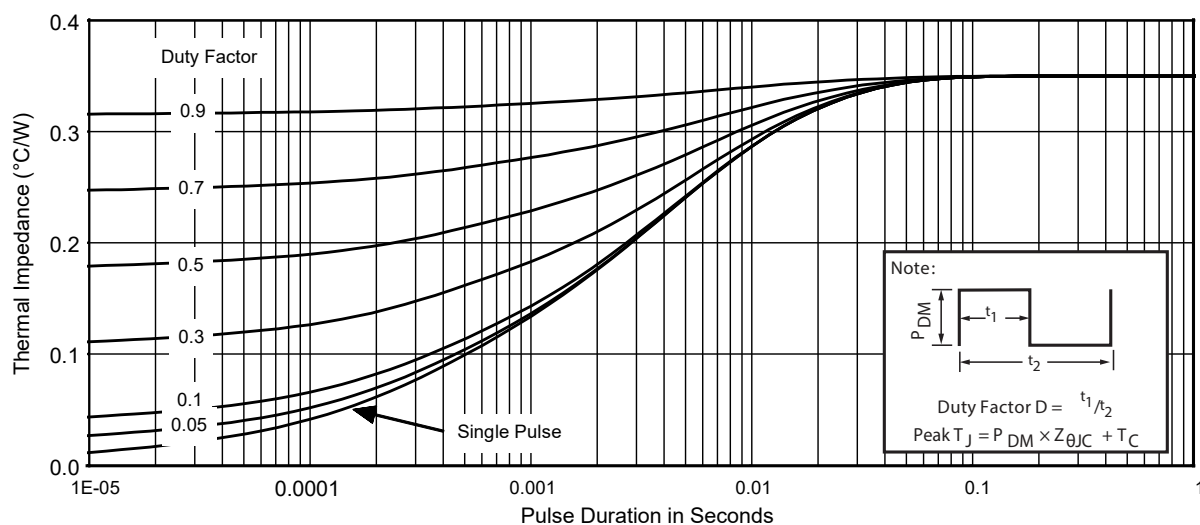


Figure 2-2. Forward Current vs. Forward Voltage

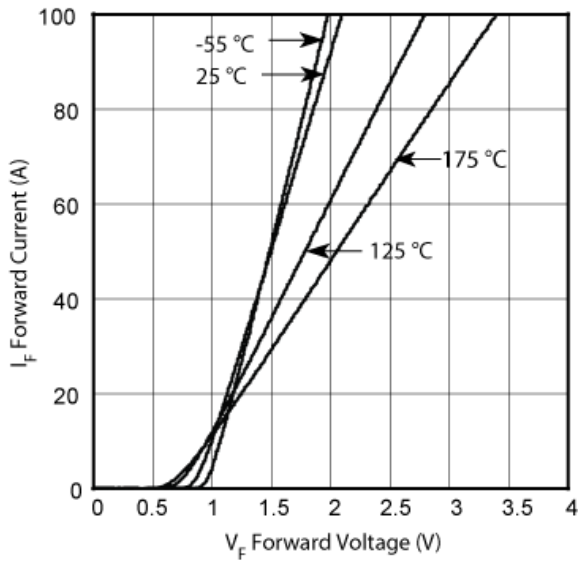


Figure 2-3. Max. Forward Current vs. Case Temp.

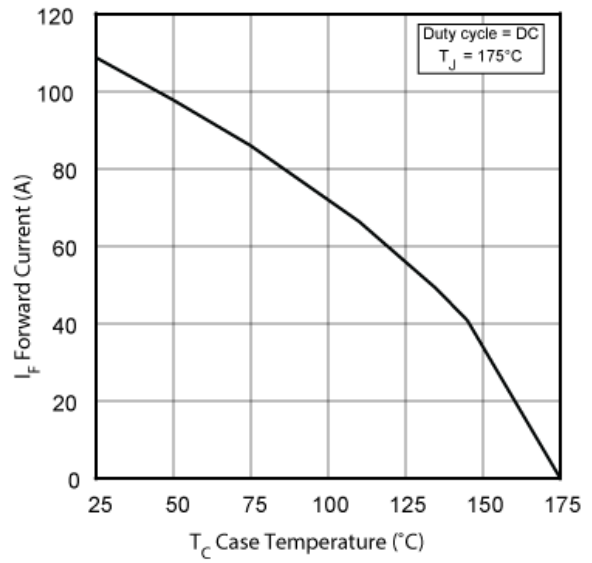


Figure 2-4. Max. Power Dissipation vs. Case Temp.

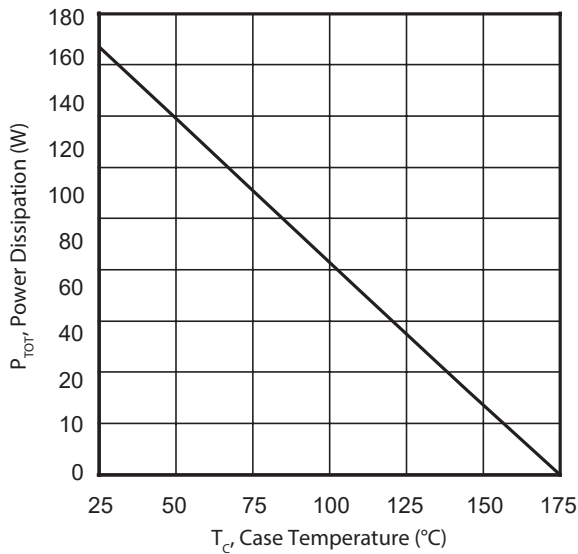


Figure 2-5. Total Capacitive Charge vs. Reverse Voltage

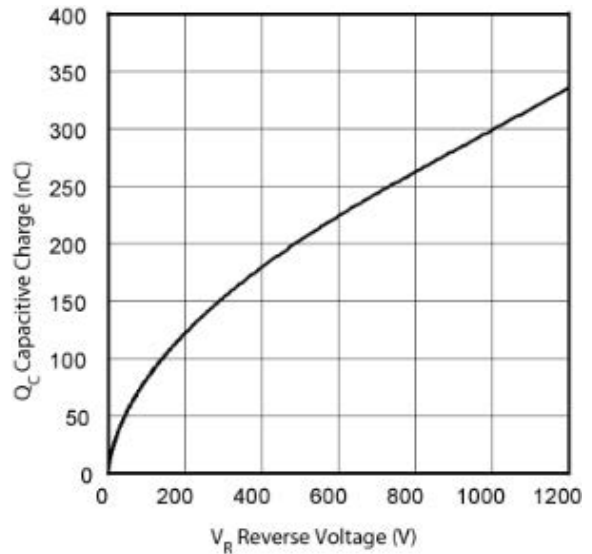
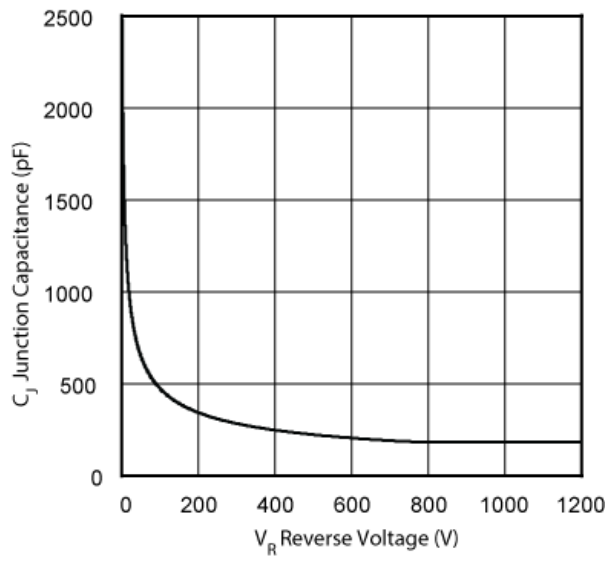


Figure 2-6. Junction Capacitance vs. Reverse Voltage

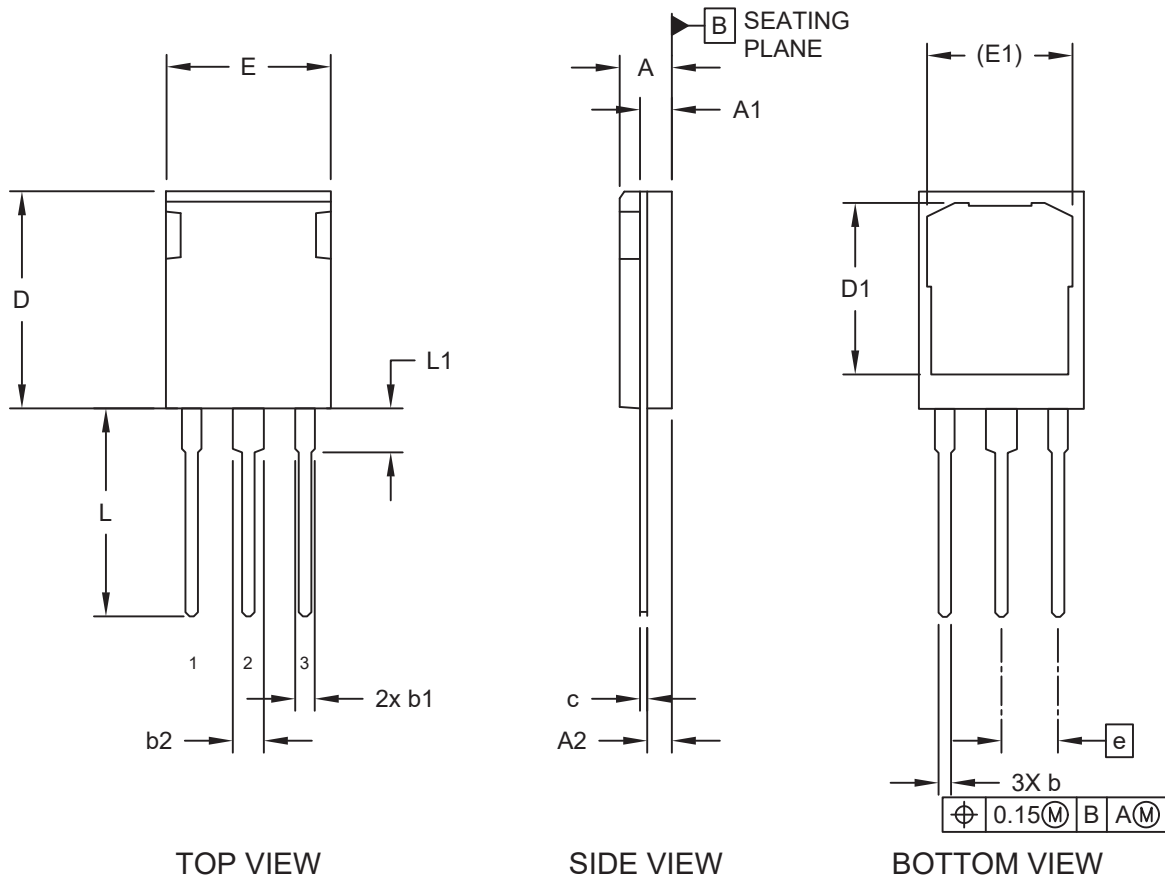
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the T-MAX package outline of this device.

Figure 3-1. Package Outline Drawing



The following table shows the T-MAX dimensions and should be used in conjunction with the package outline drawing.

Table 3-1. T-MAX Dimensions

Dimension Limits		Dimensions (mm)	
		Min.	Max.
Number of leads	N		3
Pitch	e		5.44 BSC
Overall height	A	4.70	5.31
Tab height	A1	1.50	2.49
Seating plane to lead	A2	2.21	2.59
Lead width	b	1.02	1.40
Lead shoulder width (x2)	b1	1.65	2.41
Lead shoulder width	b2	2.87	3.38
Lead thickness	c	0.41	0.79

Table 3-1. T-MAX Dimensions (continued)

Dimension Limits		Dimensions (mm)	
		Min.	Max.
Lead length	L	19.81	20.32
Lead shoulder length	L1	3.99	4.50
Molded body length	D	20.80	21.46
Thermal pad length	D1	16.25	17.65
Total width	E	15.49	16.26
Thermal pad width	E1	13.10	14.50

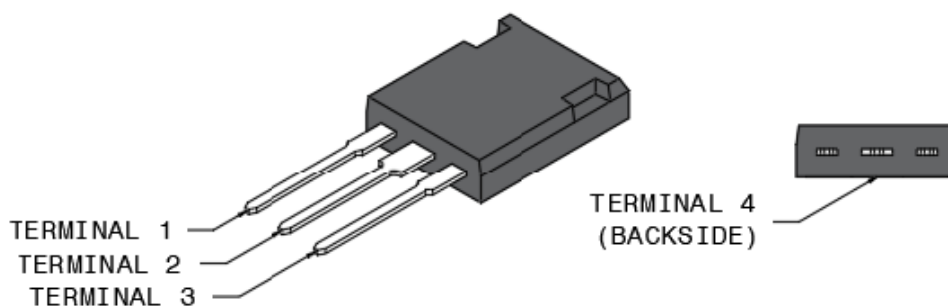
Note:

1. Dimensioning and tolerancing per ASME Y14.5M.

3.2 Terminal Pinout

The following figure illustrates the terminal pinout of this device.

Figure 3-2. Terminal Pinout



The following table shows the electrical signal terminal pinout of this device.

Table 3-2. Electrical Signal Terminal Pinout

Terminal	Definition
TERMINAL 1	Gate
TERMINAL 2	Collector, Diode Cathode
TERMINAL 3	Emitter, Diode Anode
TERMINAL 4	Collector, Diode Cathode

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	02/2025	Document created.

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