

Designing High-Performance Flyback Converters with the HV9110 and HV9120

Introduction

Although the HV91XX family of PWM ICs can be used to control single-switch converters of any topology or size, their primary usage is in low-cost, low to medium power, discontinuous-mode flyback converters. Designing such converters is relatively simple and quick if one has a basic understanding of how a flyback converter functions. It is the purpose of this note to provide such an understanding, and to illustrate, with a couple of examples, one way in which such a converter design can proceed. It should be noted that this is an engineering approach, meant to allow the user to develop a working design quickly, not a textbook approach meant to teach underlying theory. Safety margins are taken into account, and the path taken through the design is intended to make these margins work with each other in order to generate an economical and producible power supply. Many apparently arbitrary values are used. They are arbitrary, and different ones could have been used that would have resulted in different power supplies, that would have been, for whatever feature was optimized, just as valid as the examples chosen.

On Flyback Function

A flyback converter functions, as does almost every other switchmode converter, by storing energy in an inductor during a main switch ON period, then discharging the stored energy into a load during the switch's OFF period. The trickiness to this (if there is any) is that the inductor has two or more windings, (an input winding and one or more output windings) and that the current flow alternates between the input and output windings, with effectively no current (other than a little leakage) flowing in the nonconducting winding while its partner carries the current.

The way a flyback converter works can lead to some confusion if the designer tries to approach the design of its magnetic as if it were a transformer, because, except for the case of multiple output windings, the magnetic in a flyback converter is NOT a transformer. Perhaps the easiest way to view the magnetic in a flyback converter is as an energy bucket which is alternately filled (when the main switch is ON) and dumped (when the switch is OFF). A flyback magnetic is NOT a transformer despite its superficial resemblance to one: A transformer functions as a voltage-in, voltage-out power transfer device, where input and output windings

conduct simultaneously. A flyback magnetic is an energy-in, energy-out power transfer device where the input and output windings do not conduct current simultaneously. Obviously, voltages present on the active winding are reflected, by the turns ratio, to the inactive winding, but the old saw "The voltage on the main switch is twice the input voltage" is incorrect, because the voltage reflected from the output winding can be either higher or lower than the input voltage (generally it is lower) depending on the voltage at the output, and the time allotted for the output inductance to discharge into it. Discontinuous-mode operation merely means that all the energy (neglecting losses) put into the coupled inductor during one time period when the main switch is ON is then emptied out during the following period when the main switch is OFF. No energy is carried forward to a subsequent cycle. (See Figure 1.)

For both converter and magnetic design, a flyback magnetic can be thought of as two independent inductors which share a common core. Once the designer is accustomed to thinking of the flyback magnetic as a dual inductor, the rest of the design becomes easier.

What the designer needs to do is define the output side inductor so that it delivers enough energy to the load, while the switch is off, to produce the desired current at the desired voltage. Next, define the input side of the inductor so that it takes in enough energy when the switch is on to provide for both the output and system losses. To facilitate this, a conversion formula is necessary:

$$I_{AVG} = \frac{1}{2} \cdot \frac{t_{ON}}{t_{PERIOD}} \cdot I_{PK}$$

This formula converts peak to DC average of noncontiguous triangle waves.

If we deal with ON time as a percent of total clock period, (duty cycle) and define:

$$D = \frac{t_{ON}}{t_{PERIOD}}; 1 - D = \frac{t_{OFF}}{t_{PERIOD}}$$

the formula reduces to:

$$I_{AVG} = \frac{1}{2} \cdot D \cdot I_{PK} \quad \text{for the input side}$$

$$I_{AVG} = \frac{1}{2} \cdot (1 - D) \cdot I_{PK} \quad \text{for the output side}$$

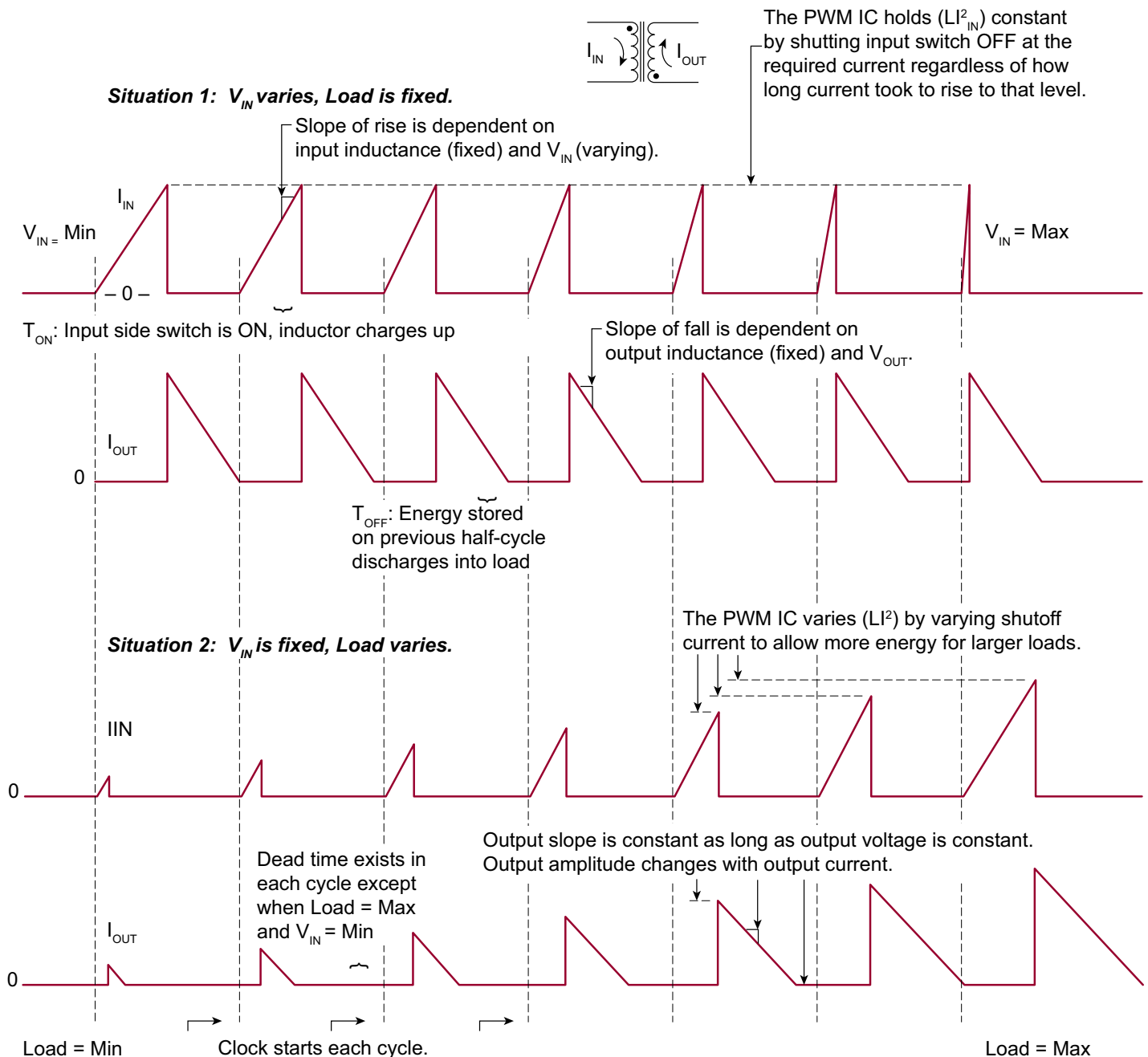
Because the designer knows the length of time the switch

will be ON and OFF (these are defined by the clock frequency and the PWM IC used) as well as the input and output voltages desired, the peak currents found from the formulae can be used with the defining formula for inductance:

$$E = L \cdot (di/dt)$$

to determine the required inductances for the input and output sides of the coupled inductor. In the process, the rest of the design generally falls into place.

Figure 1 - The “Energy Bucket”



Data Needed to Start the Design

1. Minimum and Maximum Input Voltage
2. Nominal Output Voltage(s) and Tolerance(s)
3. Maximum Output Wattage
4. Minimum Output Wattage
5. Maximum Allowable Output Ripple
6. A defined clock frequency
7. A list of mechanical and thermal constraints (if any)

Operating Frequency

Most designers approach converter design with the idea of operating at the highest possible frequency that is convenient. This is generally a useful approach, because it minimizes the size and cost of output capacitors and the coupled inductor. However, it is not always the best way to choose a frequency. In the case of low-power converters, once the magnetics are reduced in size to a vendor-dependent minimum, further reductions in size will raise the cost of the magnetics. Very small cores and ultra-fine wire are hard to handle.

There is another important consideration in the choice of frequency that is often overlooked: dynamic range. If the difference between the widest pulse a PWM IC can generate (which is a function of its operating frequency) and the narrowest pulse it can produce (a function of the PWM IC's speed and internal structure) is small, the ratio between

$P_{OUT(MAX)}$ at low line and $P_{OUT(MIN)}$ at high line must also be small, or reducing the size of the inductor and output filters will be paid for by increasing the size and cost of the EMI filter. Further, if the PWM IC selected cannot handle the full range of pulse widths required, it will start cycle-skipping (failing to turn on at all for some cycles).

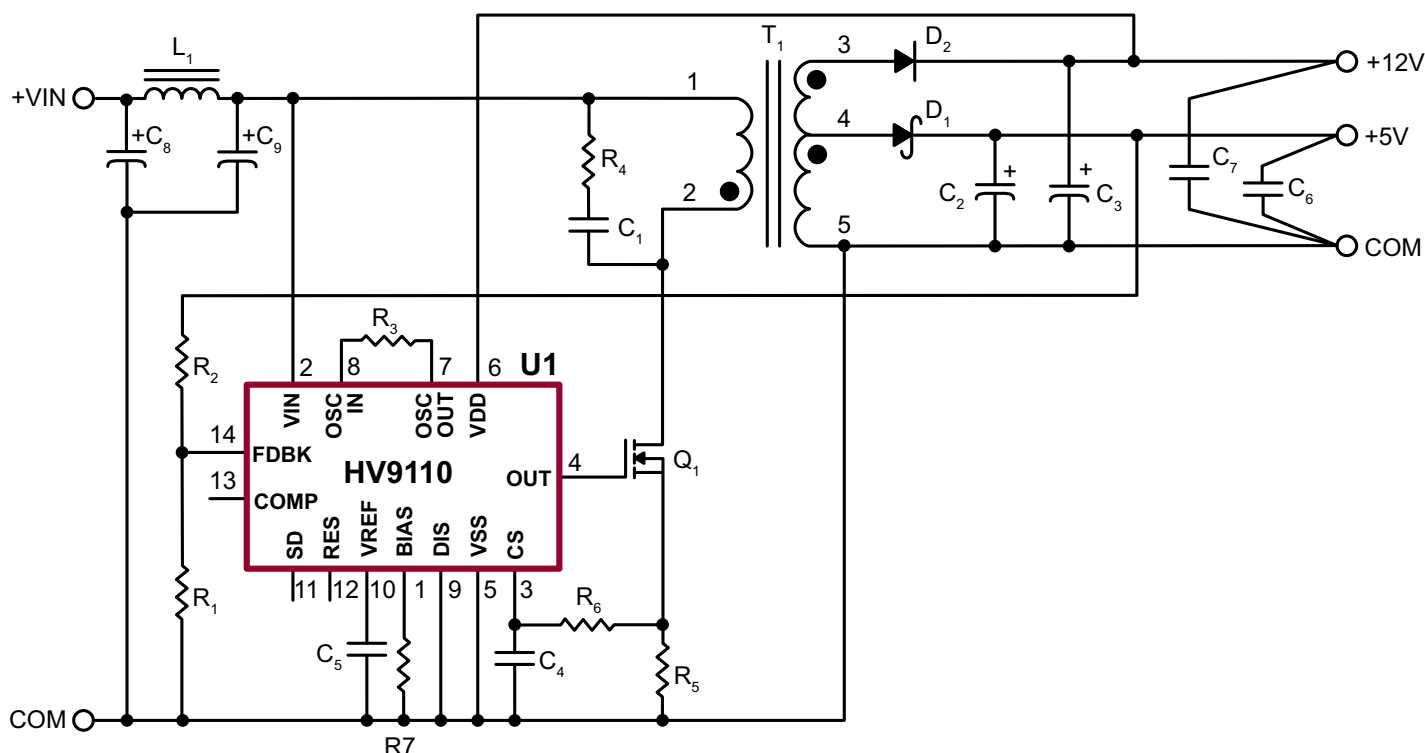
While most PWM ICs, including the HV91XX family, can simply skip cycles by not turning on at all, if the differential between V_{IN} and P_{OUT} becomes too great, skipping cycles reduces the effective clock frequency of the converter, and redefines the minimum frequency for which the input EMI filter must be designed. For example, if the converter skips every other cycle at high line/light load, the size (and cost) of the EMI filter can be doubled.

Cycle skipping also increases either the size of the output capacitors or the amount of ripple on the converter's output.

Recently, dynamic range has been overlooked because most bipolar PWMs do not have a wide dynamic range. For example, a bipolar 1845 PWM operating at 50kHz has a dynamic range of only $\approx 17.6:1$. A CMOS 9110, in contrast, has a dynamic range of $>120:1$ at 50kHz. Proper use of dynamic range can have a significant effect on EMI filter cost.

Another consideration in choosing an optimal frequency is switching power loss, which increases linearly with frequency in non-resonant converters.

Figure 2



Example 1

A 48W converter patterned after an instrument power supply. This will be a simple generic example with no bells and whistles. First, we need the input parameters listed below:

Maximum Input Voltage: 65VDC

Minimum Input Voltage: 18VDC

Outputs: A: 5.0V, $\pm 1\%$, 0.25 to 8A, 25mV ripple

B: 12.0V, $\pm 5\%$, 0.01 to 0.7A, 0.5V ripple

Maximum Output Wattage: 48.4W

Minimum Output Wattage: 1.37W

Operating Frequency: 50KHz

(See Figure 2.)

An HV9110, which will accept input voltages of up to 120V is used. As previously noted, this chip will allow a dynamic range sufficient to handle the stated line/load variations at 50kHz. Setting the clock frequency requires selecting an appropriate timing resistor. From a graph on the data sheet, the appropriate resistor for 50kHz operation is $\approx 330\text{k}\Omega$. This however does not account for the tolerance of either the resistor or the chip. To ensure that all device-resistor combinations operate at or above 50kHz, $261\text{k}\Omega$ is a better choice. The reason that the clock frequency should be set to a minimum rather than a nominal value, despite the reduction in dynamic range this causes, is to prevent the slowest converter from saturating its coupled inductor. While magnetic saturation does not cause damage in a current-mode converter as it would in a voltage-mode converter, it still causes additional dissipation and stress on the main switch. It can also limit power throughput.

The Design

First, translate the average current of the major output winding at maximum load to a peak current. From the data sheet for the HV9110 it can be seen that maximum ON time for a cycle is 50% minus approximately 150 ns. At 50kHz, this amounts to a little over 49%. We can declare a maximum duty cycle (D) of 0.49 and allow a small safety margin. If DMAX is .49, then minimum 1-D is 0.51. Using 0.50 as a value for 1-D (thus allowing a 1% overall dead band as safety margin) determine peak secondary current:

$$I_{PK(5V)} = \frac{2 \cdot 8.0A}{0.50} = 32.0A$$

This value will also be used to determine the actual voltage required of the winding, which is the output voltage plus the

drop in the output diode:

$$V_{WINDING} = V_{OUTPUT} + V_{F(DIODE)}$$

Also, repeat this procedure for each auxiliary output winding as an aid in determining the real voltage required of these windings:

$$I_{PK(12V)} = \frac{2 \cdot 0.7A}{0.50} = 2.8A$$

Next calculate minimum t_{OFF} , which will be 50% of the maximum PWM oscillator frequency. Using a 261k timing resistor, maximum frequency should be $\leq 67\text{kHz}$, which gives a t_{PERIOD} of $\geq 14.9\mu\text{s}$, and a $t_{OFF(MIN)}$ of $7.46\mu\text{s}$.

Next, we need to generate an estimate of instantaneous forward drop of the diode on the main output. We cannot actually choose a diode until we know what its reverse voltage needs to be, which will not be known until input side inductance is calculated. 0.8V should be a reasonable estimate. This voltage is added to the 5.0V output voltage to determine the actual voltage on the main output winding (5.8V in this instance).

Knowing the peak current and voltage of the output winding and the minimum t_{OFF} , we can calculate the inductance of the output winding from the defining equation for inductance, $E = L di/dt$.

$$5.8V \div (32A \div 7.46\mu\text{s}) = 1.35\mu\text{H}$$

The same procedure is used to calculate primary inductance. First we need to calculate the total power into the magnetic. This is the power out of the magnetic, plus the losses in the magnetic itself.

The power out of the magnetic is just the continuous output power of the converter, plus the losses in the output diodes. Use an average forward drop for the diodes for this step.

$$\begin{aligned} P_{OUT(5V)} &= 5.6V \cdot 8.0A = 44.8W \\ P_{OUT(12V)} &= 12.7V \cdot 0.7A = 8.89W \\ P_{OUT(TOTAL)} &= 44.8W + 8.89W = 53.69W \end{aligned}$$

The losses in a well-designed magnetic assembly, for a fixed frequency and power output, interestingly enough, depend primarily on the physical size of the magnetic. Smaller mag-

netics will be less efficient and run hotter. Larger magnetics will have less loss and run cooler. The effect is logarithmic, and means that no one will ever build a magnetic less than ³ 90% efficient, because the insulation required would burn up under normal operating conditions, and that very few people could accept a magnetic that is over 99% efficient, because the size would be prohibitively large. For a switchmode converter of the type described 95% to 97% efficiency will result in a reasonable magnetic size that is economical to build. Using an estimated magnetic efficiency of 96%, calculate input power (which is just output power divided by magnetic efficiency):

$$53.69W \div 0.96 = 55.93W$$

Next, determine the minimum voltage across the input winding. This is just the minimum input voltage to the converter, minus the drop across the switch and the current sensing resistor.

The drop across the current sensing resistor is easy to determine from the data sheet for the 9110. According to the data sheet, the voltage across the resistor should be slightly below 1.0V. If we minimum trip point for the current limiting section of the chip is 1.0V. This means that our maximum normal operating peak establish a maximum peak voltage that is much less than 1.0V, we will increase the distance between maximum normal operating current and the maximum guaranteed overcurrent trip point, which is 1.4V. Usually the best choice is to operate with a normal peak voltage across the current sense resistor very close to 1.0V, so 0.99V is a reasonable value. Note that this voltage drop across the current sensing resistor only occurs during current limit. In normal operation at loads below maximum, the trip point for the switch moves down to limit the energy going to the output. That is how this form of converter regulates.

The drop across the switch is more complicated, because first we have to choose a main switch. To do this we need an estimate of what the current will be. Generally a close enough estimate can be made using the wattage into the magnetic and an estimated minimum voltage across the winding. If we assume that the voltage across the switch will be no greater than 1.5V peak, we can subtract this voltage, and the current sense voltage, from the minimum input voltage and estimate average input current:

$$18V - (1.5V + 1V) = 15.5V$$

Dividing the previously determined input wattage to the inductor produces an average input current:

$$55.93W \div 15.5V = 3.61A$$

Dividing that by the average to peak conversion factor (based on $t_{ON} = 49\%$) gives us the peak current.

$$I_{SW(PK)} \cdot \frac{2 \cdot 3.61A}{0.49} = 14.74A$$

Dividing the previously assumed drop across the switch by the estimated peak current gives us a target $R_{DS(ON)}$ for the main switch:

$$1.5V \div 14.74A = 0.102\Omega$$

Power Dissipation in the switch may be calculated by:

$$P_{SW} = \frac{1}{3} \cdot D \cdot I_{PK}^2 \cdot R_{SW}$$

$$\frac{1}{3} \cdot 0.49 \cdot (14.74A)^2 \cdot 0.102\Omega = 36W$$

This is a fairly high loss, causing a 7% hit in efficiency. In other words, with no other losses, overall efficiency would be 93%. Choosing a transistor with lower on resistance would be prudent. The IRL2910S is a good choice, having an on resistance of 26m Ω . This corresponds to a 0.923W loss, contributing a 1.9% efficiency hit.

Aside

Obviously, by altering the estimated value for drop across the switch up or down one could change which switch ended up satisfying the circuit requirements. The end result does not change the design process, only the efficiency of final converter, and how much one pays for the switch. It is also possible to start the design with a main switch already selected or a mandatory efficiency goal, and just fill in the appropriate value for $R_{DS(ON)}$ when you get to that step of the process, but doing so may mean repeating that section of the calculations once or twice.

Similarly, one can specify different transformer efficiencies, if efficiency or volume is more than ordinarily important. Readers are cautioned, however, that magnetic efficiencies below 92% or over 98% may not result in a practical design.

By using the IRL2910S, our original estimate is close enough so there is no need to recalculate, and we can use the already calculated peak current to determine the value of current sensing resistor needed, which is simply:

$$V_{CURRENT\ SENSE} \div I_{PEAK} \text{ or } 0.99V \div 14.74A = 67m\Omega$$

The closest lower value is 66.5mΩ in 1%. A 68Ω in 5% values could also be used with small risk of a worst-case combination causing current limiting at less than 100% of normal output. To determine wattage we can use the same formula used to calculate switch loss.

$$\frac{1}{3} \cdot 0.49 \cdot (14.74A)^2 \cdot 66.5m\Omega = 2.36W$$

so a 3.0W resistor would work.

A Word on Current Sense Resistors

Obtaining a good current sensing resistor is still a problem. Most common resistors are not fit for this service because they are too inductive. What answer there is probably lies in bulk metal resistors, or noninductive resistors, but be careful. Some “noninductive” resistors are only “noninductive” at low frequencies, and can be the source of considerable error at high frequencies. Carbon film resistors and most metal film resistors are not recommended. Also, most of the low value resistors that look like carbon composition resistors are actually film or wirewound resistors in molded cases. 4-terminal resistors specifically meant for current sensing are for the most part wirewound, and meant only for DC, not switched current measurements. Be sure to test the inductance of the resistor you intend to use before you install it in your circuit! Also, even a good noninductive resistor will not work properly if long leads or long printed circuit board traces are allowed to add inductance to the mechanical assembly. Good PCB layout practice is mandatory.

The Design (cont.)

Next, we need to determine the inductance required of the input winding. Now that we know the voltage across the winding and the peak current through the winding, all we need do is calculate the minimum ton and repeat the same procedure as for the output:

$$t_{ON} = 0.49 \cdot 14.92\mu s = 7.31\mu s$$

$$\text{then } L = 15.5V \div \frac{14.74A}{7.31\mu s} = 7.69\mu H$$

Now that we have the inductances of the output and input windings we can determine the voltage stresses applies to the switch and diodes, and make a final determination of the appropriate devices. The trick here is that the inductance varies as the square of the number of turns, so the turns ratio varies as the square root of the ratio of the inductances.

$$\text{turns ratio} = \sqrt{\frac{7.69}{1.35}} = 2.39:1 \text{ or } 0.419$$

Thus, when there is 65V present on the input winding, there will be 65V • 0.419 = 27.2V on the 5.0V output winding. Adding to this the +5.0V that will be present on the cathode end of the diode from the output gives 32.2V, and means that a 45V diode allows a 40% margin for noise spikes and should work well. Two good choices are the Motorola #MBR1045 and the #MBR1645, the difference between them being that the larger one would be a bit more efficient.

Similarly, when the main switch is OFF, in addition to the 65V present from the input, there will be:

$$5.8V \cdot 2.39 = 13.9V$$

reflected from the output, for a total of 78.9V present on the drain of the main switch. This leaves a 26% margin for spikes. A 100V FET should work.

A similar procedure based on turns ratio finds the voltage present on the diode on the 12V output. This output is ratio-metrically linked to the 5.0V winding with its own turns ratio of 12.8 : 5.8, or 2.20:1, so when there is 27.2V reflected from the input winding there will be 27.2V • 2.2 = 59.7V, plus 12V from the output, for a total of 71.7V across the 12V diode. A 100V, 1.0A ultra high speed silicon diode, like a Motorola #MUR105 is a reasonable choice. Note that in the case of multiple outputs which conduct at the same time, the flyback magnetic does act like a transformer, but this is the only case in which it does.

Next, we can complete the definition of the magnetic assembly. The inductances of the input and output side are known. What remains is to define the resistances of the windings. These can be calculated from the rule that for an optimum size/efficiency magnetic, 50% of the loss occurs as resistive loss in the windings, and this loss is balanced among the windings based on the percentage of total power handled by each (the other 50% of the loss occurs in the core as hysteresis loss). Output power, as previously calculated, is 53.69W. Input power was estimated to be 55.93W. Thus

power loss in the magnetic is:

$$55.93W - 53.69W = 2.24W.$$

The copper loss should be close to 1.12W. Half of this, 0.56W, occurs in the input winding, which must supply all the outputs. The other half is split between the 5.0V and 12V windings in the ratio of their respective powers.

For the 5.0V winding this is:

$$\frac{44.8}{53.7} \cdot 0.56 = 0.467W$$

For the 12V winding it is:

$$\frac{8.89}{53.7} \cdot 0.56 = 0.093W$$

Knowing a target copper loss and average current for each winding, we can calculate the appropriate winding resistance. Since winding current has a sawtooth waveform, we first need to convert average current into RMS current.

$$I_{RMS} = I_{AVG} \sqrt{\frac{4}{3 \cdot D}}$$

As determined earlier, a D of 0.49 is used for the input winding (switch on – input winding conducting) while a D of 0.50 is used for the output windings (switch off – output windings conducting).

$$I_{RMS(INPUT)} = 3.61A \cdot \sqrt{\frac{4}{3 \cdot 0.49}} = 6.0A$$

$$I_{RMS(5.0V)} = 8.00A \cdot \sqrt{\frac{4}{3 \cdot 0.50}} = 13.1A$$

$$I_{RMS(12V)} = 0.70A \cdot \sqrt{\frac{4}{3 \cdot 0.50}} = 1.1A$$

With these currents, we can then calculate the winding resistances:

$$Input : \frac{0.56W}{(6.0A)^2} = 0.016\Omega$$

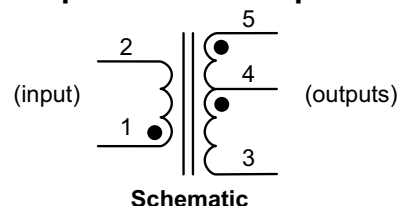
$$5.0V Output : \frac{0.467W}{(13.1A)^2} = 0.003\Omega$$

$$5.0V Output : \frac{0.093W}{(1.1A)^2} = 0.077\Omega$$

This completes the definition of the magnetic assembly.

Actually, because it is difficult to balance power loss between windings, or between windings and core, easing the calculated values up somewhat (as much as 20%) may result in a magnetic that would be significantly smaller with no increase in total losses. This should be discussed with your magnetics vendor. Also, because modern high-performance ferrites tend to have very low losses at moderate frequencies like 50 to 100KHz, you may wish to divide the total power loss differently, say 40% core, 60% copper. This can also reduce the cost of the inductor without increasing its size. This probably will not work if the clock frequency of the converter is 200KHz or more.

Figure 3 - Coupled Inductor Specification



Nominal Operating Frequency: 50 to 60KHz

WDG 1-2: L = 7.69μH ± 5% with 6A_{RMS}, 32A_{PK} flowing
DCR ≤ 0.019Ω, Leakage inductance 1-2 with 3-4 shorted: ≤200nH

WDG 3-4: L = 1.35μH ± 5% with 12.9A_{RMS} flowing
DCR ≤ 0.0036Ω

WDG 3-5: Voltage ratio of 3-5 to 3-4 is 12.8:5.8 ± 2%
DCR ≤ 0.092Ω

Polarization: Starts must be shown on schematic (pins 1, 4, 5)

Insulation: Vacuum impregnate in class A thermosetting varnish

Interwinding Insulation: not applicable

Expected thermal rise: <45°C in 40°C ambient

Mounting: Through-hole PCB

Leakage Inductance

The final thing you need to specify with regard to the magnetic is a maximum leakage inductance. Leakage inductance is a measure of the amount of flux generated by one winding in a magnetic assembly that is not coupled to the other winding(s) by the core and winding structure. For a flyback converter it is a measure of how much of the energy taken into the input winding is incapable of being transferred to the output winding when the switch turns OFF. This energy appears as a voltage spike on the drain of the MOSFET each time it turns off and must be dissipated either by the MOSFET directly, or in a snubber circuit. A reasonable value for leakage inductance is 1% to 2% of nominal inductance, but this is highly variable and depends on the intended operating frequency, size, and efficiency of the magnetic being developed. An actual maximum value should be discussed with your magnetics vendor before it is cast in concrete, and that maximum value should be used later for the development of a snubber, if a snubber appears to be worthwhile. (See Figure 3.)

Next, we select the output capacitors. Two criteria need to be met. First, the minimum capacitance must satisfy the standard capacitance definition $I = C \, dV/dt$ where I is in Amperes, C in Farads, $\Delta t = t_{ON}$ and $\Delta V \approx 25\%$ of the allowable output ripple. Second, and almost inevitably harder, the Equivalent Series Resistance (ESR) of the capacitor(s) must provide no more than the part of the ripple (75% in this case) not provided from the first criteria, in accordance with:

$$E_{RIPPLE} = I_{PEAK} \cdot ESR$$

where I_{PEAK} is the peak current from the output inductance during discharge. (This is because when the main switch turns OFF, the current in the filter capacitor switches, effectively instantaneously, from an outbound current I_{OUT} , to an inbound current, $(I_{PEAK} - I_{OUT})$. The reason for splitting the allowable ripple between the two criteria is that in the final converter they will tend to add. The reason for the asymmetrical split of the allowable ripple is that the ESR-caused ripple limit is the more difficult criteria to meet. In some instances a more drastic partitioning (5 or more to 1 in favor of the ESR ripple) may be better.

For the 5.0V output these criteria calculate out as follows:

$$C = 8A \div \frac{(0.25 \cdot 0.025V)}{10\mu s} = 12,800\mu F$$

and

$$ESR = \frac{0.75 \cdot 0.025V}{32A} = 586\mu\Omega$$

Based on Mallory type THF capacitor (330 μ F, 6 WVDC, $ESR \leq 0.04\Omega$) (a typical good output filter capacitor). This works out to 68 pieces in parallel to satisfy ripple from an ESR standpoint, and 39 pieces to satisfy ripple from a capacitance standpoint. Close enough. Note that the capacitor chosen is a tantalum capacitor, If you wish to use aluminum capacitors to perform the same service you can ignore ripple from capacitive droop and assign 100% of the ripple to ESR. Sizing an aluminum capacitor strictly from ESR will generally provide one with 40 to 100 times more capacitance than is needed. This will slow down the transient response of the converter, but it means that you will rarely, if ever, encounter stability problems.

Aside

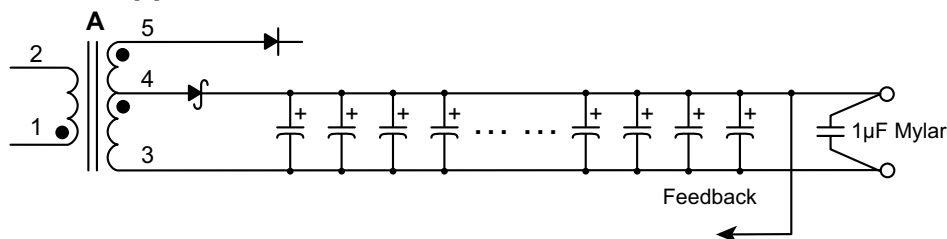
Based on the price of Mallory THFs, the stated solution may not be an optimum solution to the problem. A better solution might be to change the effective ripple specification from 0.025V to 0.250V and add an additional stage of LC filtering from the nominal output to the “real” output seen by the load. This means that instead of 68 capacitors we can use 4, but these must be followed by an LC filter with 10:1 attenuation (20dB) at 50kHz. This implies a corner frequency, f_C , of 5.0kHz, which means it won't be a small filter, but there is no necessity of using a high performance capacitor on this second filter stage. The other difficulty with a second-stage filter is that the DC resistance of the inductor is not cancelled by the feedback loop, and consequently the variation in output voltage with load current can exceed the specifications for the power supply. To hold the $\pm 1\%$ regulation specification on the 5.0V line we would need an inductor with $\approx .003\Omega$ resistance.

A second alternative would be to use a combination of electrolytic and film capacitors in parallel with the electrolytics sized solely to the load current ripple criterion and the film capacitors sized solely to the ESR ripple criterion. In this instance, ESR and capacitive droop should divide the ripple about 50-50. (See Figure 4.)

Figure 4 - Output Filters for Equivalent Ripple

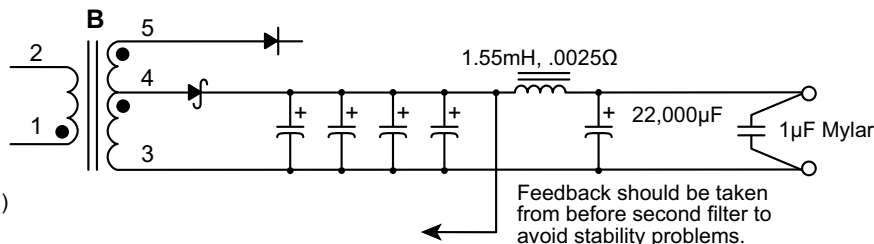
C = 68 pcs. Mallory #THF337M006P1G
Total 22,440 μ F

Cost: Highest
Response: Fastest
Volume: Smallest



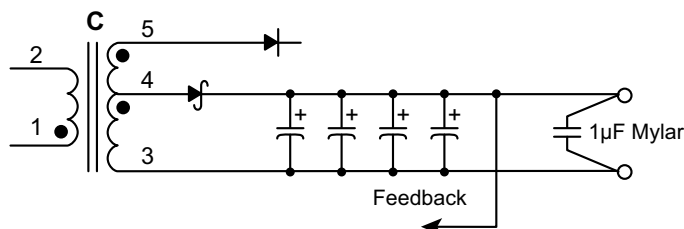
C₁ = 4 pcs. Mallory #THF337M006P1G
C₂ = 1 United Chemi-Con #RZA 22,000mF 6.3v
L = 1.5mH; 0.0025 Ω
Total C = 23,320 μ F

Cost: Intermediate
Response: Intermediate (Reduced Load Regulation)
Volume: Largest



C = 4 pcs. Sprague #676D159M6R3JT5C
Total C = 60,000 μ F

Cost: Least
Response: Slowest
Volume: Intermediate



Next we define the filter capacitors for the 12V output in the same way:

$$C \geq 0.7A \div \frac{0.25 \cdot 0.5V}{10\mu s}, \text{ thus } C \geq 56\mu F$$

$$ESR \leq \frac{0.75 \cdot 0.5}{2.8A}, \text{ thus } ESR \leq 0.134\Omega$$

This is a much easier capacitor to find. A Sprague type 676, 900 μ F 12WVDC, aluminum electrolytic (the smallest 12V capacitor in this series) will work well. A 56 μ F, 15V, Mallory type THF will also work.

Next we define the divider resistors which will be used to feed back a sample of the 5.0V output to the error amplifier in the PWM. Because the error amp in the HV9110 is CMOS, its input bias current is negligible, and the divider string can carry a very small current; 100 μ A is plenty. The feedback terminal of the HV9110 (the inverting terminal of the error amplifier) is satisfied by 4.00V $\pm$ 1%. If we use a 100 μ A divider, the lower resistor should be:

$$4.00V \div 0.0001A = 40k\Omega$$

The closest real value is 40.2k Ω . To produce exactly 4.00V with 40.2k Ω we need an actual divider string current of:

$$4.00V \div 40200\Omega = 99.50\mu A$$

Dividing the 1V remaining between 4V and our intended output of 5V by our actual divider string current, gives a value of:

$$1.00 \div .00009950 = 10,050\Omega$$

The closest value is 10.0k Ω .

Normally, the next and final step in the design process would be stability analysis. However, it turns out that one of the advantages of discontinuous-mode, current-mode flyback converters with a maximum duty cycle of < 50%, with output capacitors (especially if they are aluminum electrolytics) sized to ripple requirements, is that they are usually stable "as is." As a matter of prudence, checking the loop response of a new power supply on a network analyzer or Venable machine is always a good idea, but for supplies of this nature this writer no longer considers full analysis mandatory. For this reason, and because including stability analysis in this application note would probably double its length, analysis is omitted. For those desirous of performing a full mathemati-

cal analysis of every loop, the following texts⁵ on the subject are recommended:

DC to DC Switching Regulator Analysis

Dan Mitchell, McGraw-Hill, ISBN 0-07-042597-3

Switch Mode Power Conversion

K. Kit Sum, Marcel Dekker, ISBN 0-8247-7234-2

Modeling, Analysis and Design of PWM Converters, Vol. 2

VPEC staff, VPEC2, ISBN (none)³

Advances in Switched-Mode Power Conversion, Vol. I & II

R. D. Middlebrook and S. Cúk, Teslaco, ISBN (none)⁴

Dynamic Analysis of Switching-Mode DC to DC Converters

Nathan Sokal, Andre Kislovski, and Richard Redl, Van Nostrand Reinhold, ISBN 0-442-21396-4

Modern DC to DC Switchmode Power Converter Circuits

R. Severns and G.E. Bloom, Van Nostrand Reinhold, ISBN 0-442-21396-4

Accessory Circuits

1. The snubber circuit for the MOSFET drain switching spike should be sized to absorb the energy taken into the magnetic that is not coupled to the output. The available energy is $1/2 L \cdot I^2$ where L is the leakage inductance of the primary and I is the peak input side current. Using a reasonable estimate of 2% for leakage inductance gives a value of 250nH. Spike energy then is:

$$1/2 (250nH \cdot (14.74A)^2) = 27.2\mu J$$

Multiplying this by the maximum repetitions per second (which occurs at maximum frequency) gives:

$$27.2\mu J \cdot 67,000Hz = 1.82W$$

which is the amount of power to be dissipated either in the MOSFET or the snubber.

To dissipate it in the snubber it must be captured in the snubber capacitor without exceeding the drain breakdown of the FET.

Minimum FET breakdown: 100V

Maximum circuit-supplied voltage on FET drain: 78.9V

Maximum voltage for snubber cap: 21.1V

To calculate the size of the snubber capacitor we convert the $1/2 L \cdot I^2$ energy previously calculated to $1/2 C \cdot V^2$ energy, and divide by the maximum voltage we desire on the capacitor:

$$\frac{2 \cdot 27.2\mu J}{21.1V^2} = 122nF$$

Using the nearest real capacitor (120nF in this case) assures us that the voltage spike will not be large enough to break down the MOSFET. The resistor in series with the snubber capacitor must have a low enough value to allow the capacitor to discharge in the minimum on-time of the switch, which for a HV9110 will be about 200ns. Because the discharge distance (62.5V max) is much greater than the charge distance (21.1V) declaring 400ns = RC will work. Thus:

$$400ns \div 120nF = 3.33\Omega$$

The catch here is that, except when the switch is on for the minimum time, the capacitor will reverse charge to:

$$V_{IN} - (V_{FET} + V_{CURRENT\ SENSE}) = 62.5V.$$

It is this energy which must be dissipated in the resistor:

$$1/2 (62.5V^2 \cdot 122nF) \cdot 67kHz = 16.0W$$

So a 20W resistor will be necessary. To save 679mW in the FET, this hardly seems worthwhile, but it can be done if desired.

2. If a snubber is used, an RC filter network should be added between the current sense resistor and the current sense terminal of the HV9110 to prevent the higher-than-usual leading edge spike on the current waveform from shutting the switch off prematurely. The RC time constant of this filter should be approximately 20% of the snubber time constant, but never more than $\approx 100ns$. (Otherwise authentic fault current spikes may be slowed down too much.) The R for the current spike filter can be a lot larger, and the C much smaller, because the load presented by the HV9110 is quite small (on the order of 3.0pF). Using a 1.0k Ω resistor and a 75pF capacitor should be sufficient for the snubber above.

3. Two small capacitors are shown in Figure 2, connected directly at the converter outputs. These are 1.0 μF stacked film capacitors with very good AC characteristics, intended for general noise suppression. They may not be necessary, but they are reasonable insurance.

4. An Input EMI filter will also be required under most circumstances. For conducted emissions, generally an asymmetrical pi-type filter is sufficient. The converter-side capacitor should be sized to convert the ΔI caused by switching to a reasonably low Δ voltage over t_{OFF} . The inductor and input side capacitor should be designed to have a corner frequency that complements the corner frequency of the regulator loop, to minimize susceptibility to outside noise coming in to the regulator.

In this case, from previous calculations, input switching current is known to be a maximum of 14.74A. Similarly, minimum t_{OFF} is 7.46 μ s, and a reasonably low value for ΔV is 250mV. Thus, from $I = C \, dV/dt$, the converter side capacitor calculates out to:

$$\frac{14.74A}{(0.25V / 746\mu s)} = 440\mu F$$

A good choice is 470 μ F. This capacitor can also serve to insure a minimum holdup time for short input dropouts.

The values of the inductor and the input side capacitor can be calculated from:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

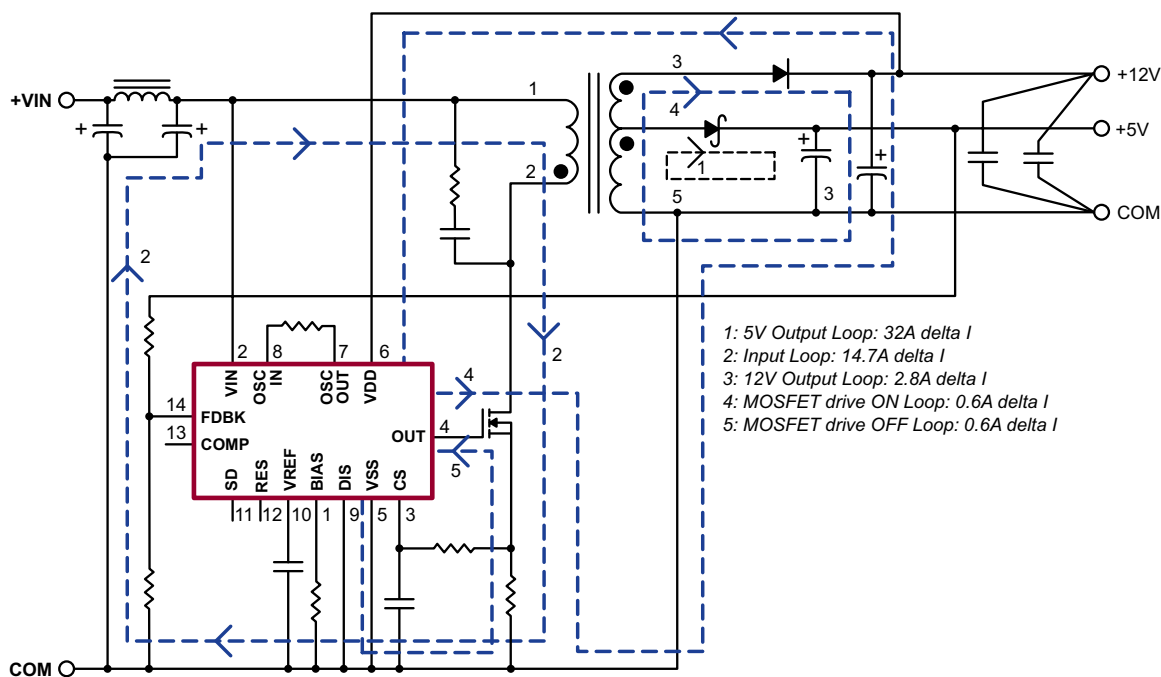
once the corner frequency of the regulator loop is known. In this case the regulator loop is rather slow, due to the large output capacitors required by the ripple specifications, and an appropriate frequency to use is only 750Hz. This gives us a $\sqrt{LC} = 212 \times 10^{-6}$. This means that any combination of inductor and capacitor values whose product is 4.5×10^{-8} will provide an adequate filter. Generally, it is best to use a larger value of capacitor and a smaller value of inductor because inductors usually cost more. In this case using a 1000 μ F capacitor results in a 45 μ H inductor, 47 or 50 μ H is easily obtainable, small and inexpensive. The DCR should be low enough so that our previous calculations based on V_{IN} remain valid. Based on 3.6A maximum DC input current, a 0.5 Ω DCR will give a 0.14V drop, which is well within allowable safety margins, and results in a cheap, small inductor.

On Layout and Noise (Radiated EMI)

Anyone using the HV9100, HV9110, or other parts in the same family, will end up switching current flow on and off. Sometimes, quite large currents are switched in short periods of time. In the current example, the dI/dt on the 5.0V secondary will be over 300 amps per microsecond! This is sufficient to cause significant radiated EMI if it is improperly handled.

Controlling EMI from a switchmode converter is neither difficult nor costly, provided attention is paid to the subject early enough in the design cycle.

Figure 5 - High Switched Current Paths



There are no “tricks” to EMI control, only one basic rule: Minimize the area of the loops around which switched currents circulate.

This is purely a mechanical constraint, and should be dealt with during PCB layout. Generally, unless you have a PCB layout person with prior experience with switching converters, the circuit designer will have to lead the board designer through the first few layouts, and even thereafter, will have to show the board designer where the switched current loops are in the circuit. (See *Figure 5*.)

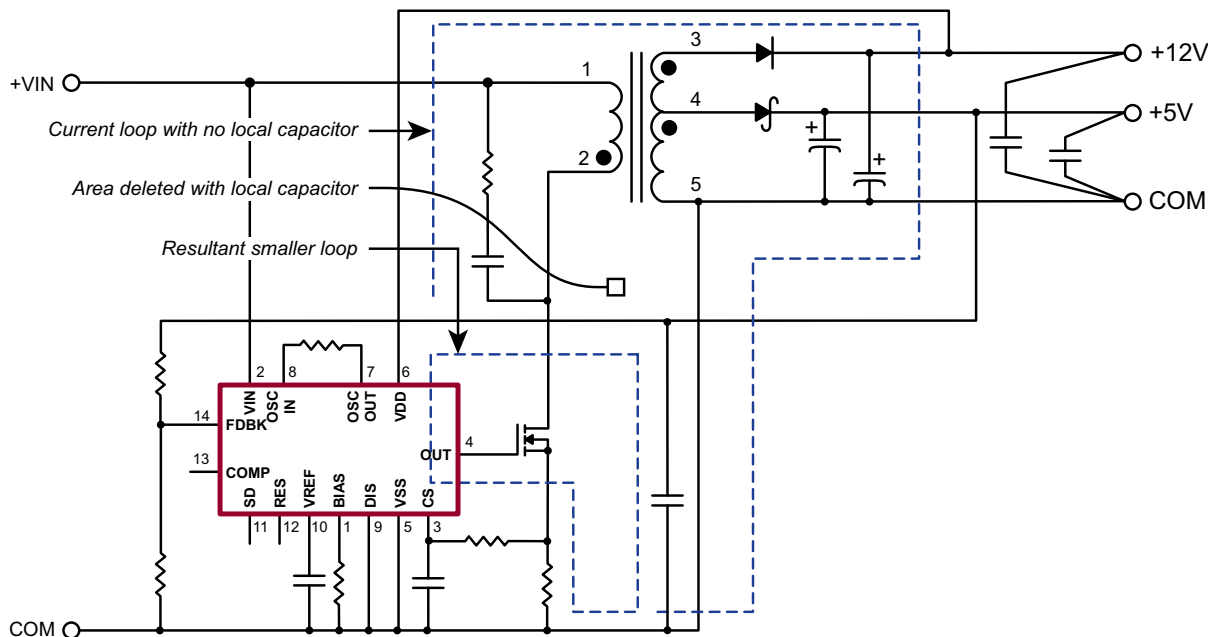
Obviously, there are other constraints to a switchmode converter PCB as well, and these also affect system performance. Most converters should be laid out single-sided, with the second side of the PCB reserved for a ground plane. Also, high currents require wide lands, just to keep DC resistances low. First and foremost though, should be the effort to keep switched current loop area minimized. Loop length is also important, as long runs can have enough inductance to disrupt circuit operation. On the HV9110/HV9120 this is only likely around the gate drive loops, which have relatively low ΔI 's, and the current sense resistor, where stray inductance can cause the overcurrent sensing to shut the main switch off prematurely, thereby limiting power output.

Board layout should proceed by taking the switched current loops in order of delta I, and laying the DC portions of the circuit out last. Using the first circuit as an example, this means starting with the 5.0V loop, (which includes only the coupled

inductor, 5.0V diode, and output capacitors) taking the input loop next (coupled inductor, power MOSFET, current sense resistor, and input filter cap) and following those with the 12V output loop, and the MOSFET drive loops. In each instance, it is the entire loop that matters, including the return path. Assuming that the return path is good, even on boards with ground planes, is risky. Look at each loop carefully to see that its area is minimized. After the switched current loops are laid out, the DC sections can be fitted where they are convenient. They do not contribute noise, but they can convey it if it is generated elsewhere. The feedback loop is a special case. By itself, this is a DC loop, but it is susceptible to noise generated on other loops, and because it is, for the most part, a high-impedance path, not much energy is required to disrupt it. The feedback loop should also be laid out for minimum area, but it is more important that the path of its circuitry lies well away from, and where possible perpendicular to, the switched current loops. Generally, layout grows outward from the transformer, and careful choosing of which pins on the transformer connect to which windings can do a lot to make layout convenient.

There are a few things that can be done in designs with the HV91XX family that may make a specific layout more convenient: First, it should be remembered that the high current paths associated with the current sense resistor do not include the line from the junction of the resistor and the MOSFET to the current sense terminal of the IC. The sense lead to the IC is a very low current path, and can be comparatively long providing that the path from MOSFET to re-

Figure 6 - Effect of Local V_{DD} - V_{SS} Capacitance on Area of MOSFET On-drive Loop



sistor to ground is short. The output lead from HV9110s and HV9120s however should be kept short, because it services both the charge and discharge paths from the MOSFET gate. Also, when a 10 or 12V winding on the transformer is used to power the HV91XX, it may help to split the filter capacitor into two pieces, one near the transformer and diode (to keep that current loop short) and a second near the HV91XX to keep the ON-drive current loop short. The VDD and VSS terminals of the HV91XX are adjacent to each other specifically to allow this. (See Figure 6.)

Inevitably, there will be some residual radiated EMI, and some of this will be picked up by the DC circuits and seen on the input and outputs as conducted EMI. The 1.0 μ F film capacitor previously noted should suffice to remove this from the outputs, and a small commercial line filter should suffice for the input. Most commercial EMI filter suppliers offer EMI lab services (sometimes free!) to assure that the end converter + filter meets whatever requirements are in force for your particular circumstances. Using these services as a final check is generally worthwhile.

There is only one additional noise control measure necessary. The reference pin of the HV91XX is a high impedance node, and is designed to work with a 0.01 to 0.1 μ F capacitor between itself and VSS. This capacitor should not be omitted. On the other hand, a capacitor between the bias pin and VSS should not be required. If a capacitor from the bias pin to VSS improves operation, the capacitor should be placed from VDD to VSS. As usual for any switching circuit, all noise

filtration capacitors should be types with good high frequency performance: Stacked Mylar and ceramic multi-layer caps generally are best. (See Figure 7.)

Example 2

A 3W converter for a DPM. Size is to be as small as is consistent with low cost, input range is 65 to 240VAC, load is fairly constant.

As before, first we need is specifications to design to:

$$\text{Max input voltage} = 3.90\text{VDC} \{[(240 \div 15\%) \cdot \sqrt{2}] - 1.4\}$$

$$\text{Min input voltage} = 90\text{VDC} [(65 \cdot \sqrt{2}) - 1.4]$$

Outputs:

A: +5.0V $\pm$ 5%, 0.4 to 0.55A, $\leq$ 100mV ripple

B: -5.0V $\pm$ 5%, 30mA, $\leq$ 100 mV ripple

C: +10V $\pm$ 10%, 14mA, $\leq$ 100mV ripple

Maximum Output Wattage: 3.04W

Minimum Output Wattage: 2.29W

Operating Frequency: 500kHz (min)

An HV9120, which accepts input voltages up to 450VDC will be required. This time, even with the high operating frequency, sufficient dynamic range exists (13.2:1) so that the end supply should not exhibit cycle skipping. This minimizes the size of output filters. (See Figure 8.)

Figure 7 - The Final Design

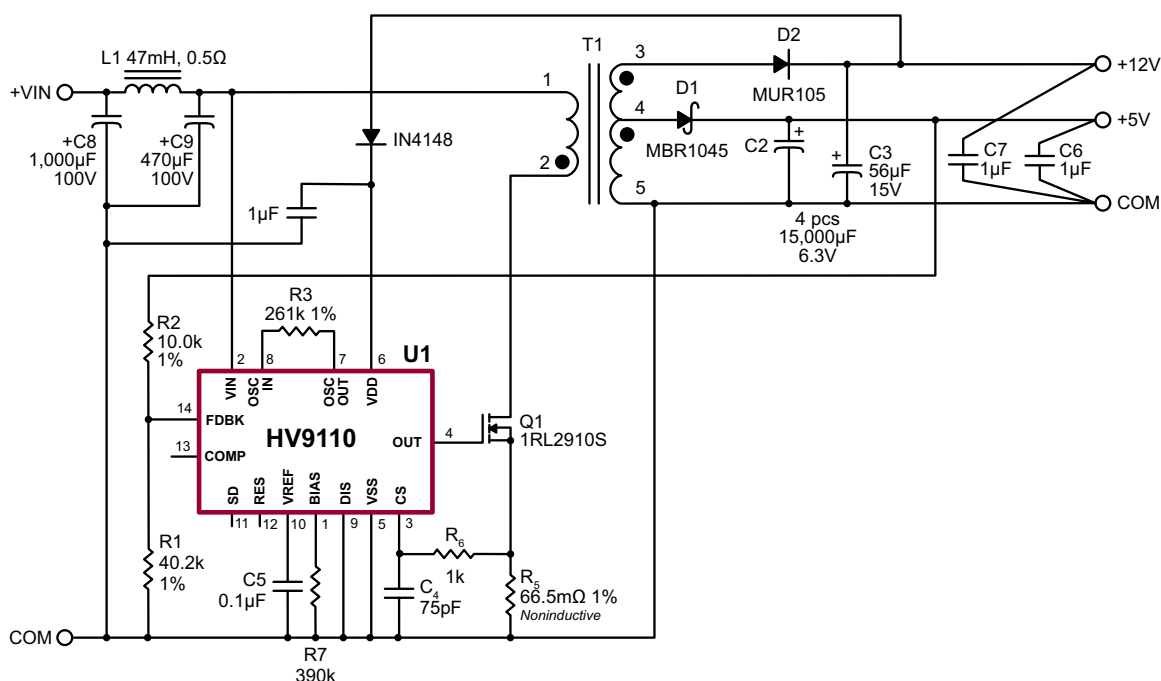
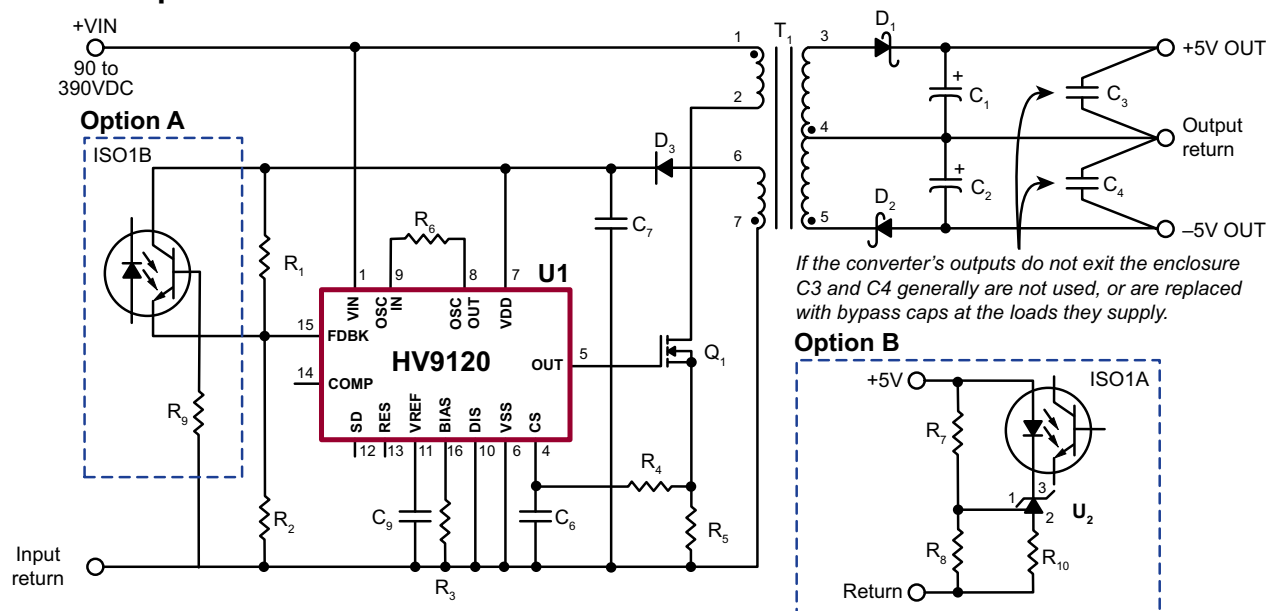


Figure 8 - Example 2



The Design

First, select a timing resistor. To assure that all units operate at 500kHz or above despite tolerance effects, a 16.5kΩ resistor should be sufficient. But, because parasitic capacitances associated with the PCB layout can have a serious effect on clock oscillator performance at high frequencies (the timing capacitance in the 9120 totals less than 10pF), the value of the timing resistor should be confirmed in the final assembly to assure desired performance.

Next, calculate minimum t_{OFF} and t_{ON} . If minimum frequency is 500kHz, worst case maximum can be up to 600kHz, and at 600kHz, maximum duty cycle will be no greater than 46.5%. Thus, minimum t_{ON} will be:

$$1667ns \cdot 0.465 = 775ns$$

and minimum t_{OFF} will be:

$$1667 - 775 = 892ns$$

or 53.5% of total period. For peak current calculations (to follow) it will be sufficient to declare D (duty cycle) = 46.5%, and 1-D = 51.5%, leaving a 2% deadband to assure discontinuous-mode operation.

Next, translate the DC current of the output with the greatest percentage of the load (+5.0V this time) to a peak current using the same formula as in the previous example:

$$0.55A \frac{2}{0.515} = 2.14A_{PEAK}$$

This allows us to calculate the inductance of the secondary using $E = L \, di/dt$. Remember that the voltage seen by the inductor includes the forward drop of the output diode, so the actual calculation works out to:

$$5.75V \div (2.14A \div 858ns) = 2.30\mu H$$

The -5.0V winding will be equal in turns (thus also in voltage and inductance) to the +5.0V winding. The 10V winding, (which powers the HV9120) conducts at the same time as the main +5.0V winding, and thus has a turns ratio equal to its voltage ratio, (10.7:5.7) and no inductance calculation for it is necessary.

Note:

The load stated above for the 10V winding (14mA) is considerably larger than the 1.0mA specification for the HV9120. The remaining 13mA are what is required to provide the charge to the gate of the power MOSFET the HV9120 will be driving at 500kHz. This current was determined by dividing the total gate charge of the MOSFET (Q_g) at $V_g = 10V$ (from the MOSFET data sheet) by 10V (V_g) to determine the effective gate capacitance, then using that capacitance value in $I = CVf$ (converting charge to current) to determine the current required to charge the gate 500,000 times per second. While this calculation is a good check of real supply current for the HV9120 in operation, it is seldom necessary unless the converter is operating at over 100kHz.

Next, using the same system, calculate the required inductance of the input winding. To start, we need the power into the magnetic, which is just the power out of the magnetic divided by its efficiency. Power out of the magnetic includes not only output power, but the voltage drop through the output diodes. At the currents needed, 0.75V is a safe estimate for diode drop. So maximum power out of the magnetic will be:

$$[5.75V \cdot (0.55A + 0.03A)] + (10.75V \cdot 0.014A) = 3.485W$$

Because it is more difficult to design small magnetics (and size was one of our original constraints) to high efficiency, and because higher frequency magnetics tend to be less efficient, this time I will adopt an efficiency estimate of only 94%. Now, power into the magnetic calculates out as:

$$3.485W \div 0.94 = 3.707W$$

To obtain a DC input current, this wattage is divided by the minimum DC voltage across the input winding, which is just the minimum DC input voltage less the drop in the current sensing resistor and the power MOSFET. The maximum drop across the current sensing resistor again should be set to just under 1.0V (from the HV9120 spec.) and a reasonable estimate for drop in the MOSFET is 2.1V, (based on the use of a Supertex #VN2460N3, 600V, 20Ω MOSFET). So minimum input side voltage will be:

$$90 - (1 + 2.1) = 86.9V$$

and DC input current will be:

$$3.707W \div 86.9V = 42.7mA$$

Knowing DC average input current and duty cycle we can now calculate peak input current, which will be:

$$0.0427A \frac{2}{0.465} = 184mA$$

Knowing peak input current, minimum input voltage and smallest maximum ton, we can now calculate input side inductance from $E = L \, di/dt$. This works out to:

$$86.9V \div \frac{184mA}{775ns} = 336\mu H$$

Next, we need to determine the DC resistances of the various windings of the magnetic. In this case, because of the

operating frequency, copper losses and core losses probably will be approximately equal. Again, power loss in the magnetic is just $P_{IN} - P_{OUT}$ or 222mW. Assuming half of this is copper loss gives a copper loss of 111mW. This should be divided among the various windings in proportion to their proportion of the total wattage.

Input winding: 50%, or 55.5 mW

+5V output: 45.4% or 50.4 mW

-5V output: 2.5% or 2.75 mW

+10V output: 2.2% or 2.40 mW

Actually, this shortchanges the input winding somewhat, as it carries slightly more power than all outputs combined, but this is usually trivial. As before, RMS current (NOT average) is used to determine resistance knowing dissipation:

For the input winding: $.0555W \div (72mA)^2 = 10.6\Omega$

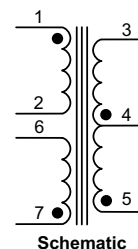
For the +5V winding: $.0504W \div (885mA)^2 = 64m\Omega$

For the -5V winding: $.00275W \div (48mA)^2 = 1.18\Omega$

For the 10V winding: $.0024W \div (23mA)^2 = 4.73\Omega$

This gives us enough information to complete a specification for the coupled magnetic. (See Figure 9.)

Figure 9 - Coupled Inductor Specification



Nominal Operating Frequency: 500 to 600KHz

WDG 1-2: $L = 366\mu H \pm 5\%$ with $184A_{PK}$ flowing
DCR = 30Ω (MAX), Leakage inductance
1-2 with 3-4 shorted: 10μH (MAX)

WDG 3-4: $L = 2.3\mu H \pm 5\%$ with $2.14A_{PK}$ flowing
DCR = 0.16Ω (MAX)

WDG 5-4: Voltage ratio WDG 5-4 to WDG 3-4 is
1.0:1.0 $\pm 2\%$
DCR = 3.0Ω (MAX)

WDG 6-74: Voltage ratio WDG 6-7 to WDG 3-4 is
10.7:5.7 $\pm 2\%$
DCR = 12.5Ω (MAX)

Polarization: Starts must be shown on schematic (pins 1, 4, 5, 7)

Insulation: Vacuum impregnate in class H thermosetting varnish

Interwinding Insulation: WDG 3-4-5 to WDG 1-2 & 6-7
1.5KVAC (MIN)
WDG 1-2 & 6-7
500VAC (MIN)

Expected thermal rise: <60°C in 50°C ambient

Mounting: Through-hole PCB

The value of the current sensing resistor can be determined once the peak input current is known. The sensing voltage levels for the HV9120 are the same as they were for the HV9110 in example 1. Thus:

$$0.99V \div 0.184A = 5.38\Omega$$

The next lower resistor is 5.36Ω in 1% or 5.1Ω in 5%. As the last time, using a 5% resistor will probably result in very few (if any) units that do not allow full output power at low line. Wattage of the current sense resistor is calculated as I^2R using RMS winding current (72.3 mA). This calculates out to 26.7mW based on a 5.1Ω resistor, so a 1/10 watt resistor (if you can find a noninductive one) can be used.

The drop across the main switch and its power loss should be calculated next. In this case we already selected a main switch (a Supertex VN2460N3) based solely on its being the smallest (and least expensive) 600V MOSFET available.

The on-resistance of the VN2460N3 is 20Ω, which implies a peak-current voltage drop of 3.68V, and a power dissipation of 105mW, which is easily handled by the TO-92 version.

Using the “square root of inductances ratio” we can now determine the approximate voltages reflected across the coupled inductor to determine the actual voltages present on the main switch when it is off and the diodes when they are blocking. This time that works out to:

$$\sqrt{\frac{366\mu H}{2.30\mu H}}$$

or 12.6:1. Thus when the main switch is off, it will see:

$$5.7V \times 12.6 = 71.8V$$

added to the 390V present from the input, a total of 462V.

The diodes, when blocking, can see a maximum of:

$$390 \div 12.6 = 31.0V$$

added to the 5.0V present on the output capacitors. So 1.0A 40V Schottky diodes, such as the 1N5819, should work well for 5.0V output diodes.

If increased efficiency were required, 1N5822 three-amp Schottky diodes, and/or a 500V, 13Ω, VN2450N3 main switch could be substituted.

As with the first example, the next thing to do is to calculate the requirements for the output filter capacitors. This time the ripple specification is easier to meet (100mV vs 25) and the loads are smaller. The technique remains the same, and a 25% / 75% division of ripple between capacitance and ESR should still hold. Thus, for the +5.0V output:

$$C = 0.55A \div (0.025V \div 930 \times 10^{-9} \text{sec}) = 20.5\mu F$$

Remember that for capacitor holdup, maximum rather than minimum ton is used, as the time for which the capacitor must hold up is the maximum time the switch could possibly be on. ESR ripple is also done exactly as before:

$$ESR = 0.075V \div 2.14A = 35m\Omega$$

This is a much easier capacitor to find. A Nichicon SF type 150μF, 6.3V would work fine. So would a Sprague 672D227H6R3CG3C (220μF, 6.3V aluminum) or a Sprague 199D336X96R3DA1 (33μF, 6.3V dipped tantalum).

The -5.0V secondary works the same way, except the current is only 30mA:

$$C = 0.030A \div (.025V \div 930 \times 10^{-9} \text{sec}) = 1.1\mu F$$

$$ESR = 0.075V \div 0.117A = 0.641\Omega$$

In this case, because the load current (and thus the capacitor) are so small, it is probably better to use a 1.0μF stacked film capacitor and ignore the ESR which will be orders of magnitude below requirements. A 1.0μF 50V Wima #MKS-2 (ESR ≈ 0.02Ω) would be fine. The same capacitor could also be used on the 10V output that feeds the HV9120 (14mA). This particular capacitor is also an excellent choice for the final noise filters on the regulator's outputs (as in

example 1). But in this case the regulator's outputs will not go outside the enclosure and extra noise filters are probably unnecessary.

Feedback for this circuit is shown two ways: First, as just a resistive divider off the secondary that feeds the HV9120, and second as optical feedback, which requires additional circuitry. (See Figure 10.) For the regulation specifications given, ($\pm 5\%$) a resistive divider on a separate winding is sufficient over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$). Such a "divider on a separate output" relies on the magnetic coupling between windings on a common core to regulate the isolated windings. Within limits (accuracy, mostly) it works very well, but it would require an excellent transformer builder to be able to meet $\pm 5\%$ regulation of magnetically coupled outputs over a full -55°C to $+125^{\circ}\text{C}$ military temperature range.

The resistive divider, as in the previous example, can draw very little current, because the CMOS error amp in the HV9120 does not draw significant bias current. Because the last example used $100\mu\text{A}$ divider current this one will use $40\mu\text{A}$. (Using much less than $20\mu\text{A}$ requires using high value precision resistors that are expensive.) Again, the feedback point of the HV9120 is internally trimmed to expect 4.00V at design output voltage. This time the design voltage of

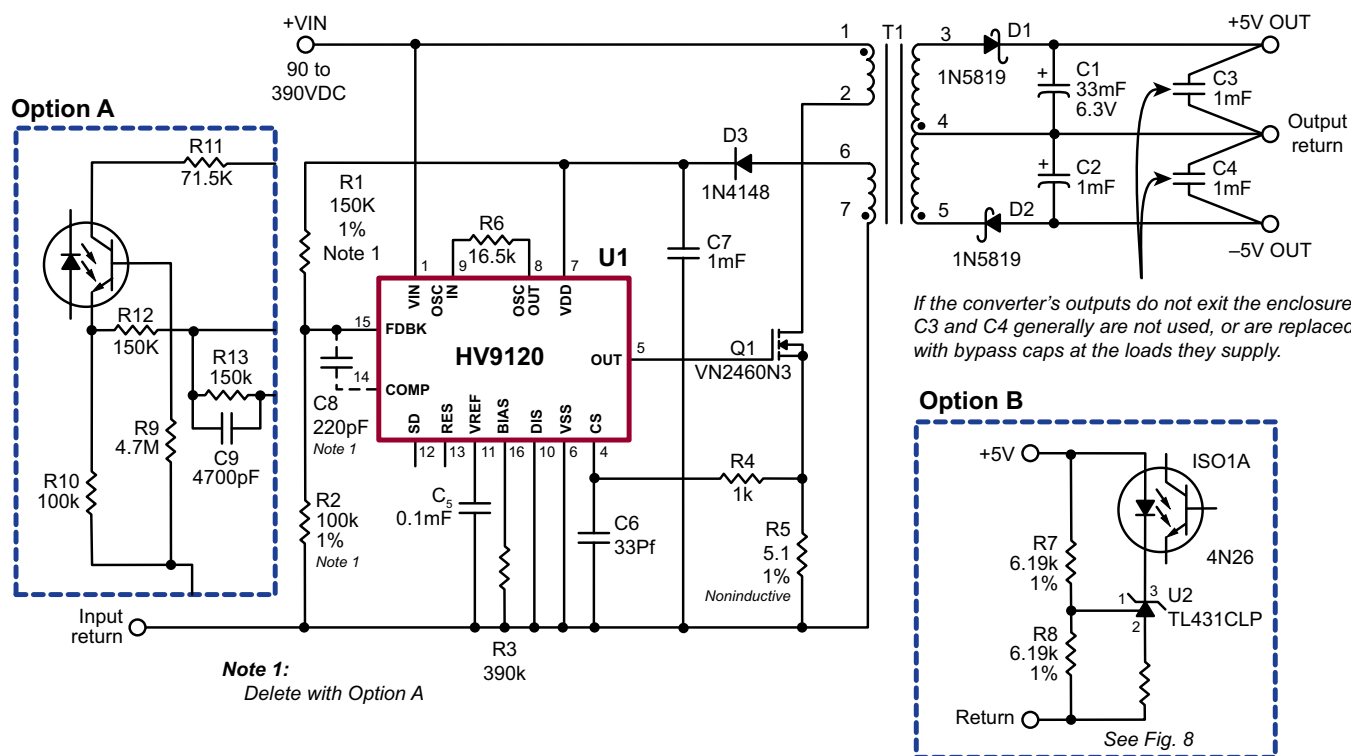
the winding directly coupled to the divider is 10V , so using a $40\mu\text{A}$ divider current, the lower resistor becomes $100\text{k}\Omega$, and the upper resistor becomes $150\text{k}\Omega$.

Accessory Circuits

1. No snubber circuit is shown on this converter, and none should be necessary. Maximum energy available to be snubbed, like last time, is just $L_{\text{LEAKAGE}} \times I_{\text{PEAK}2}$, or 304nJ per switch-off. At 600kHz that works out to 182mW , which is easy to ignore. Also, the main switch chosen has 20pF of reverse transfer capacitance, which can absorb this much energy while only rising an additional 76V . This still leaves V_{DRAIN} of the MOSFET below 90% of breakdown and should be safe.

2. Leading-edge spike suppression on the current sense resistor can be handled as it was in the first example, with a $1.0\text{k}\Omega$ resistor between the top of the current sense resistor and the current sense pin on the HV9120, plus a capacitor between the current sense terminal and ground. For this regulator, leading edge spike suppression is probably more important than it was for the last one, because the peak gate drive current to the power MOSFET is actually greater than the load current! Because the gate capacitance of the FET is much smaller though, the capacitor's size should be reduced. 33pF is a good starting value.

Figure 10 - The Final Design



3. Optical feedback is usually only used on isolated outputs that must be regulated to a tighter tolerance than $\pm 5\%$ over industrial temperature range or $\pm 7.5\%$ over the military temperature range. Optically isolated feedback has been developed over the past few years so that it is straightforward and relatively inexpensive, consisting of a T.I. #TL431, an optocoupler and two to four resistors. Because of the high gain of the TL431 (80dB), virtually any level of accuracy desired is achievable.

The TL431 requires 2.5V at its third terminal to achieve regulation. As we require a 5.0V output, the divider resistors will be equal. The TL431 requires a maximum of 4.0 μ A into the reference terminal. To hold reference current to a maximum of 1% divider error, divider current must be $\geq 400\mu$ A. Thus the divider resistors should be $\leq 6250\Omega$ each. A reasonable value is 6.19k Ω . The original feedback divider at the HV9120 is replaced by a divider composed of the phototransistor and its emitter load. Precision resistors for this divider are no longer required because the regulation loop will compensate for any errors here. The current used earlier on this path (40 μ A) can be kept, or adjusted as convenient. We will stay with the original value.

The choice of optocoupler will depend on the loop response speed required. Optocouplers tend to be slow, and unless care is taken in optocoupler selection, the optocoupler ends up being the controlling element in regulation loop response speed. For this example, I used a 4N26 because it was on hand. A 6N135 or similar high speed optocoupler would have given loop response more appropriate for a 500kHz converter. The resistor shown between the base of the optoisolator transistor and ground is a noise/leakage eliminator and should have a value between 1.0M Ω and 10M Ω , depending on the optocoupler used. For a 4N26, 4.7M Ω works well.

Because there are now two op amps in the regulation loop, loop gain will be far more than necessary, and some of it must be done away with. Otherwise stabilization will be a problem. There are two simple ways to eliminate gain. Either convert the error amp in the HV9120 to a gain of -1 configuration with two equal resistors, or add a resistor between the anode of the TL431 and output return to reduce its gain to approximately 1. Both methods work equally well. The error amp in the HV9120 has a minimum guaranteed output sink current of 120 μ A, so any feedback resistor greater than 50k Ω will allow full opposite swing. 150k Ω gives plenty of margin, and reduces power a little.

Alternatively, a resistor between the anode of the TL431 and output return can be used as a gain-destroyer to reduce the

gain of the TL431 (plus the optoisolator) to approximately 1. The value of the gain-destroyer resistor is dependent on the coupling "gain" of the optoisolator and the current required from the phototransistor. Using a 4N26, the current required from the phototransistor is approximately 40 μ A, and the LED current required to achieve it will be approximately 100 μ A. To adequately reduce the gain of the TL431 will require a delta V on its anode of about 50mV, so a 470 Ω resistor should work.

Conclusion

To demonstrate functionality, both examples were assembled and tested by a technician at our facility. A few suggestions to avoid difficulties are as follows:

- 1) Wire-wrap construction methods are, and always will be, completely incompatible with power supply construction. The light gauge wire will not carry the current, and the stray inductance caused by longer-than-necessary paths will disrupt the circuit and cause additional EMI. Seriously, the requirement for short, low-inductance, low-resistance paths and good mechanical layout throughout the design is mandatory. Every unnecessary tenth of an inch of lead should be eliminated. This may not appear to save space in a completed design, but in fact it will save both space and trouble.
- 2) Flyback power supplies should never be operated without a load! Once the main switch turns off, the energy stored in the coupled inductor inevitably goes into the output and charges the output filter capacitors. If no load is present to remove the charge, the capacitors or the output diodes will break down.
- 3) Output voltage ratios for the multiple output windings may need to be adjusted slightly, to get all output voltages into tolerance. This happened in the small converter where the 10V output winding, because it was closer to the input winding than the other output windings, put out more voltage than planned. The solution was to reduce the number of turns on that winding by about 10%.
- 4) My choice of the optoisolator (a 4N26) was not appropriate. The result was that the regulation loop crossover frequency was only 9.0kHz, when it should have been over 100kHz. A transistor with a 10 μ s storage time, like the phototransistor in the 4N26, just isn't capable of the response speed desired from a 500kHz switcher.

In summation, two different circuits have been developed to show the flexibility of flyback converters built with the HV91XX family PWM ICs, and the simplicity of their design and con-

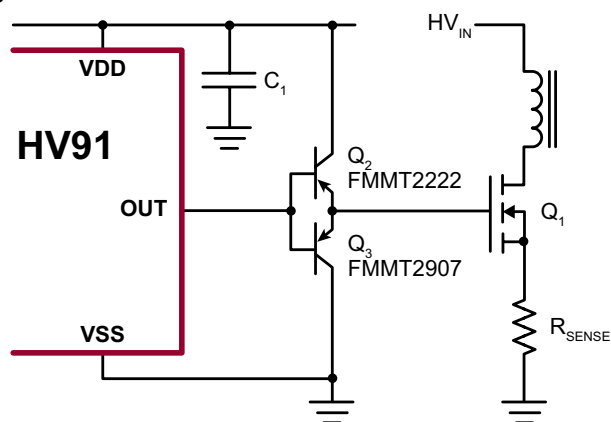
struction. Both circuits met their original design goals. The field of use for the HV91XX family is a lot broader than can be illustrated in a single application note. Many other forms of converters, which may be best suited for their particular purposes can also be built using the HV91XX PWM ICs.

Contact Supertex for additional application notes.

Final Note: OUTPUT to MOSFET Drive Circuits

In some instances, designs greater than 10W, the output MOSFET may have a very high input capacitance. In these cases the output drive waveform of the HV91 would have slow rise and fall times causing low dynamic range and excessive heat dissipation. Low dynamic range is due to a larger minimum pulse width than desired. Excessive heat dissipation would be due to the on-to-off cycle of the MOSFET being too slow.

Figure 11



These problems can be solved by using an emitter-follower buffer to drive the MOSFET gate, see Figure 11. The transistors Q_2 and Q_3 would provide ample drive current to quickly turn the MOSFET Q_1 on and off.

One thing to consider when sizing the filter capacitor C_1 is to ensure it is large enough to provide ample energy during the initial start-up phase of the HV91 power supply. Otherwise, the V_{DD} voltage will droop and the HV91 would go into an under-voltage lockout condition.

References:

- 1) Virginia Power Electronics Center,
Bradley Department of Electrical Engineering,
Virginia Polytechnic Institute and State University,
Blacksburg VA 24061.
- 2) Available from publisher or see footnote 5.
- 3) Only available from publisher: TESLAcO, 10 Mauchly,
Irvine CA 92718 (714)727-1960.
- 4) Books with ISBN numbers can be ordered from any
bookstore. All the books in this list except
the TESLAcO book can also be acquired from:
E.J. Bloom Assoc. Educational Division, 115 Duran
Dr., San Rafael CA 94903-2317 (415)492-1239.
They generally have them in stock.
- 5) Magnetic assemblies for the converters supplied by:
GFS Manufacturing, Inc. 140 Crosby Rd.,
Dover, NH 03820-1409 (603)742-4375.

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