KSZ8081RNB

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8081RNB. These checklist items should be followed when utilizing the KSZ8081RNB in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 11. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

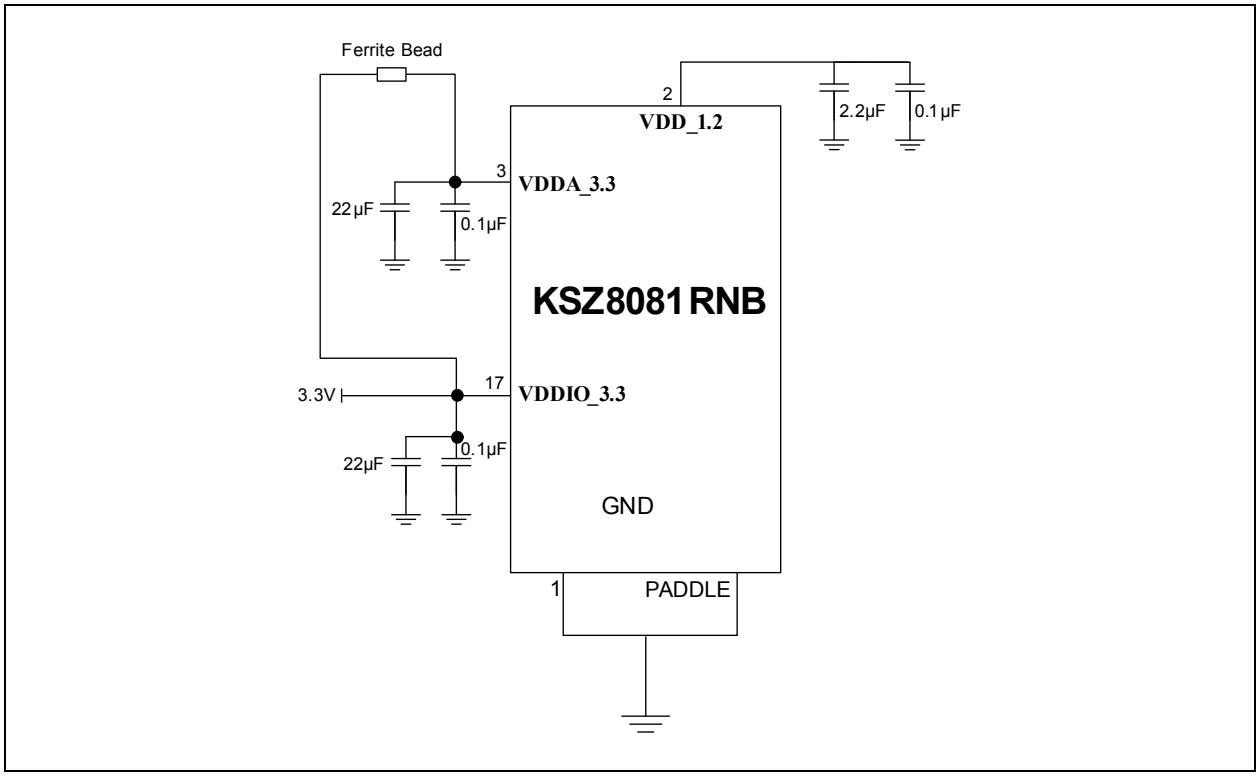
- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- The analog supply (**VDDA_3.3**) is located on pin 3, and requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100-MHz) ferrite bead is used.
- The **VDDA_3.3** pin should include 0.1-µF and 22-µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pin 17 (**VDDIO**) is a variable supply voltage for the I/O pads. It should be connected to the +3.3V, 2.5V, or 1.8V supply. A bulk capacitor is needed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors need to be placed as close to the part as possible to reduce high frequency noise being injected through EMI interference.
- Pin 2 is the internally generated 1.2V core power rail. Connect 2.2-µF and 0.1-µF capacitors from Pin 2 to ground using wide traces as appropriate for power distribution. Do not connect an external 1.2V source.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



Caution: This +1.2V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

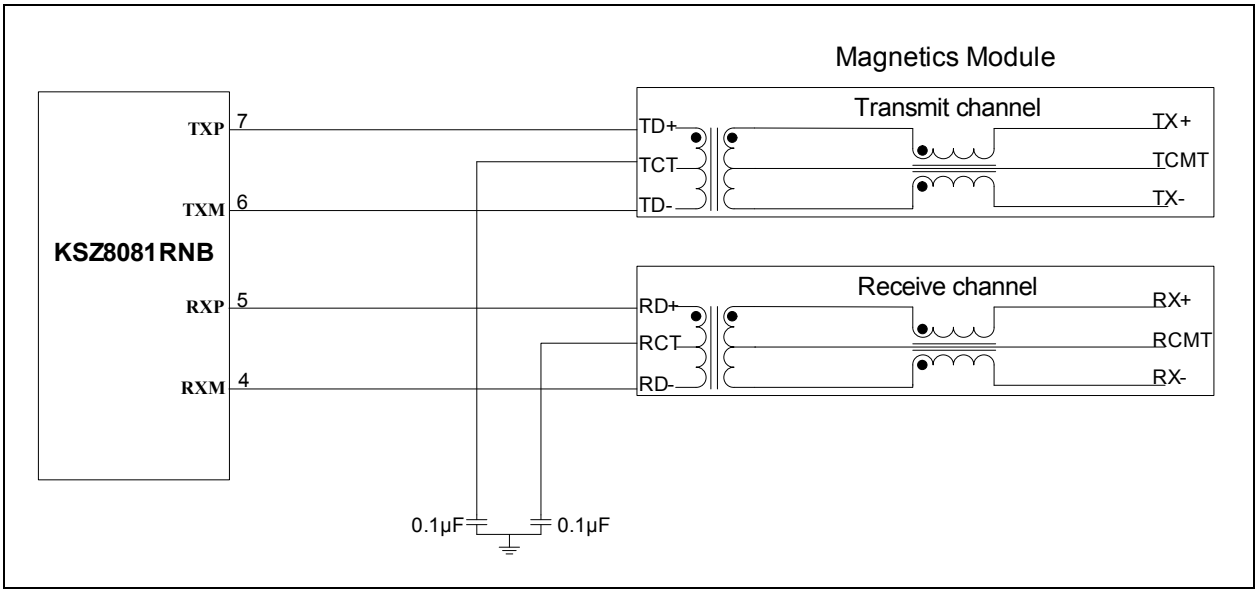
4.0 ETHERNET SIGNALS

4.1 PHY Interface

- **TXP** (pin 7): This pin is the transmit twisted pair output positive connection from the internal PHY. It has an internal terminator and a bias, so it can be directly connected to the transmit channel of the magnetics and no external terminator and bias are needed.
- **TXM** (pin 6): This pin is the transmit twisted pair output negative connection from the internal PHY. It has an internal terminator and a bias, so it can be directly connected to the transmit channel of the magnetics and no external terminator and bias are needed.
- **RXP** (pin 5): This pin is the receive twisted pair input positive connection to the internal PHY. It has an internal terminator and a bias, so it can be directly connected to the receive channel of the magnetics and no external terminator and bias are needed.
- **RXM** (pin 4): This pin is the receive twisted pair input negative connection to the internal PHY. It has an internal terminator and a bias, so it can be directly connected to the receive channel of the magnetics and no external terminator and bias are needed.

For transmit and receive channel connections details, refer to Figure 4-1.

FIGURE 4-1: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS



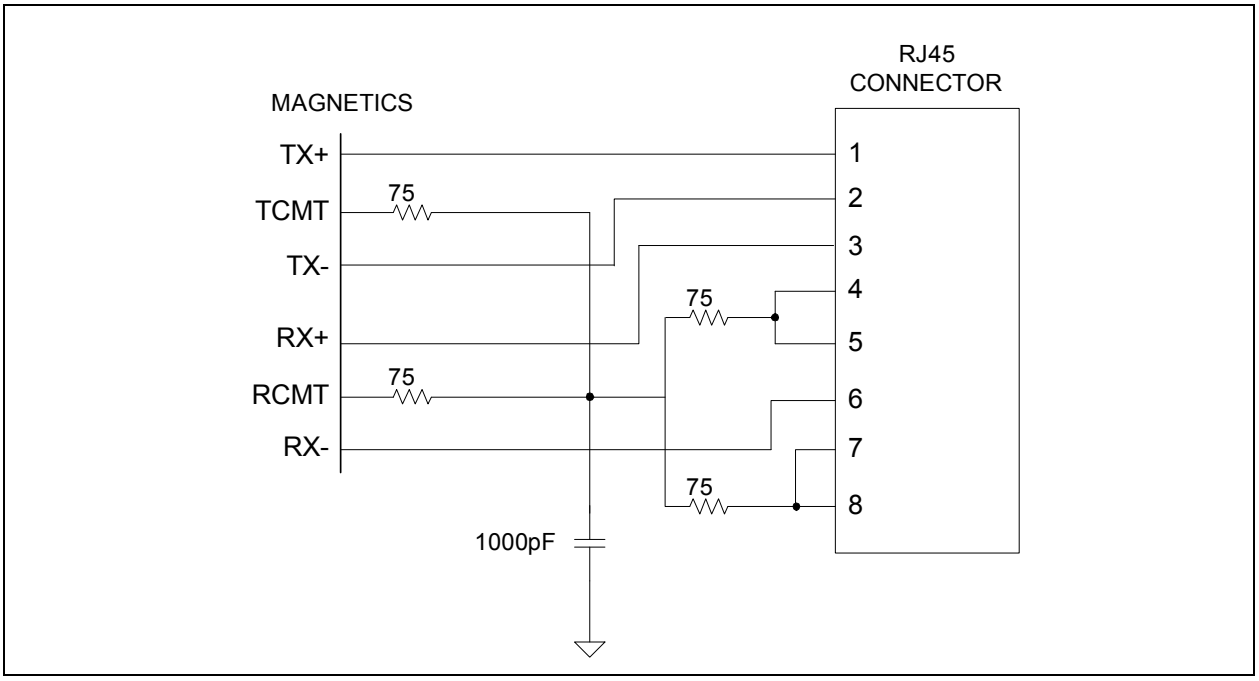
4.2 Magnetics Connection

- The center tap connection on the KSZ8081RNB side for the transmit channel only connects a 0.1-µF capacitor to GND and no bias is needed.
- The center tap connection on the KSZ8081RNB side for the receive channel only connects a 0.1-µF capacitor to GND and no bias is needed.
- The center taps of the magnetics of the transmit and receive channels should not be connected together.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75-Ω resistor through a 1000-pF, 2-KV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75-Ω resistor through a 1000-pF, 2-KV capacitor to chassis ground.
- Only one 1000-pF, 2-KV capacitor to chassis ground is required. It is shared by both TX and RX center taps.
- MDI Connections:
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 7) of the KSZ8081RNB.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to TXM (pin 6) of the KSZ8081RNB.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 5) of the KSZ8081RNB.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to RXM (pin 4) of the KSZ8081RNB.
- MDIX Connections:
  - Pin 3 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 7) of the KSZ8081RNB.
  - Pin 6 of the RJ45 is TX- and should trace through the magnetics to TXM (pin 6) of the KSZ8081RNB.
  - Pin 1 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 5) of the KSZ8081RNB.
  - Pin 2 of the RJ45 is RX- and should trace through the magnetics to RXM (pin 4) of the KSZ8081RNB.
- When using the KSZ8081RNB device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (that is, the one where the TX and RX channels are identical) is required.

4.3 RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000-pF, 2-KV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9-Ω resistors. The common connection of these resistors should be connected through a third 49.9-Ω resistor to the 1000-pF, 2-KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9-Ω resistors in parallel perform like a 25-Ω resistor. The 25-Ω resistor in series with the 49.9-Ω resistor causes the entire circuit to function as a 75-Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75-Ω resistor in series with the 1000-pF, 2-KV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000-pF, 2-KV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9-Ω resistors. The common connection of these resistors should be connected through a third 49.9-Ω resistor to the 1000-pF, 2-KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9-Ω resistors in parallel perform like a 25-Ω resistor. The 25-Ω resistor in series with the 49.9-Ω resistor causes the entire circuit to function as a 75-Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75-Ω resistor in series with the 1000-pF, 2-KV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground.

FIGURE 4-2: RJ45 CONNECTIONS



5.0 CLOCK CIRCUIT

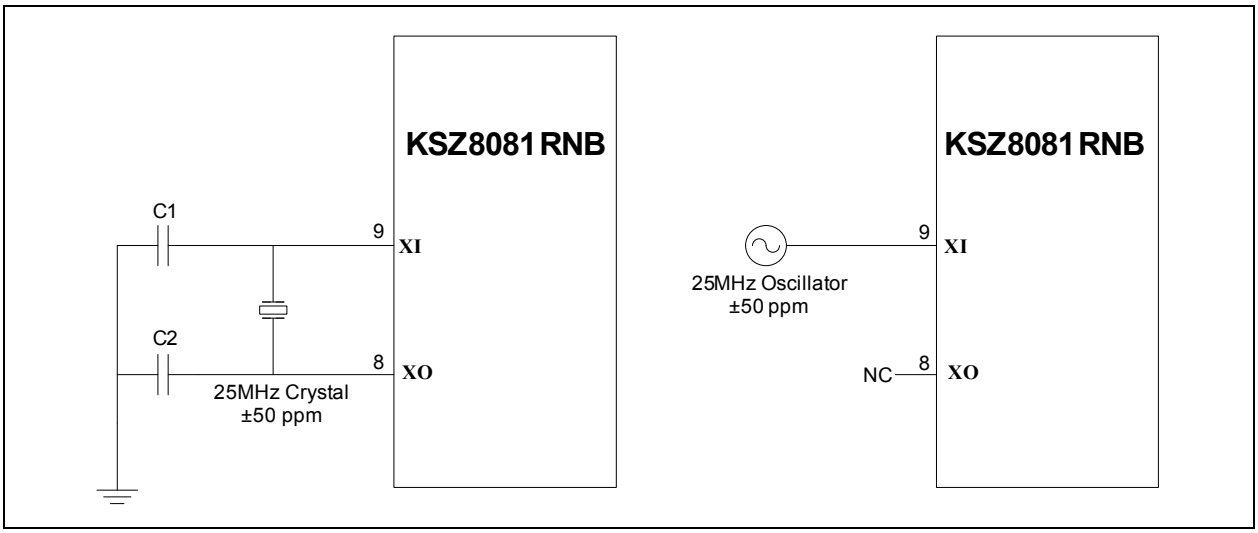
5.1 Crystal and External Clock Connection

A 25.000-MHz (±50ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the KSZ8081RNB data sheet.

- **XI** (pin 9) is the clock circuit input for the KSZ8081RNB. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 8) is the clock circuit output for the KSZ8081RNB. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system dependent, based on the CL spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternately, a 25.000-MHz, 3.3-V clock oscillator may be used to provide the clock source for the KSZ8081RNB. When using a single ended clock source, **XO** (pin 8) should be left floating as a No Connect (NC).

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS



6.0 DIGITAL INTERFACES

6.1 RMII Interface

- When utilizing either an external RMII MAC interface, the following table indicates the proper connections for the 10 signals, including two management pins (MDC and MDIO).

TABLE 6-1: RMII CONNECTIONS

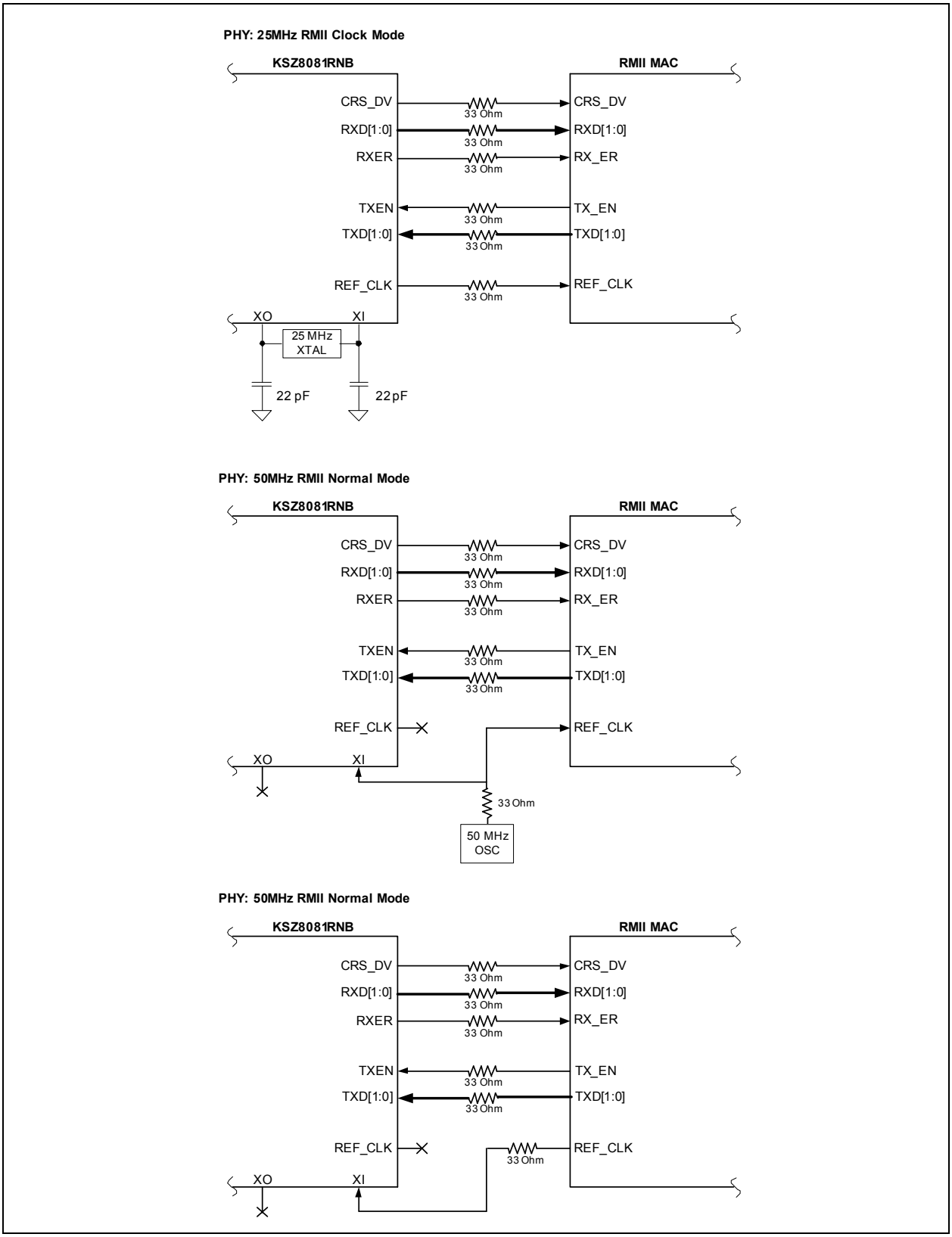
From KSZ8081RNB:	Connects to RMII MAC Device:
RXD0 (pin 16)	RXD<0>
RXD1 (pin 15)	RXD<1>
RXER (20)	RX_ER
CRS_DV (pin 18)	CRS_DV
REF_CLK (pin 19)	REF_CLK
TXD0 (pin 24)	TXD<0>
TXD1 (pin 25)	TXD<1>
TXEN (pin 28)	TX_EN
MDIO (pin 11)	MDIO
MDC (pin 12)	MDC

- Provisions should be made for series terminations for all RMII interface pins. Series resistors enable the designer to closely match the output driver impedance of the KSZ8081RNB and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

- The KSZ8081RNB offers two RMII clock modes:
  - 25-MHz RMII Clock Mode (crystal or external oscillator) (default mode of operation)
  - 50-MHz RMII Normal Mode (external oscillator only)

- Example RMII connection diagrams for 50-MHz and 25-MHz clock modes are detailed in Figure 6-1. For additional details on clock requirements, refer to Section 5.1, Crystal and External Clock Connection. For additional details on register and strapping configuration, refer to the KSZ8081RNB datasheet.

FIGURE 6-1: RMII CONNECTION DIAGRAMS



6.2 Required External Pull-ups

- When using the KSZ8081RNB MDC/MDIO management pins, a pull-up resistor from 1-KΩ to 10-KΩ on the **MDIO** signal (pin 11) is required, based on an **MDC** frequency from 10-MHz to <= 1-MHz.
- If used, the **INTRP** (pin 21) requires a 4.7-KΩ external pull-up resistor since this output is an open drain. If the **INTRP** pin is not used then this pin can float.

7.0 STARTUP

7.1 Reset Circuit

RST# (pin 32) is an active-low reset input. This signal resets all logic and registers within the KSZ8081RNB. A hardware reset (**RST#** assertion) is required following power-up. Please refer to the latest copy of the KSZ8081RNB data sheet for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ8081RNB when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

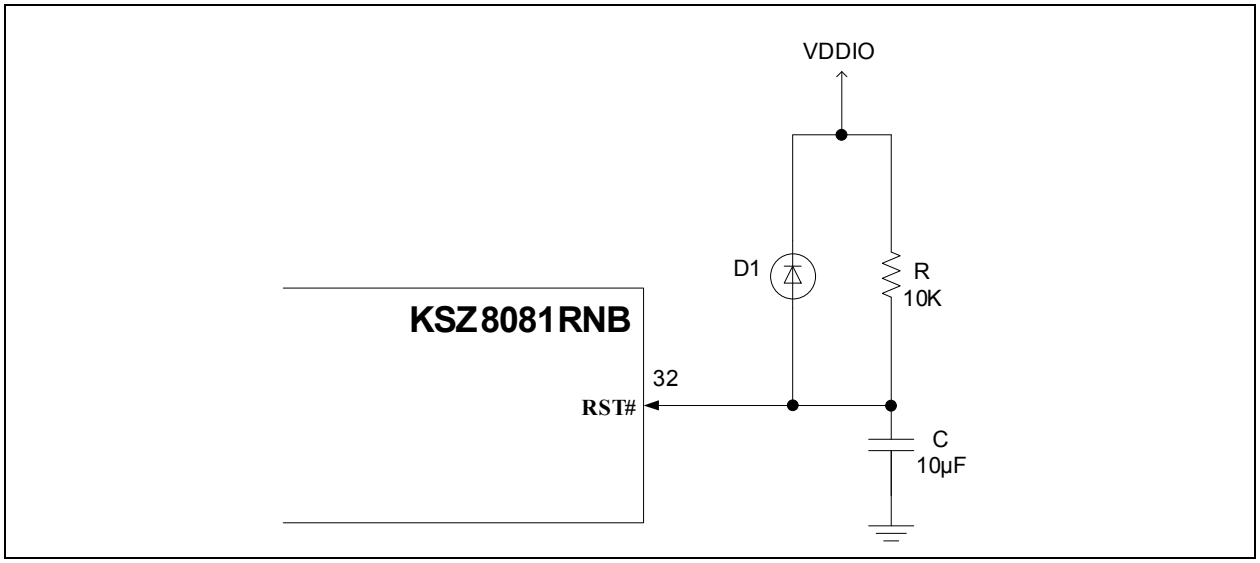
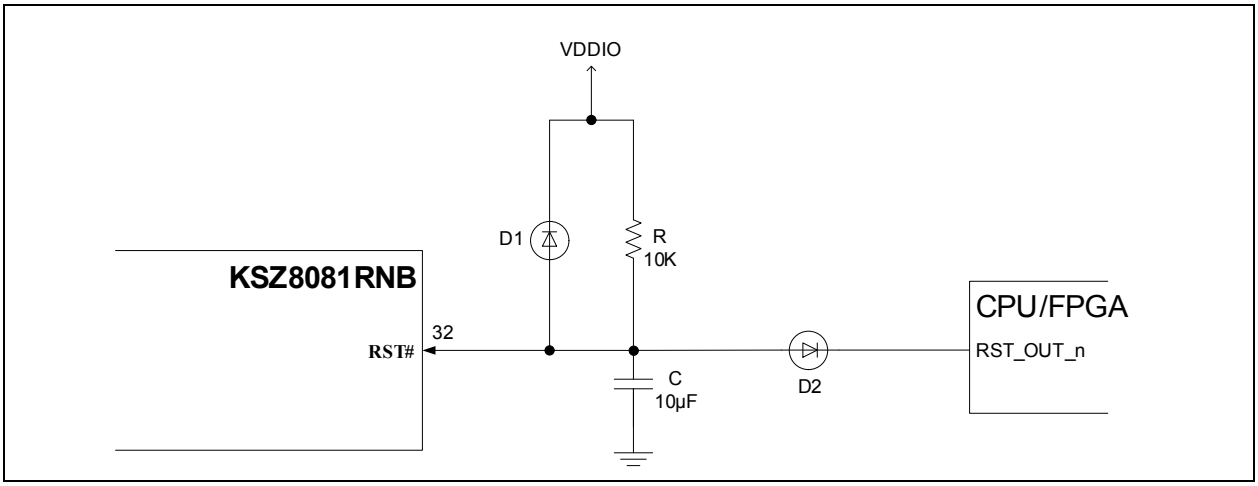


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (RST_OUT_n) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be directly connected.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Configuration Mode Pins (Strapping Options)

The configuration mode pins of the KSZ8081RNB (**CONFIG[2:0]**) control the default configuration of the 10/100 PHY. Speed, duplex, auto-negotiation, and power-down functionality can be configured through these pins. The value of these three pins are latched upon power-up and reset. In some systems, the MAC receive input pins may drive high during power-up or reset and consequently cause the PHY strap-in pins on the RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to ISOLATE mode or is not configured with an incorrect PHY address. Refer to the KSZ8081RNB data sheet for complete details for the operation of these pins.

7.3 LED Pins

- The KSZ8081RNB provides two LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220Ω-470Ω). Refer to the KSZ8081RNB data sheet for further details on how to connect each pin for correct operation.
- The LED functionality signal pins are shared with the following pin strapping functions:
  - LED0 is shared with **NWAYEN** on pin 30 for KSZ8081RNB.
  - LED1 is shared with **SPEED** on pin 31 for KSZ8081RNB.

Note 1: For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the **SPEED** and **NWAYEN** strapping pins are functional with a 4.7KΩ pull-up to 1.8V VDDIO (or be floated) for a value of '1', and with a 1.0KΩ pull-down to ground for a value of '0'.

2: If using RJ45 jacks with integrated LEDs and 1.8V VDDIO, a level shifting is required from LED 3.3V to 1.8V. In this case, a bipolar transistor or a level shifting device can be used.

8.0 MISCELLANEOUS

8.1 REXT Resistor

The **REXT** pin on the KSZ8081RNB must connect to ground through a 6.49-KΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100 Ethernet physical device.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a zero ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7-22 µF) for each power plane.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure **VDDA_3.3** and **VDDIO** are in the range 3.135V to 3.465V and a 22-µF capacitor is on each pin. • **VDD_1.2** requires two 0.1-µF capacitors.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY Interface"	Verify that the TX and RX pin do not contain any termination resistors.		
	Section 4.2, "Magnetics Connection"	Verify that the center taps are connected to the GND using separate 0.1-µF capacitors on the KSZ8081MLX device side, and are terminated with 75-Ω resistors through a 1000-pF, 2-kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.3, "RJ45 Connector"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000-pF, 2-kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Clock Connection"	Verify usage of 25-MHz ±50ppm crystal.		
Section 6.0, "Digital Interfaces"	Section 6.1, "RMII Interface",Section 6.2, "Required External Pull-ups"	Confirm proper RMII signals between MAC and PHY interface with correct termination resistors (33Ω) and external pull-up for MDIO signal.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2, "Configuration Mode Pins (Strapping Options)"	In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1-KΩ pull-downs on the PHY strap pins.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "REXT Resistor"	Confirm proper REXT resistor (6.49 KΩ, 1.0%).		
	Section 8.2, "Other Considerations"	• Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the chip ground instead of the digital ground. • Incorporate sufficient power plane bulk capacitors (4.7-22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002779A (08-07-18)	Initial release	

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