

LAN7500/LAN7500i Layout Guidelines

1 Introduction

This layout guide provides important information about the PCB layout requirements for the LAN7500/LAN7500i.

The LAN7500/LAN7500i is a high performance Hi-Speed USB 2.0 to 10/100/1000 Ethernet controller. With applications ranging from embedded systems, set-top boxes and PVR's, to USB port replicators, USB-to-Ethernet dongles and test instrumentation, the LAN7500/LAN7500i is a high performance and cost competitive USB-to-Ethernet connectivity solution.

The LAN7500/LAN7500i contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY, Hi-Speed USB 2.0 device controller, TAP controller, EEPROM controller, and a FIFO controller with a total of 32 KB of internal packet buffering. The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The LAN7500/LAN7500i implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u and IEEE 802.3ab standards. ARP and NS offload is also supported.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

1.1 References

LAN7500/LAN7500i Datasheet

LAN7500/LAN7500i Reference Design

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2 General PCB Layout Guidelines

2.1 Power Supply Considerations

1. Ensure adequate power supply ratings. Verify that all power supplies and voltage regulators can supply the amount of current required.
2. Power supply output ripple should be limited to less than 50 mV.
3. Noise levels on all power planes and ground planes should be limited to less than 50 mV.
4. Ferrite beads should be rated for 4 – 6 times the amount of current they are expected to supply. Any de-rating over temperature should also be accounted for.

2.2 PCB Decoupling

1. Every high-speed semiconductor device on the PCB assembly requires decoupling capacitors. One decoupling cap for every power pin is necessary.
2. Decoupling capacitor value is application dependent. Typical decoupling capacitor values may range from 0.1 μ F to 0.001 μ F.
3. The total decoupling capacitance should be greater than the load capacitance presented to the digital output buffers.
4. Typically, Class II dielectric capacitors are chosen for decoupling purposes. The first choice would be an X7R dielectric ceramic capacitor for its excellent stability and good package size vs. capacitance characteristics. The designer's second choice may be the X5R dielectric for its excellent stability. However, the X5R may be somewhat limiting in the package size vs. capacitance characteristics. For a third choice, one may look to the Y5V dielectric. However, this Class III dielectric is less stable and the package size vs. capacitance characteristics may be problematic for most applications. Low inductance is of the utmost importance when considering decoupling capacitor characteristics.
5. Each decoupling capacitor should be located as close as possible to the power pin that it is decoupling.
6. All decoupling capacitor leads should be as short as possible. The best solution is plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.

2.3 PCB Bypassing

1. Bypass capacitors should be placed near all power entry points on the PCB. These caps will allow unwanted high-frequency noise from entering the design; the noise will simply be shunted to ground.
2. Bypass capacitors should be utilized on all power supply connections and all voltage regulators in the design.
3. Bypass capacitor values are application dependent and will be dictated by the frequencies present in the power supplies.
4. All bypass capacitor leads should be as short as possible. The best solution is plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.

Figure 2.1 illustrates an example of PCB bypassing techniques.

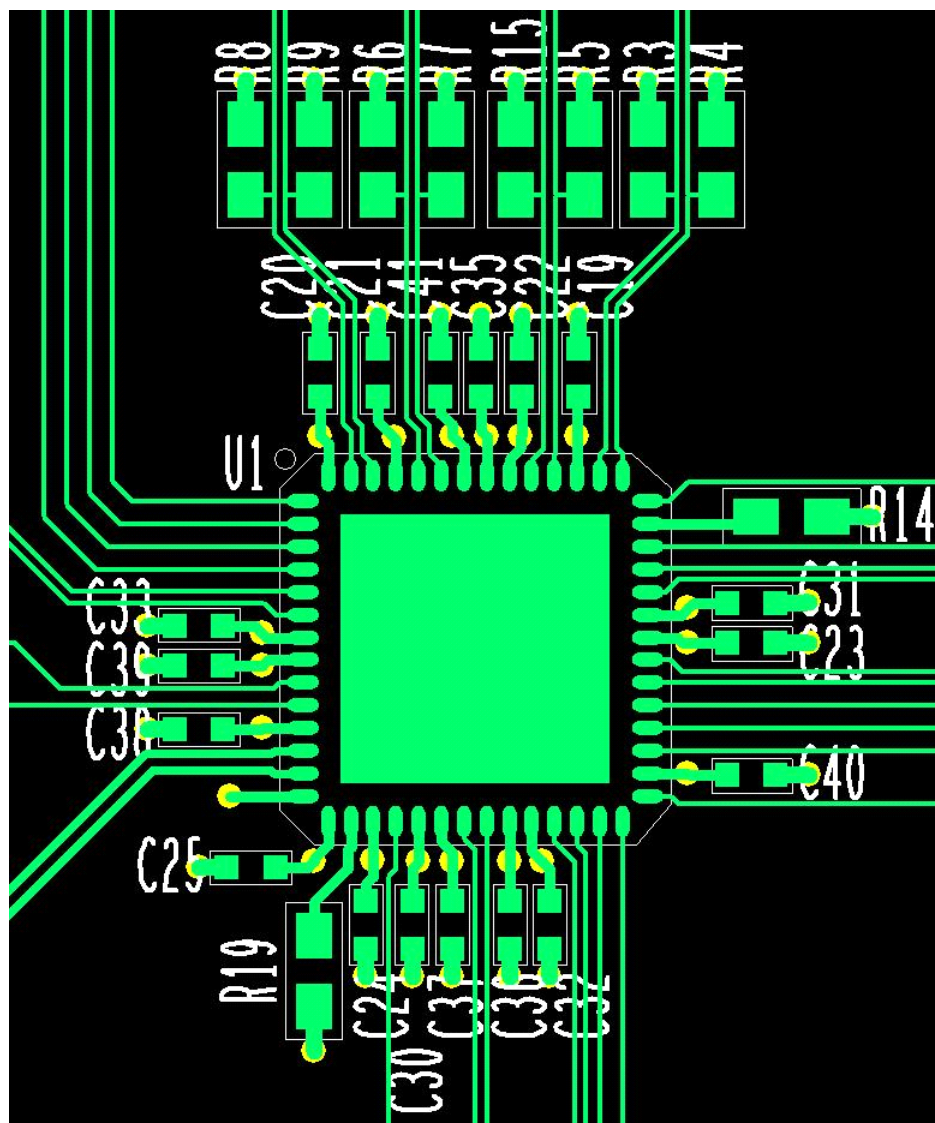


Figure 2.1 PCB Bypassing

2.4 PCB Bulk Capacitors

1. Bulk capacitors must be properly utilized in order to minimize switching noise. Bulk capacitance helps maintain constant DC voltage and current levels.
2. Bulk capacitors should be utilized on all power planes and all voltage regulators in the design.
3. All bulk capacitor leads should be as short as possible. The best solution is plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance.

4. In general, good design practices dictate that whenever a ferrite bead is used in the circuit, bulk capacitance should be placed on each side of the ferrite bead.
5. In the case where a ferrite bead is used on the USB connector to filter the VCC, the use of bulk capacitance on the USB connector side is not recommended. This is an attempt to limit the in-rush current of the USB circuitry. SMSC does recommend the use of a 4.7 uF bulk capacitor on the in-board side of the ferrite bead. Refer to the latest LAN7500/LAN7500i reference schematic for details.

2.5 PCB Layer Strategy

1. SMSC strongly recommends using at least a 4 layer PCB for all high-speed Ethernet LAN designs.
2. The typical PCB stack-up uses a signal layer on the top (component side) layer, a solid, contiguous ground plane layer on Layer 2, a solid power plane layer on Layer 3 and another signal layer on Layer 4. Layer 1 is considered the prime layer for critical routes and components because of the solid digital ground plane directly beneath it and Layer 1 also requires no vias to connect components located on Layer 1.
3. All PCB traces (especially high-speed and critical signal traces) should be routed on Layer 1 next to the solid, contiguous ground plane layer. These traces must have a continuous reference plane for their entire length of travel. This will improve EMC performance and signal integrity issues.
4. The implementation of an Ethernet chassis ground plane separate from the digital ground plane is required.
5. Avoid creating ground loops in the PCB design and the system design.
6. In order to facilitate routing and minimize signal cross talk issues, adjacent layers in a multi-layer design should be routed orthogonal.

2.6 Signal Integrity Concerns

1. Provide AC terminations for all high-speed switching signals and clock lines when required. Locate these terminations at the load end of the trace. This design issue becomes more critical with longer length traces on the PCB.
2. Provide impedance matching series terminations to minimize ringing, overshoot and undershoot on critical signals (address, data & control lines). These series terminations should be located at the driver end of the trace as apposed to the load end of the trace. This design issue becomes more critical with longer length traces on the PCB.
3. Minimize the use of vias throughout the design. Vias add capacitance to signal traces.
4. Be certain to review the entire PCB design for any traces crossing over any reference plane cuts. This will more than likely create an EMC occurrence. Refer to LANCheck reference document number ER226303, "EMI Reduction Document, PCB Design Guidelines, Reference Plane Cuts" for further information.
5. In general, review all signal cross talk design rules to avoid cross talk problems. Use the 3-W rule to provide enough trace separation to avoid cross talk problems.
6. Guard traces may also be utilized to minimize cross talk problems.

2.7 Component Guidelines

1. Verify that all components in the design meet application requirements. For instance, if the application requires operation in the industrial temperature range, be certain that all the other devices in the design (in addition to the LAN device) meet this requirement. This should include crystals, magnetics, ferrite beads, etc.

2. If the application requires operation to a specific high ESD level, be certain that all the other devices in the design (in addition to the LAN device) meet this requirement. This should include bypass caps (usually 2KV for Ethernet applications), magnetics, etc.
3. Review all surface mount components for proper sizing with respect to power dissipation.
4. Locate any bias resistor on the component side of the PCB.
5. In general, locate any bias resistor as close as possible to the device bias pin. Route the bias resistor with short, wide traces and connect immediately to the ground plane.
6. Do not run any traces under bias resistors. In general, it's a good PCB design rule practice to not run any traces in between any surface mount pads (resistors, capacitors, ferrite beads, etc.).

2.8 PCB Trace Considerations

1. PCB traces should be routed using 45 degree corners when changing directions. 90 degree corners should never be used.
2. PCB traces should be designed with the proper width for the amount of current they are expected to supply. The use of mini-planes in a local area on either the top or bottom layers will ensure proper current supply.
3. All component leads to any power plane or ground plane should be as short as possible. The best solution is plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 mils in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc.

2.9 Crystal Circuitry

1. Locate all crystal circuit components on the top layer. This will reference all these components and their traces to the same digital ground plane.
2. As best as possible, isolate all the crystal components and traces from other signals. The crystal oscillator is sensitive to stray capacitances and noise from other signals. The crystal oscillator may also disturb other signals and cause EMI noise.
3. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB and VBUS power lines. The load capacitors return path should be to the digital logic power supply ground plane.
4. PCB traces from the LAN7500/LAN7500i to the crystal, resistors and capacitors should be matched in length, as close as possible, while maintaining the shortest possible path. Length matching should take a higher priority over minimization of the path length.
5. Verify that the crystal circuit operates within specification (± 50 PPM) over the entire operating range of the application. This includes temperature, time and application tolerance.

Figure 2.2 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from USB lines.

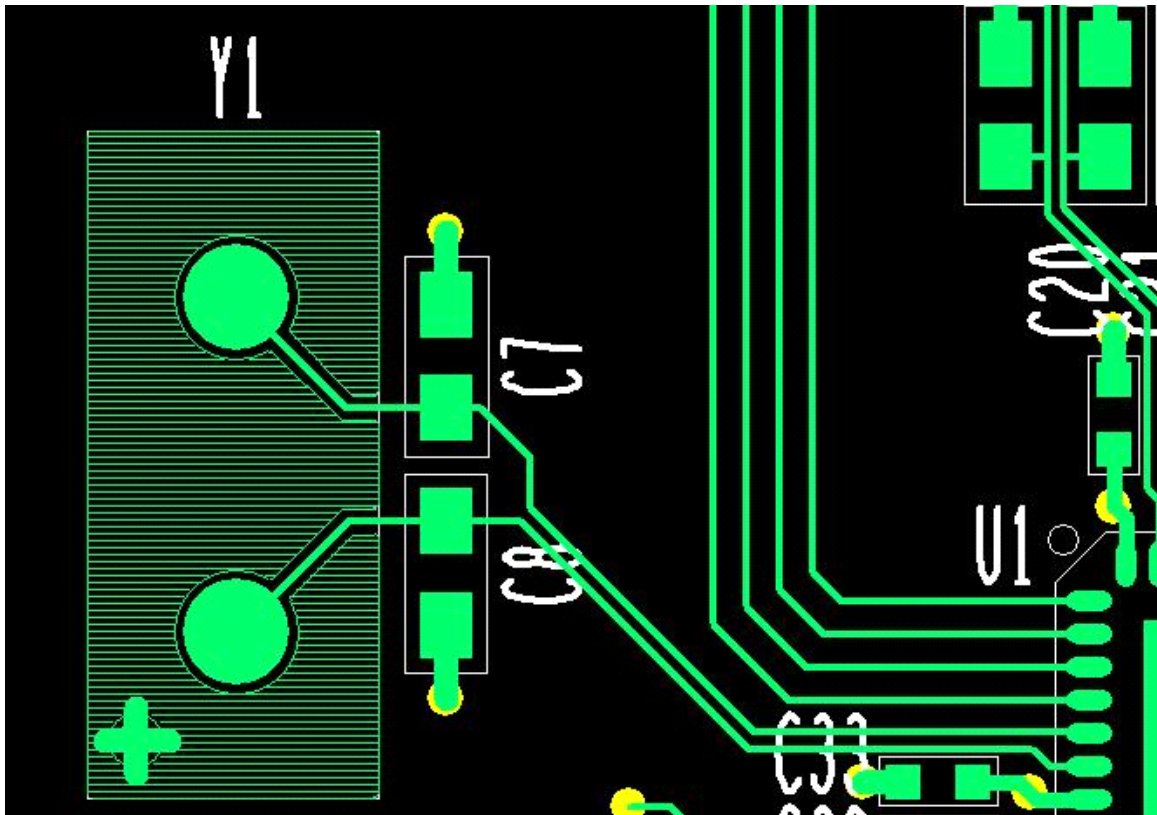


Figure 2.2 Crystal Oscillator Component Layout

2.10 VIAS in Ground Flag (Exposed Pad)

There are 16 thermal vias connecting the pad to the ground plane. Each via has a 12 mil plated hole with a 24 mil annular ring. Tolerances are +/- 2 mils. Vias are completely connected to the ground plane, not cross-hatched. Via spacing is 60 mils center to center with a 36 mil gap between edges of the annular rings. Vias are tented with solder mask.

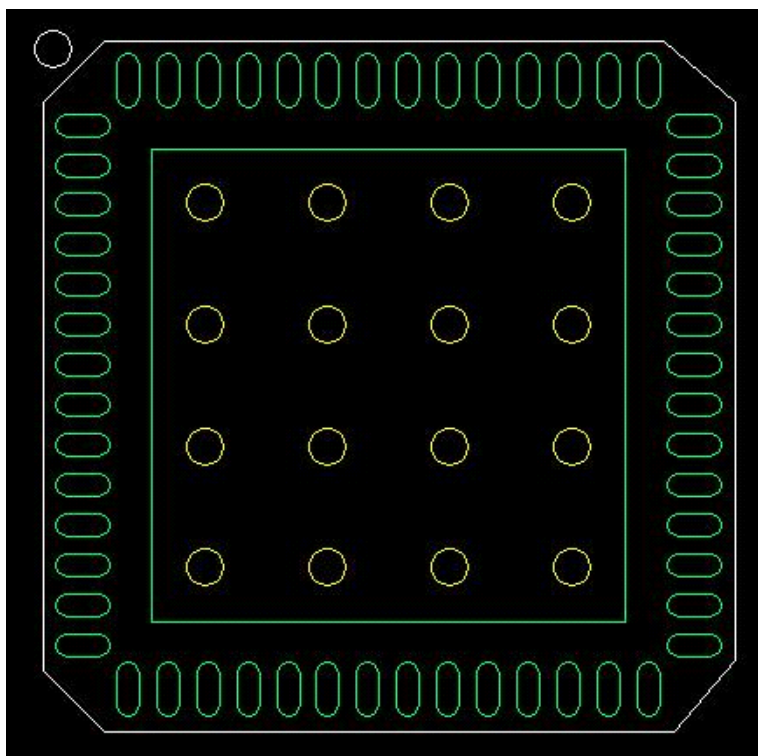


Figure 2.3 Vias In Ground Flag (Exposed Pad)

2.11 Miscellaneous

1. Review all PCB connector interfaces for proper shielding and grounding to ensure good EMC performance. An improperly designed connector circuit may allow EMC energy to radiate from the system.

3 Recommended PCB Stack-up

3.1 PCB Recommended Stack-up

The following section outlines the recommended PCB stack-up for good EMC performance. Depending upon the specific application and EMC testing required, many stack-ups and configurations may work for the designer. However, for the highest EMC level of testing, certain PCB stack-ups perform better than others. Incorrect stack-ups may increase EMC emissions. If the product being designed must pass higher EMC test levels, the designer should consider all design points that will give his product the best chance of passing those EMC levels.

3.2 4-Layer Stack-ups

Figure 3.1 represents a 4-layer stack-up. Each signal layer has an adjacent reference plane.

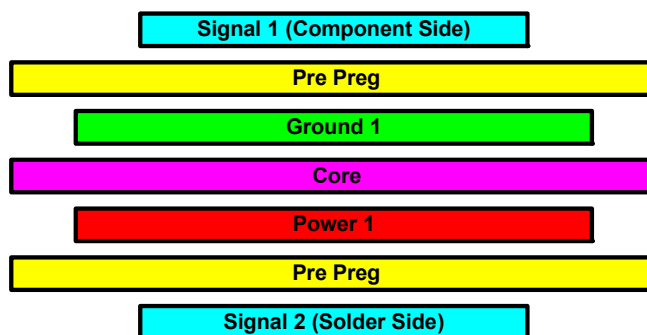


Figure 3.1 4 Layer Stack-Up

As a final recommendation to customers who require EMC testing of their product, determine what EMC test levels are required as early as possible and design the PCB accordingly. Begin EMC testing as soon as possible in the design cycle. Test early and test often. Waiting until the end of the design cycle to begin EMC testing may result in not achieving passing levels with the current design. With the added pressure of impending release schedules, the end of the design cycle is not the time to analyze and correct EMC problems. The correct time in the design cycle to combat EMC problems is in the very beginning, during schematic design and PCB design.

4 USB Layout Guideline

4.1 Controlled Impedance for USB Traces

The USB 2.0 specification requires the USB DP/DM traces maintain a nominal 90 Ohms differential impedance (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). A continuous ground plane is required directly beneath the DP/DM traces that extends at least 5 times the spacing width to either side of DP/DM lines. Maintain close to 90 Ohms differential impedance. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be calculated. Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance, a range of 42 to 78ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

Figure 4.1 shows DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

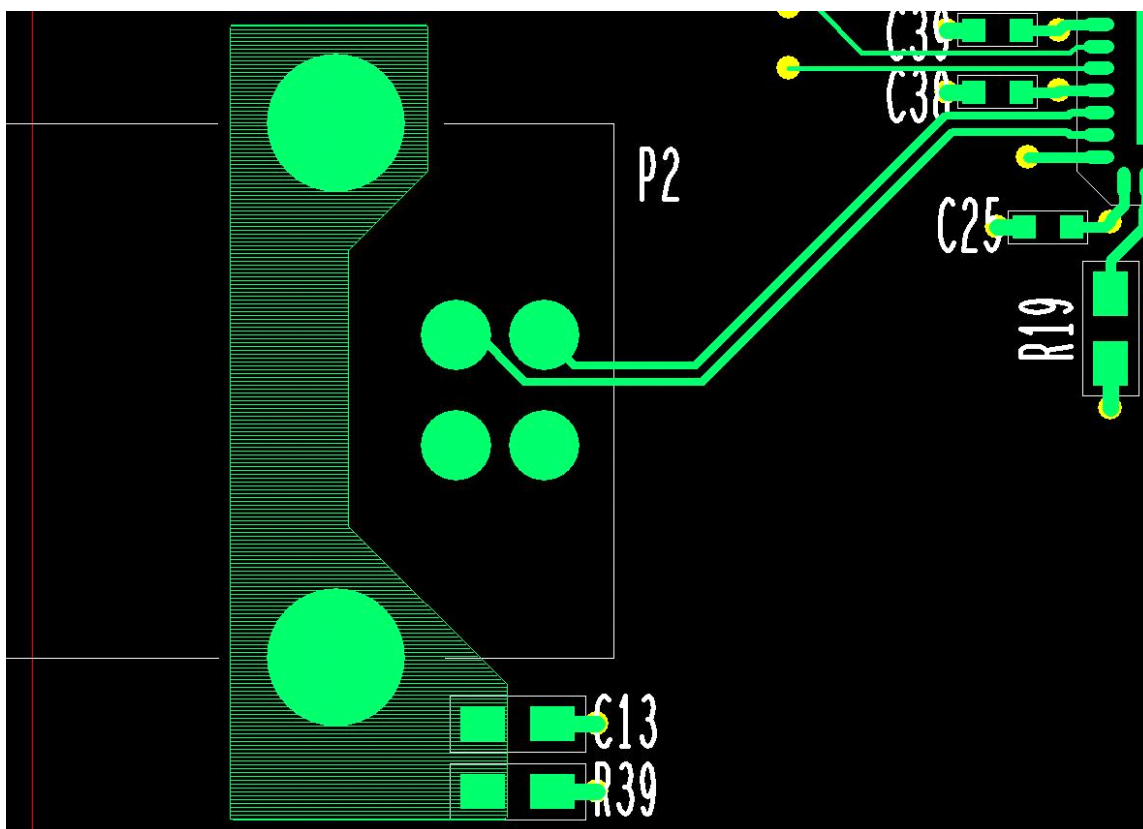


Figure 4.1 Example of Routing DP/DM to Type B Connector

4.2 Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of parts-to-lines that is greater than or equal to 5 times the distance of the spacing between the traces. Do not route differential pairs under parts. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM traces over solid plane, not over power planes.

4.3 Isolated Shielding on the USB Connector

LAN7500/LAN7500i incorporates a USB peripheral device PHY. [Figure 4.2](#) shows the B-connector housing DC isolated, but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds.

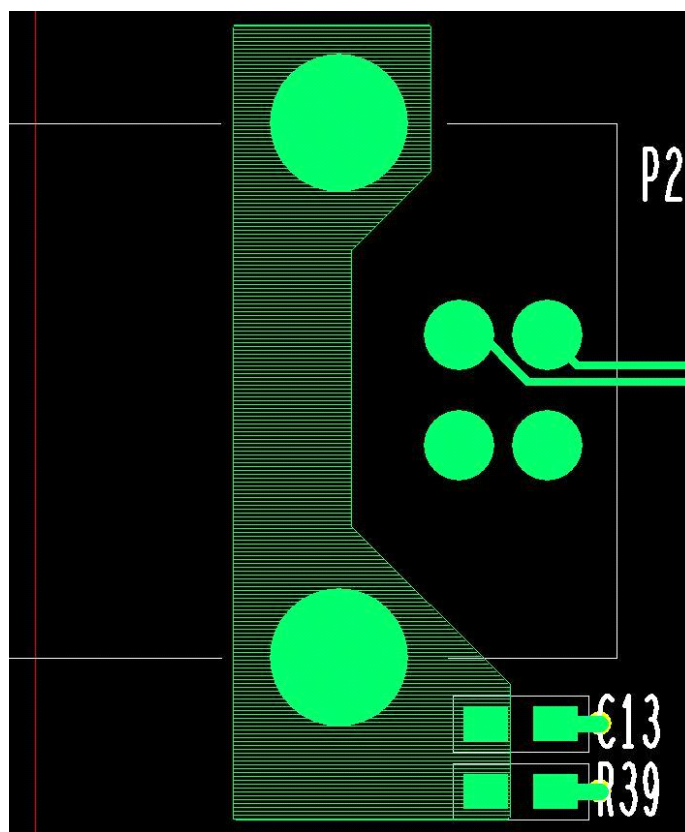


Figure 4.2 Connections to Shield of Type B USB Connector

4.4 USBRBIAS

The USBRBIAS resistor sets an internal current source reference. Thus, the USBRBIAS pin is a high impedance node and any noise induced on the USBRBIAS traces will directly impact internal current references, negatively degrading the eye-diagram quality. The USBRBIAS resistor should be placed

close to the USBRBIAS pin and the ground return should be short and direct to the ground plane. If possible, resistor traces should be very short and isolated from nearby traces.

5 Ethernet Layout Guideline

5.1 Ethernet Differential Pairs

1. Each TRxP/TRxN signal group (where x=0-3) should be routed as differential pairs. This includes the entire length of travel of the traces from the RJ45 connector to the LAN device.
2. A single differential pair should be routed as close together as possible. Typically, when beginning the impedance calculation, the smallest trace space (4 – 5 mils) is selected. The trace width is then adjusted to achieve the necessary impedance.
3. Differential pairs should be constructed as 100 ohm, controlled impedance pairs.
4. Differential pairs should be routed away from all other traces. Try to keep all other high-speed traces at least 0.300" away from the Ethernet front end.
5. Each trace of the differential pair should be matched in length.
6. The differential pairs should be as short in length as possible.
7. The use of vias is to be minimized. If vias are used, keep them to a minimum and always match vias so the differential pairs are balanced.
8. Layer changes are to be minimized. Keep the differential pairs referenced to the same power/ground plane whenever possible.
9. In general, when routing gigabit Ethernet's 4 differential pairs into an RJ45 connector, at least one pair will need a via to the opposite external layer. In this case, it must be assured that the routing on the other side of the board (usually layer 4) passes over a contiguous reference plane that has a low impedance to ground. Never route over a plane boundary.
10. For optimum immunity, route each pair as far away from each other as possible.
11. Always reference any terminations to the same reference plane as the differential routes.
12. Precedence should be given to differential pair routing. Terminations should be added after the routing is determined. The terminations should simply be "dropped" onto the differential routing.
13. All resistive terminations in the Ethernet front end should have values with 1.0% tolerances.
14. All capacitive terminations in the Ethernet front end should have tight tolerances and high quality dielectrics (NPO).
15. For optimum separation, experimentation with inserting a ground plane island between the differential pairs may be performed. A separation of 3–5 times the dielectric distance should be maintained from this ground plane to any of the traces.
16. This same separation technique described above can be used to separate different Ethernet ports if port cross talk is an issue. A ground plane can be inserted between Ethernet channels. The separation space between the two channels should be as wide as possible. Again, a separation of 3–5 times the dielectric distance should be maintained from this ground plane to any of the traces.

Figure 5.1 illustrates chip-to-magnetics differential pair routing. Figure 5.2 and Figure 5.3 illustrate magnetics-to-RJ45 differential pair routing.

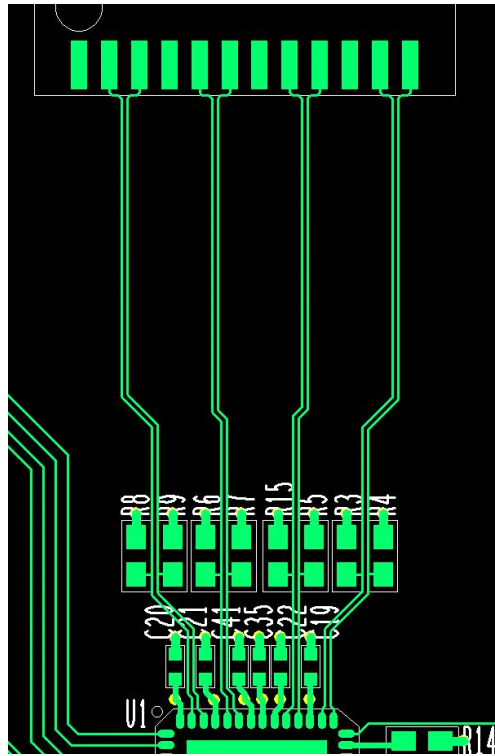


Figure 5.1 Chip-to-Magnetics Differential Pair Routing

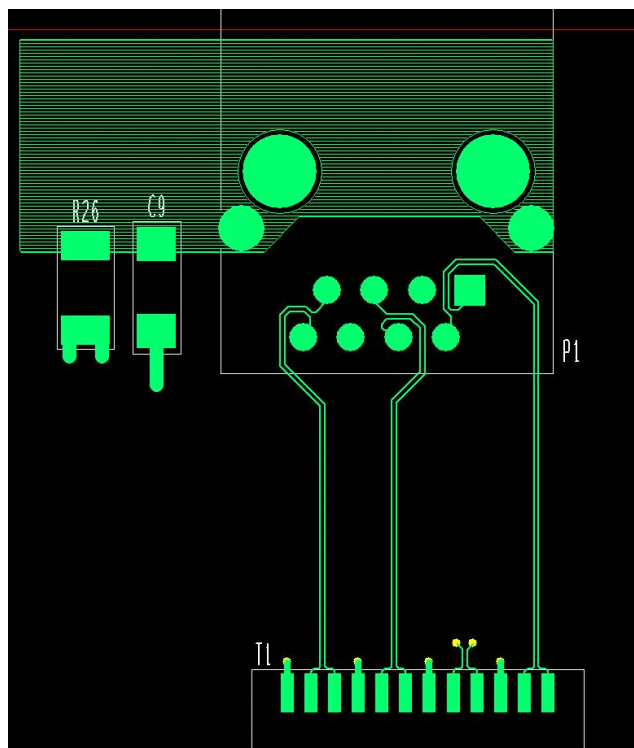


Figure 5.2 Magnetics-to-RJ45 Differential Pair Routing - Board Top

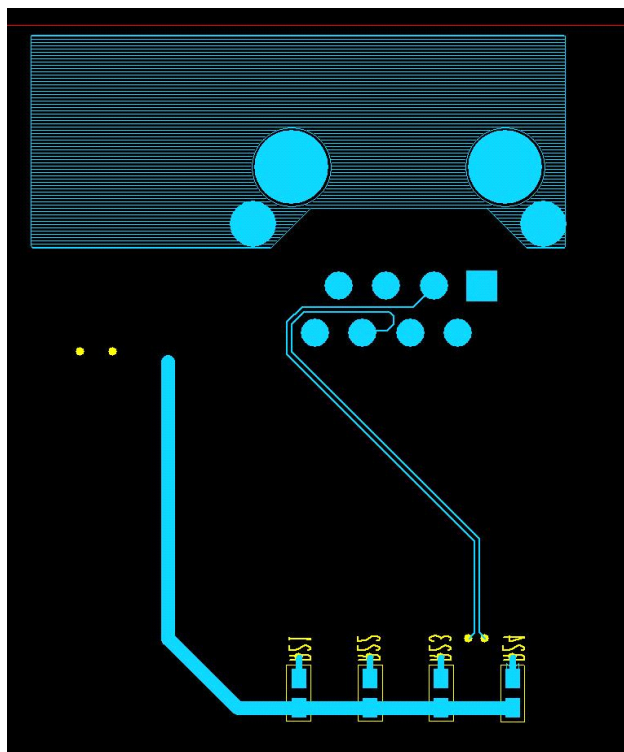


Figure 5.3 Magnetics-to-RJ45 Differential Pair Routing - Board Bottom

5.2 RJ45 Connector

1. A shielded, metal enclosed RJ45 connector is recommended.
2. The metal shield should be connected directly to a proper chassis ground plane.
3. To maximize ESD performance, the designer should consider selecting an RJ45 module without LEDs. This will simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.
4. ESD performance can also be enhanced by using an RJ45 connector with surface mount contacts. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

5.3 Magnetics

1. There are many different types and configurations of magnetics available for use with any particular LAN device. A suitable 10/100/1000 magnetic should be selected for the LAN7500/LAN7500i. Different packages, orientations and sizes are all factors that need to be considered when selecting magnetics. For all SMSC LAN devices, it is suggested to use a qualified, recommended magnetic from our "Suggested Magnetics" application note. This application note is available from our website.
2. If the design engineer chooses to select an alternate magnetic for his application, steps should be taken to ensure a proper match is made with the SMSC LAN device. Referring to the "Suggested Magnetics" application note, the designer should use a tested and qualified magnetic from the list

as a reference. By obtaining the data sheet for that preferred magnetic and using it for comparison, the alternate magnetic can be evaluated. By comparing the specifications from the two data sheets, the design engineer can make an informed decision on how the alternate magnetic compares to the recommended magnetic and determine if it is suitable for use with a particular SMSC LAN device.

3. Generally speaking, the magnetics should be placed close to the RJ45 connector. In the case of the LAN7500/LAN7500i, SMSC recommends 0.50" at a minimum and 0.75" at a maximum.
4. The style of the selected magnetic (North/South or East/West) will determine the orientation of the magnetics in relation to the RJ45 connector. Ensure that the network side of the magnetics faces the RJ45 connector and the device side of the magnetics faces the LAN device. This will ensure that the high voltage barrier through the middle of the magnetics can be correctly routed and designed on the PCB.
5. Ideally, the SMSC LAN device should be placed close to the magnetics. If this is not possible, the RJ45 connector and magnetics must remain in close proximity. This will allow the LAN device to be placed in a location more remote from the RJ45/magnetics. In the case of the LAN7500/LAN7500i, SMSC recommends a distance between the LAN7500/LAN7500i and the magnetics of 1.0" at a minimum and 3.0" at a maximum.
6. To maximize ESD performance, the designer should consider selecting a discrete transformer as opposed to an integrated magnetic/RJ45 module. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

5.4 PCB Layer Strategy

1. In typical applications, power planes and digital ground planes are run from the LAN device to halfway through the magnetics module.
2. Typically, all planes are cleared out on the PCB in the area located halfway through the magnetics to the RJ45 connector. The TRxP/TRxN pairs should be the only traces in this cleared out region of the PCB. This creates one part of the high voltage barrier required for LAN applications.
3. Then, a chassis ground plane is designed up around the RJ45 connector. Once the plane shape is determined, this same shape should then be mirrored on all layers of the PCB.
4. Keep the chassis ground plane dimensions in a 6:1 ratio. Any sizing smaller than this will result in the plane behaving more like a trace instead of a plane.
5. Do not allow any other plane or trace to overlap the chassis ground plane. This will reduce the isolation/protection performance of the chassis ground plane.
6. Review basic Chassis Ground Plane Design Guidelines for PCBs before committing to a PCB assembly.

5.5 ETHRBIAS

The ETHRBIAS resistor sets an internal current source reference. Thus, the ETHRBIAS pin is a high impedance node and any noise induced on the ETHRBIAS traces will directly impact internal current references, negatively degrading the eye-diagram quality. The ETHRBIAS resistor should be placed close to the ETHRBIAS pin and the ground return should be short and direct to the ground plane. If possible, resistor traces should be very short and isolated from nearby traces.

6 EMI Considerations

6.1 PCB EMI Design Guidelines

Designing for EMC success must be considered during the schematic design and the PCB design cycles within the overall product design cycle. EMC design violations are especially critical to any Ethernet product simply due to the relationship between an Ethernet enabled device and EMC testing. Any circuit, anywhere inside the system enclosure, can generate EMC energy. The EMC energy will attempt to exit the system through any opening in the metal enclosure or at any cable making a system connection.

This leads to the following situation; first order evaluations identify the Ethernet portion of the design as the source for the radiated energy. More times than not, upon further investigation, it is found that the Ethernet portion of the design is designed and implemented correctly. Upon closer examination, it is found that offending designs have an “EMC generator” residing elsewhere in the design on the system PCB. The radiated energy is simply exiting the system at the Ethernet port. Upon correcting the source of the problem, the offending system usually passes testing with a much lower EMC signature.

When EMC problems are encountered, it is a common reaction to address the symptoms and not identify and correct the source of the EMC energy. Designers may try to include series resistors, series ferrite beads and additional common mode chokes on the Ethernet differential transmit pairs to reduce EMC levels. However, because this does not address the source of the problem, it is not the correct course of action. The EMC problem must be investigated and the “EMC generator” in the system must be identified and corrected. EMC issues are best corrected at the source.

6.2 Identify Critical Circuits

- Emissions – Clocks, buses and other repetitive circuits
- Immunity – Resets, interrupts and critical control lines

6.3 Choose Devices with EMI in Mind

- Slower is better – rise times and clocks
- Watch out for high-speed CMOS – both signal and power

6.4 Choose a Board Design

- Multilayer boards are 10 to 100 times better for both emissions and immunity
- Do not embed traces in power or ground planes

6.5 Perform the Initial Layout

- Separate high- and low-speed sections
- Keep critical circuits away from I/O circuits
- Hand route critical lines

6.6 Pay Attention to Power Decoupling

- Decouple every device with a high-frequency capacitor

- Bypass every power input to the board with a high-frequency capacitor
- Keep capacitor leads short
- To improve noise and EMI in very high speed designs, a mix of 0.1uF, 0.01uF and lower value capacitors may be used

6.7 Pay Attention to Connectors

- Keep critical circuits away from connectors
- Use adequate ground returns (5:1 minimum for high-frequency circuits)
- Watch out for internal-cable sneak paths

6.8 Special Concerns for Clocks

- Keep the hot leads short and matched if a crystal is used
- Add small damping resistors or ferrites to the clock oscillator
- Control clock routing
- Watch out for noisy oscillator modules
- Whenever possible, oscillators should be avoided. Oscillators increase EMI, power consumption, and jitter
- Use a crystal if possible

6.9 Special Concerns for Resets, Interrupts & Control Lines

- Add high-frequency filtering at circuit inputs
- Control trace routing
- Do not cross any plane splits with high-speed signal traces

6.10 Special Concerns for I/O Circuits

- Three EMI paths through I/O – signal, power & ground
- Add high-frequency filtering to all I/O lines – even slow I/O
- Isolated I/O planes can help, but must be implemented correctly

6.11 Test Early and Often

- Don't wait until the end of the design cycle to perform EMI testing
- Develop and implement your own engineering-level EMI testing
- Objective is to improve probability for success in compliance tests

7 ESD Considerations

7.1 Ethernet Specific Considerations

1. The RJ45 connector must have a metal shield to ensure the highest ESD performance.
2. The metal shield of the RJ45 connector must be connected directly into the system's chassis ground plane at two points.
3. For increased ESD protection, the design engineer should consider using an RJ45 connector that does not have integrated LEDs. Selecting an RJ45 connector without LEDs will simplify the design of the high-voltage barrier and simplify any troubleshooting of the ESD hardness of the product.
4. Consider using discrete magnetics versus integrated magnetics. Since the basic concept of good ESD performance is separation, the discrete magnetic choice may be the wiser selection. The belief is that it is simply easier to get the proper spacing for all the components in the Ethernet front end with discrete magnetics. Using discrete magnetics will also greatly simplify any troubleshooting of the ESD hardness of the product.
5. All power planes and non-Ethernet traces must be cleared out from halfway under the magnetics to the RJ45 connector. Separation should be maintained for at least 0.250".
6. The choice and placement of the magnetics is very important for high ESD performance. Depending on space and location on the PCB, magnetic modules must be selected and placed according to their construction. North/South magnetics are pinned differently than East/West magnetics and must be placed accordingly on the PCB. The size of the magnetic module may prove to be important. All these factors have an affect on the design and outcome of the high-voltage barrier required by the Ethernet interface.
7. The PCB on which the Ethernet circuitry resides should rest on metal stand-offs that are at least 0.250" high (or higher if solder nibs are not trimmed) from the metal case of the product.
8. The choice and placement of the specific RJ45 connector may also have a very high impact on the ESD performance of the product. RJ45 connectors with the chassis ground tabs as far away from the 8-pin connections may prove to be the best configuration for ESD. Placement of the RJ45 connector with respect to other connectors and the overall PCB location may prove very important in overall ESD performance.
9. Be certain to check that all circuitry related to and residing in the high-voltage barrier region is referenced to chassis ground only. LEDs, capacitors, transorbs and anti-parallel diodes referenced to digital ground in the high-voltage barrier area will compromise the high-voltage barrier.

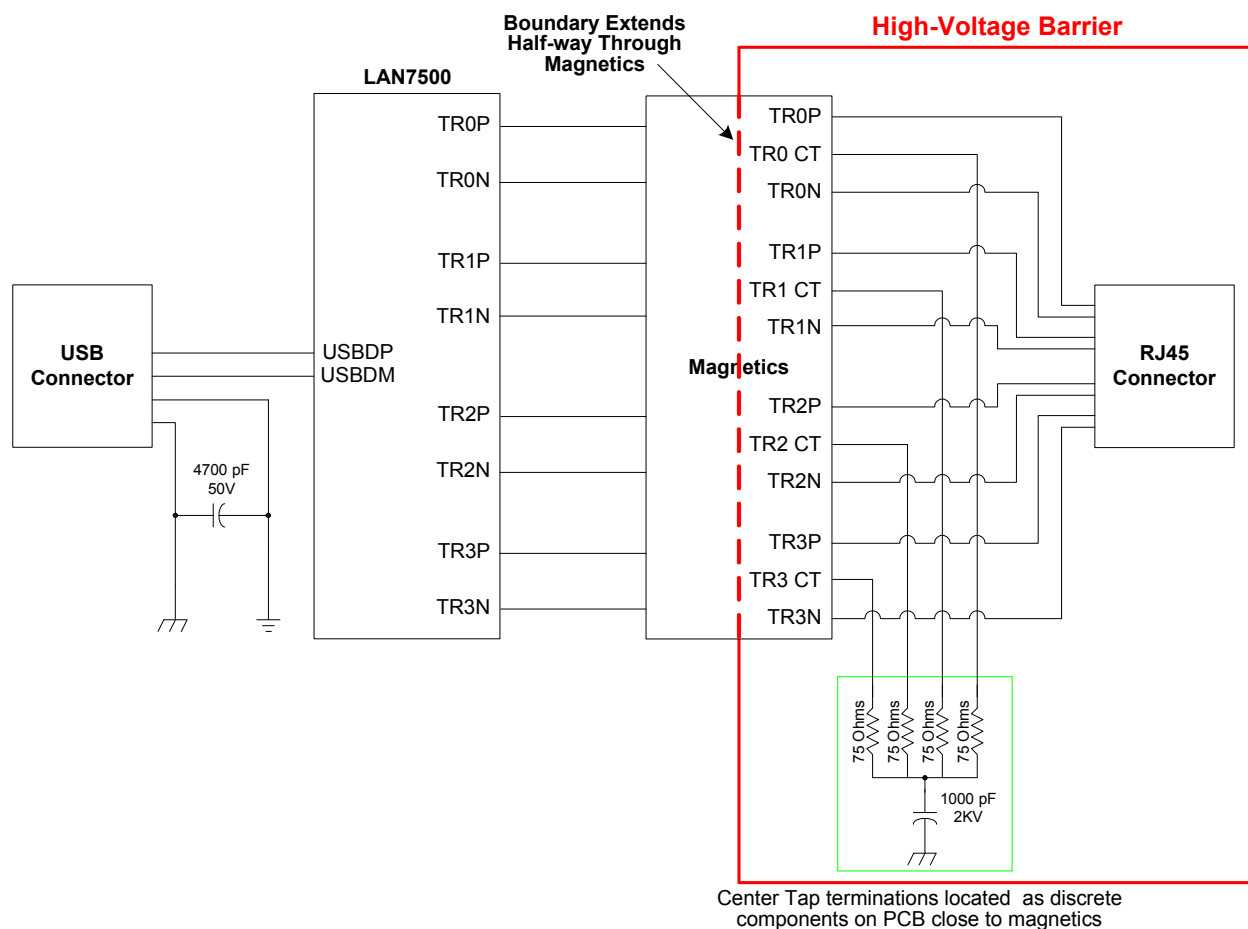


Figure 7.1 Ethernet and USB Front End Schematic

7.2 Power Supply Considerations

1. Power supply voltage wires should be twisted tightly together with their return wires.
2. All power entries to the PCB must be bypassed properly as close as possible to the power connector on the PCB.

7.3 PCB Layer Strategy

1. SMSC strongly recommends using at least a four layer PCB for all high-speed Ethernet LAN designs. Multi-layer PCBs are very important in order to control ESD problems.
2. The implementation of an Ethernet chassis ground plane that is completely separate from the digital ground plane is required.
3. The chassis ground plane should be mirrored on every layer of the PCB. Each chassis ground plane on each layer should then be stitched together with multiple vias.

4. Use a large plated hole to connect the chassis ground planes to the metal enclosure (Earth ground). This mounting hole should have large, conductive pads on both the component side and solder side of the PCB. These two large, conductive pads should also be stitched together with multiple, plated-through vias. The pads should also be free from solder to ensure a good, flat surface to mate with the metal standoff.
5. All chassis ground plane connections must have low impedance connections. Short traces and multiple via connections will attain this.
6. The Earth ground connection mounting hole should be located within 1.0" of the RJ45 connector.
7. Locate the Earth ground connection(s) away from sensitive circuitry. This strategy will force the flow of an ESD occurrence away from the sensitive circuitry and direct it to Earth ground.
8. All other connectors in the system should also incorporate a chassis ground beneath them. Any connector going to the outside world is a candidate for a chassis ground plane.
9. Any other PCB mounting hole can be designed with optional digital ground plane connections through a wide SMD footprint. In this case, each of the other mounting holes in the design can be configured as a soft ground (500 – 1K ohm jumper), hard ground (zero ohm jumper), separate from ground (no connection) or an AC-coupled connection to ground (high voltage capacitor). This will give the designer the flexibility required to shape the ESD profile of his product to the exact test needs.

7.4 Signal Integrity Concerns

1. All signal traces throughout the design should be kept to a minimum. Consider adding a digital ground "guard trace" to signal traces over 12" long.
2. Place I/O circuits close to their respective connectors. This will minimize trace length and susceptibility.
3. ESD occurrences can cause digital ground plane "ground bounce" if allowed to enter the digital ground plane. This can cause erratic system behavior and/or system failure. Every effort should be taken to make sure that any ESD source is not allowed to enter any digital ground or power plane on the PCB.

7.5 Component Guidelines

1. Verify that all components in the design meet application requirements. For instance, if the application requires operation to a specific high-ESD level, be certain that all other devices in the design (besides the LAN device) meet this requirement. This should include bypass caps (usually 2KV for Ethernet applications), magnetics, etc.
2. Review all component placing guidelines for proper clearance (0.250") from outside metal cases, board edges and chassis ground plane contacts.

7.6 PCB Trace Considerations

1. All component leads to any power plane or ground plane should be as short as possible. Though costly, the best solution is to include plane connection vias inside the surface mount pads. However, when using vias outside the surface mount pads, pad-to-via-edge connections should be less than 5–10 mils in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc..
2. Review all signal traces for proper clearance (0.250") from outside metal cases, board edges and chassis ground plane contacts.

7.7 Miscellaneous

1. Review all PCB connector interfaces for proper shielding and grounding to ensure good ESD performance. One improperly designed connector circuit may allow ESD energy to enter the system and cause system failure.
2. The design engineer must design in ESD safeguards at the onset of the design. In order to ensure compliance at the time of production release, the design should undergo ESD testing at the earliest possible stage of the design. Waiting until the end of the design cycle to determine the system's ESD hardness can prove to be a major mistake.
3. When designing a PCB that will be housed in an enclosure, connectors external to the enclosure need to be tested with an ESD gun.
4. Review the SMSC Design Guide for Power Over Ethernet Applications (AN17.18) if using the device in a POE application (www.smisc.com).



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