SY898530U

500 MHz, 1:16, 3.3V-to-2.5V/3.3V LVPECL Fanout Buffer

Features

- 16 Differential 2.5V/3.3V LVPECL Outputs
- Differential CLK Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL Logic Levels
- Translates Any Single-Ended Input Signal to 2.5V/3.3V LVPECL Levels with a Resistor Bias on /CLK Input
- 500 MHz Maximum Output Frequency
- <50 ps Output Skew
- <250 ps Part-to-Part Skew
- <2 ns Propagation Delay
- 3.3V Core, 2.5V/3.3V Output Operating Supply
- 0°C to +70°C Operating Temperature
- Available in a 48-Lead TQFP Package
- Pin-to-Pin Compatible with ICS8530

Applications

- Data Distribution
- High-Performance PCs
- Communications
- Parallel Processor-Based Systems

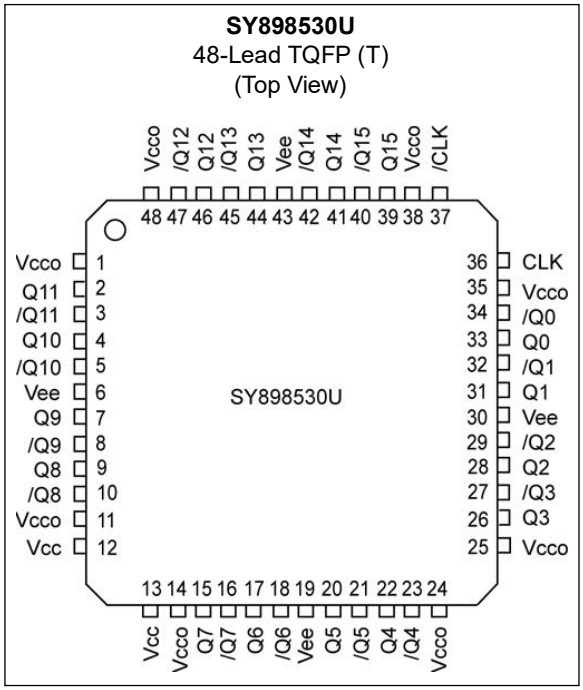
General Description

The SY898530U is a 1:16 fanout buffer that can accept most standard differential logic levels and outputs the signal as a differential 2.5V or 3.3V LVPECL signal. The part can amplify input signals as small as 150 mV_{PP} to the full LVPECL output swing. The SY898530U is well suited for clock distribution applications which demand versatility and low-skew performance. It is pin-to-pin compatible with IDT's ICS8530 fanout buffer.

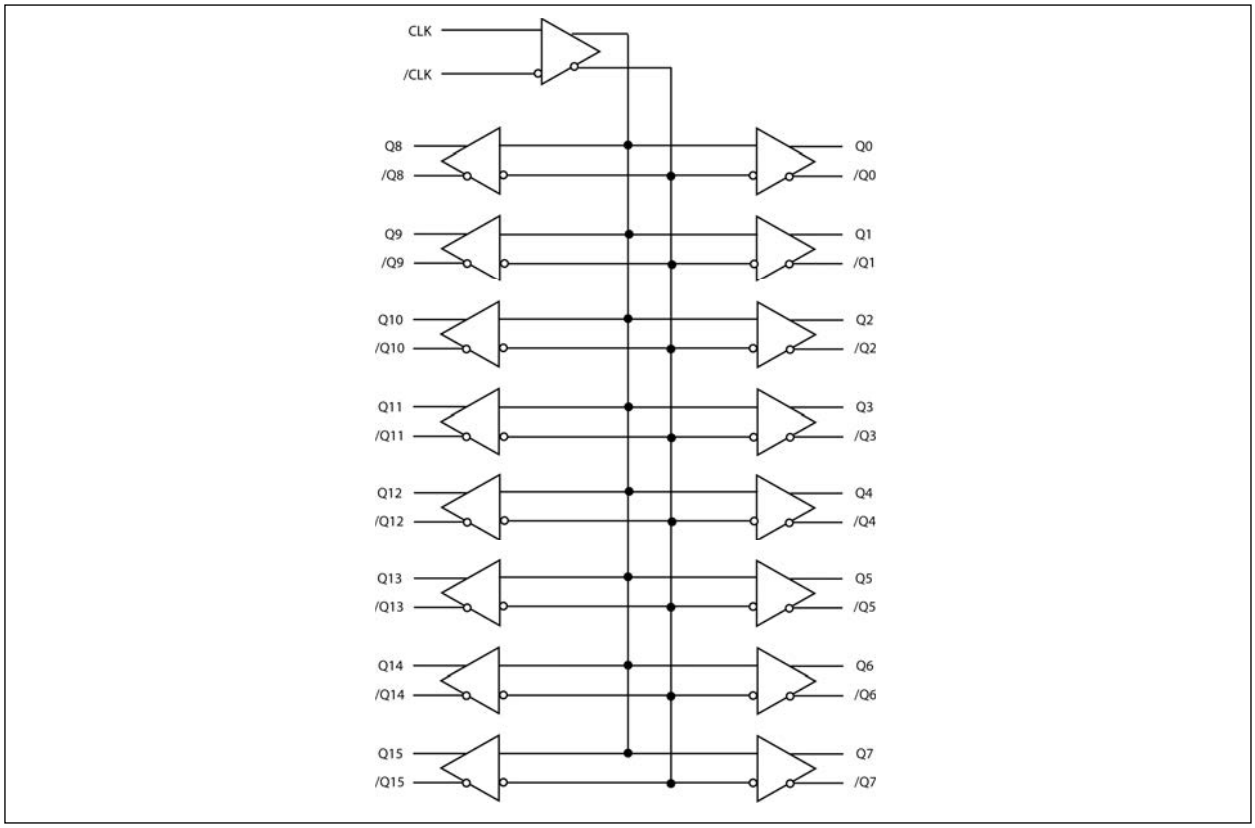
The SY898530U operates from a 3.3V ±5% core power supply and a 2.5V ±5% or a 3.3V ±5% output supply. The SY898530U is ensured over the full commercial temperature range (0°C to +70°C). It is available in a 48-lead TQFP lead-free package.

Package Type

SY898530U
48-Lead TQFP (T)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.5V
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +3.135V to +3.465V
Output Supply Voltage (V_{CCO}) ..... +2.375V to +3.465V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	V_{CC}	3.135	3.3	3.465	V	—
Output Power Supply	V_{CCO}	2.375	—	3.465	V	—
Power Supply Current	I_{EE}	—	—	125	mA	Maximum V_{CC}, V_{CCO}
CLK Input High Current	I_{IH}	—	—	150	µA	V_{CC} = V_{IN} = 3.465V
/CLK Input High Current		—	—	5		
CLK Input Low Current	I_{IL}	–5	—	—	µA	V_{CC} = 3.465V, V_{IN} = 0.5V
/CLK Input Low Current		–150	—	—		
Peak-to-Peak Input Swing	V_{PP}	0.15	—	1.3	V	—
Common Mode Input Voltage	V_{CMR}	0.5	—	V_{CC} – 0.85	V	Note 2, Note 3

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

2: For single-ended applications, the maximum input voltage for CLK, /CLK is V_{CC} + 0.3V.

3: Common mode voltage is defined as V_{IH}.

PECL OUTPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, Outputs terminated with 50Ω to V_{CCO} – 2V unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{CCO} – 1.1	—	V_{CCO} – 0.7	V	—
Output Low Voltage	V_{OL}	V_{CCO} – 2.0	—	V_{CCO} – 1.4	V	—
Output Voltage Swing	V_{OUT}	0.55	—	0.93	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	500	—	—	MHz	—
Propagation Delay	t_{PD}	1	—	2	ns	Note 1
Output-to-Output Skew	t_{SKEW}	—	26	50	ps	Note 2, Note 4
Part-to-Part Skew		—	—	250	ps	Note 3, Note 4
RMS Phase Jitter	t_{JITTER}	—	127	—	fs_{RMS}	Output = 500 MHz, Integration Range: 12 kHz to 20 MHz
Output Rise/Fall Time	t_r, t_f	300	—	700	ps	At full output swing
Duty Cycle	DC	47	50	53	%	—

Note 1: Measured from the differential input crossing point to the differential output crossing point.

2: Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.

3: Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: This parameter is defined in accordance with JEDEC Standard 65.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	0	—	+70	°C	—
Package Thermal Resistances						
Thermal Resistance, TQFP 48-Ld (Note 1)	θ_{JA}	—	48	—	°C/W	Still-Air
	θ_{JC}	—	13	—	°C/W	Junction-to-Case

Note 1: θ_{JA} and θ_{JC} values are determined for a 4-layer board in still-air.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, V_{CCO} = 2.5V or 3.3V, T_A = +25°C, Input Signal = 800 mV.

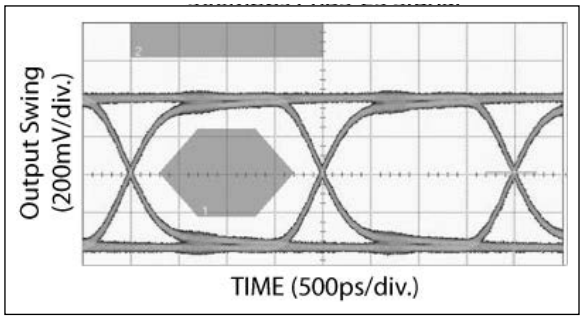


FIGURE 2-1: *500 Mbps PRBS-23 Signal.*

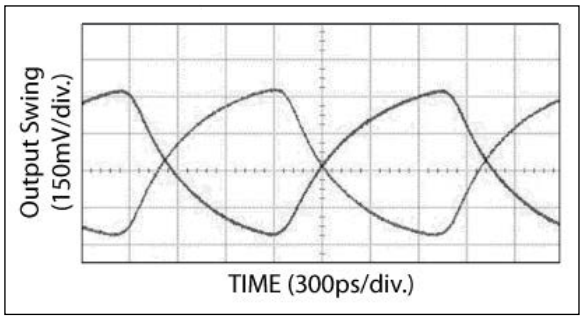


FIGURE 2-2: *500 MHz Clock Signal.*

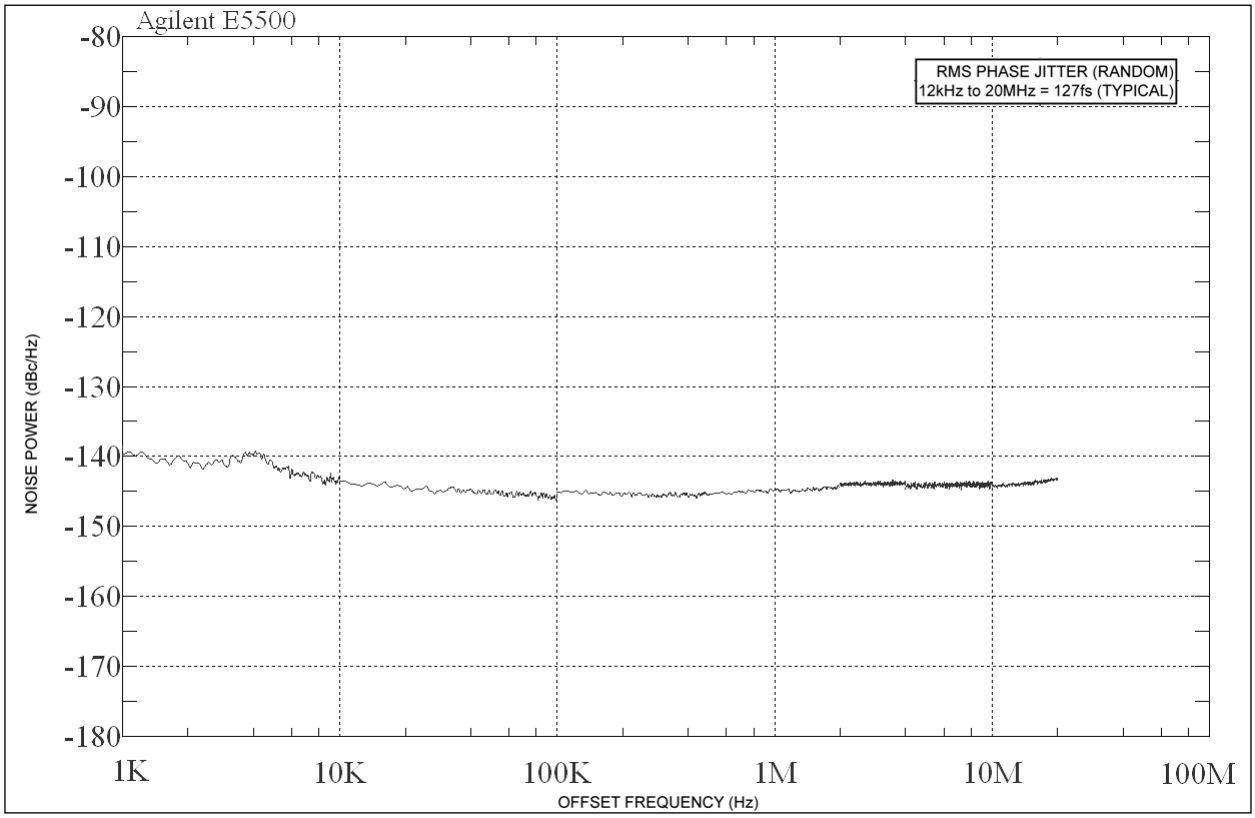


FIGURE 2-3: *Phase Noise Graph.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
36, 37	CLK, /CLK	Differential Clock Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL logic levels. CLK is internally connected to a pull-down resistor, /CLK is internally connected to a pull-up resistor. See Table 3-2 for typical values.
33, 34 31, 32 28, 29 26, 27 22, 23 20, 21 17, 18 15, 16 9, 10 7, 8 4, 5 2, 3 46, 47 44, 45 41, 42 39, 40	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11 Q12, /Q12 Q13, /Q13 Q14, /Q14 Q15, /Q15	LVPECL Differential Output Pairs. Differential buffered copies of the input signal. The output swing is typically 740 mV. See the Interface Applications section for termination information.
1, 11, 14, 24, 25, 35, 38, 48	VCCO	Output Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers.
12, 13	VCC	Core Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors as close to the VCC pins as possible. Supplies input and core circuitry.
6, 19, 30, 43	VEE	Ground.

TABLE 3-2: PIN CHARACTERISTICS

Symbol	Description	Typical Value
C_{IN}	Input Capacitance	4 pF
R_{PULLUP}	Input Pull-Up Resistor	50 kΩ
$R_{PULLDOWN}$	Input Pull-Down Resistor	30 kΩ

TABLE 3-3: CLOCK INPUT FUNCTION

Inputs		Outputs		Input to Output Mode	Polarity
CLK	/CLK	Qx	/Qx		
0	1	Low	High	Differential to Differential	Non-Inverting
1	0	High	Low	Differential to Differential	Non-Inverting
0	Biased(1)	Low	High	Single-Ended to Differential	Non-Inverting
1	Biased(1)	High	Low	Single-Ended to Differential	Non-Inverting
Biased(1)	0	High	Low	Single-Ended to Differential	Inverting
Biased(1)	1	Low	High	Single-Ended to Differential	Inverting

Note 1: Refer to the Interface Applications section for Single-Ended interfaces.

4.0 TEST CIRCUITS

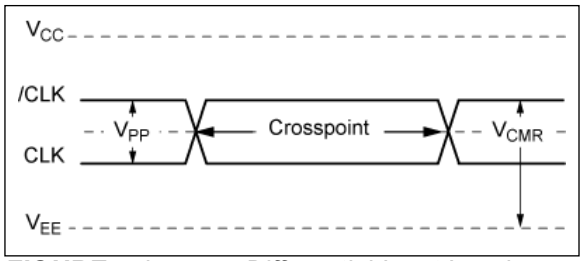


FIGURE 4-1: *Differential Input Level.*

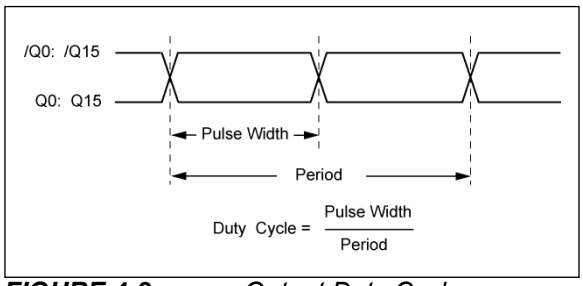


FIGURE 4-2: *Output Duty Cycle.*

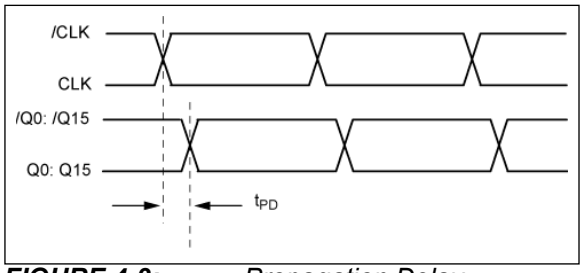


FIGURE 4-3: *Propagation Delay.*

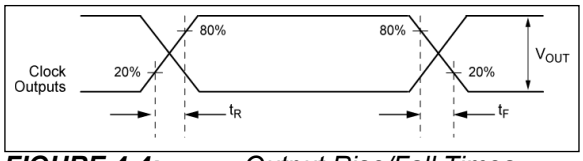


FIGURE 4-4: *Output Rise/Fall Times.*

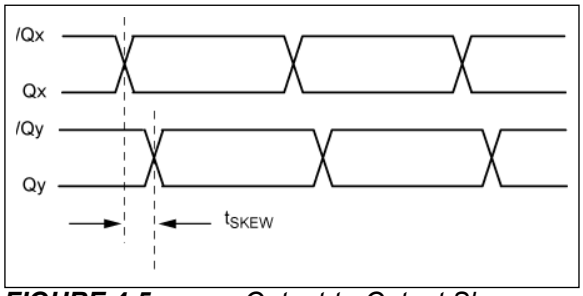


FIGURE 4-5: *Output-to-Output Skew.*

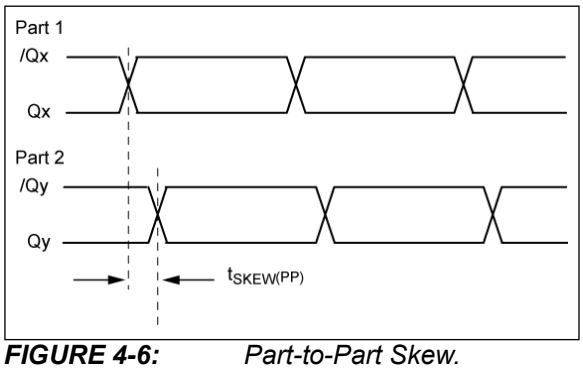


FIGURE 4-6: *Part-to-Part Skew.*

5.0 JUNCTION TEMPERATURE

The maximum recommended junction temperature is T_J = +125°C. The outputs are terminated with 50Ω to V_{CCO} – 2V. Below is a calculation of the worst case scenario with zero airflow:

5.1 Terms

- T_J = Junction temperature.
- T_A = Ambient temperature.
- θ_{JA} = Junction-to-Ambient thermal resistance.
- P_D = Power dissipation.

5.2 Calculations

$PD = P_{D\_CORE} + P_{D\_OUTPUTS}$

$P_{D\_CORE} = V_{CC(MAX)} \times I_{EE(MAX)}$

P_{D_CORE} = 3.465V x 125 mA = 433 mW

$P_{D\_OUTPUT} = P_{D\_H} + P_{D\_L}$

$P_{D\_H} = [(V_{OH} – (V_{CCO} – 2V))/R_L] \times (V_{CCO} – V_{OH(MAX)})$

P_{D_H} = [(2V – 0.7V)/50Ω] x 0.7V

P_{D_H} = 18.2 mW

$P_{D\_L} = [(V_{OL} – (V_{CCO} – 2V))/R_L] \times (V_{CCO} – V_{OL(MAX)})$

P_{D_L} = [(2V – 1.4V)/50Ω] x 1.4V

P_{D_L} = 16.8 mW

P_{D_OUTPUT} = 35 mW

$P_{D\_OUTPUTS}$ = 16 x 35 mW

$P_{D\_OUTPUTS}$ = 560 mW

P_D = 433 mW + 560 mW

P_D = 0.993 W

$T_J = T_A + \theta_{JA} \times P_D$

$T_{J\_WORST\_CASE}$ = 70°C + 0.993W x 48°C/W

$T_{J\_WORST\_CASE}$ = 118°C in still air.

The worst case junction temperature is below 125°C.

6.0 INPUT INTERFACE APPLICATIONS

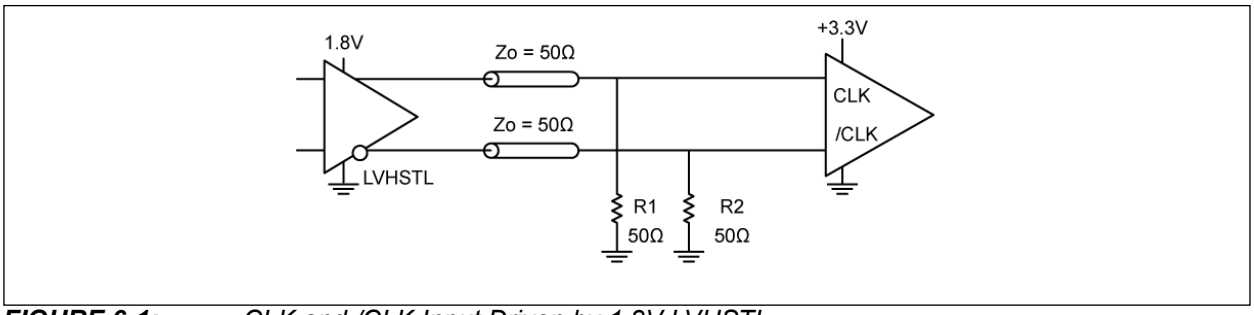


FIGURE 6-1: *CLK and /CLK Input Driven by 1.8V LVHSTL.*

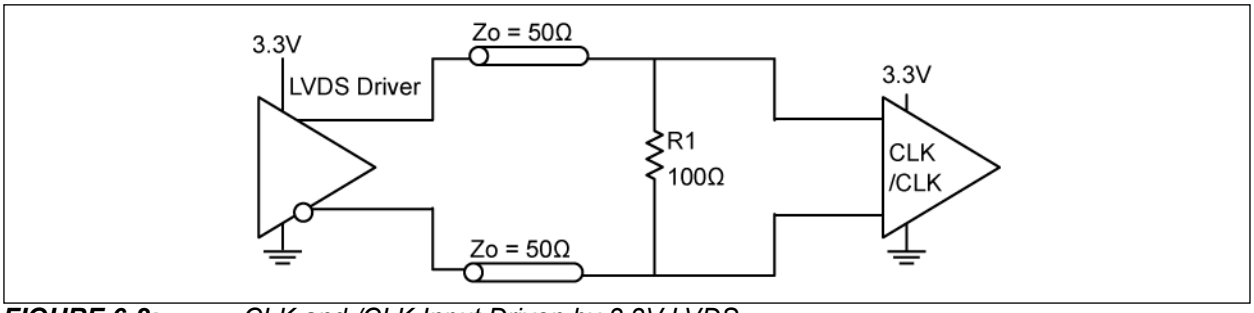


FIGURE 6-2: *CLK and /CLK Input Driven by 3.3V LVDS.*

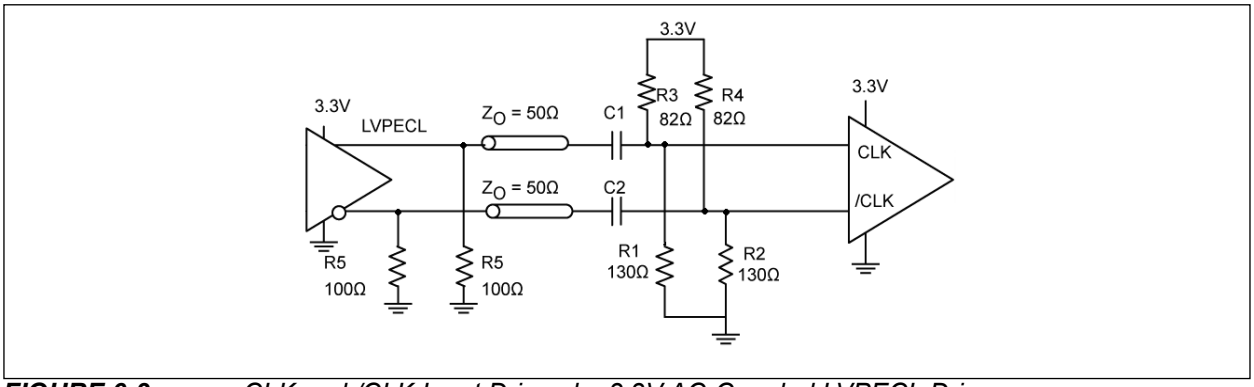
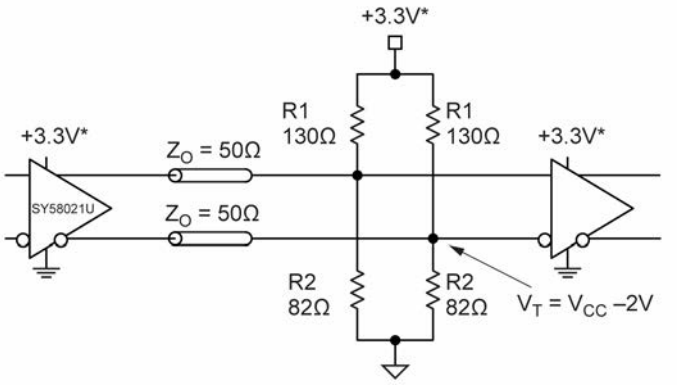


FIGURE 6-3: *CLK and /CLK Input Driven by 3.3V AC-Coupled LVPECL Driver.*

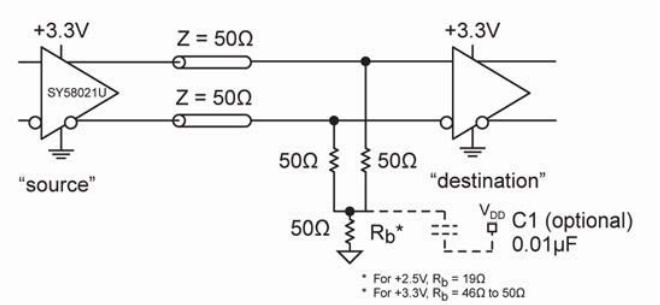
Note: For +2.5V systems: R5 = 50Ω, R1 & R2 = 220Ω, R3 & R4 = 68Ω.

7.0 OUTPUT INTERFACE APPLICATIONS



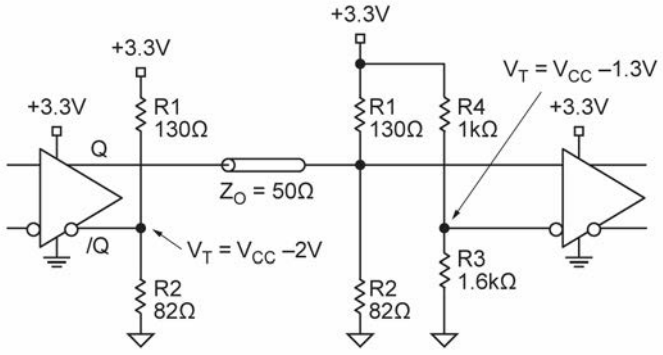
Note:
1. For +2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

FIGURE 7-1: *Parallel Termination: Thevenin Equivalent.*



Notes:
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. For +2.5V systems, R_b = 19Ω. R_b resistor sets the DC bias voltage, equal to V_T.

FIGURE 7-2: *Parallel Termination: Three-Resistor.*



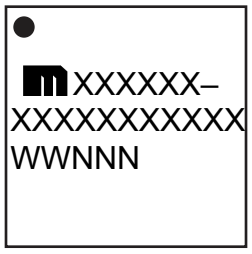
Notes:
1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250, R2 = 62.5, R3 = 1.25k, R4 = 1.2k

FIGURE 7-3: *Terminating Unused I/O.*

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

48-Lead TQFP*



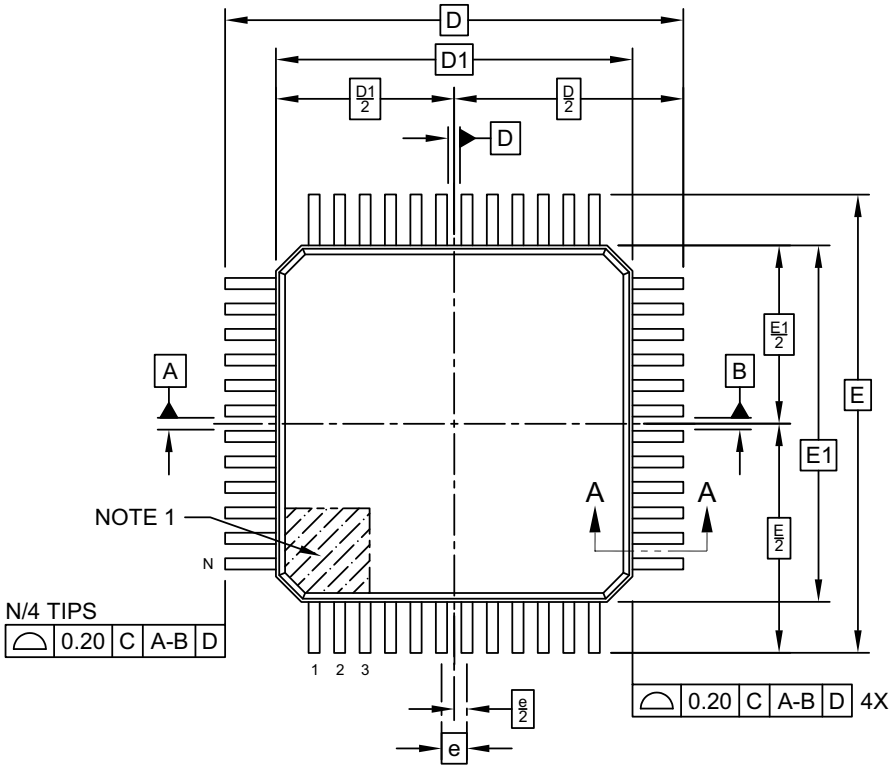
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

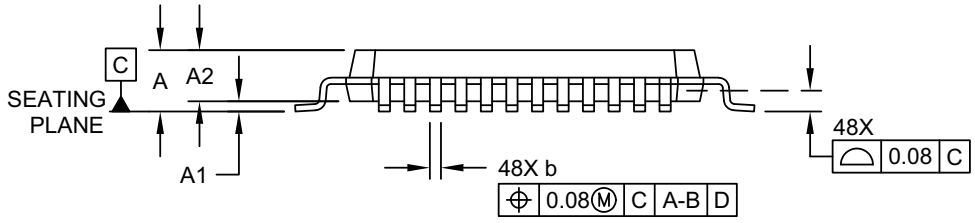
Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

48-Lead Plastic Thin Quad Flatpack (CQA) - 7x7x1.0 mm Body [TQFP]
Micrel Legacy Package TQFP7x7-48L

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

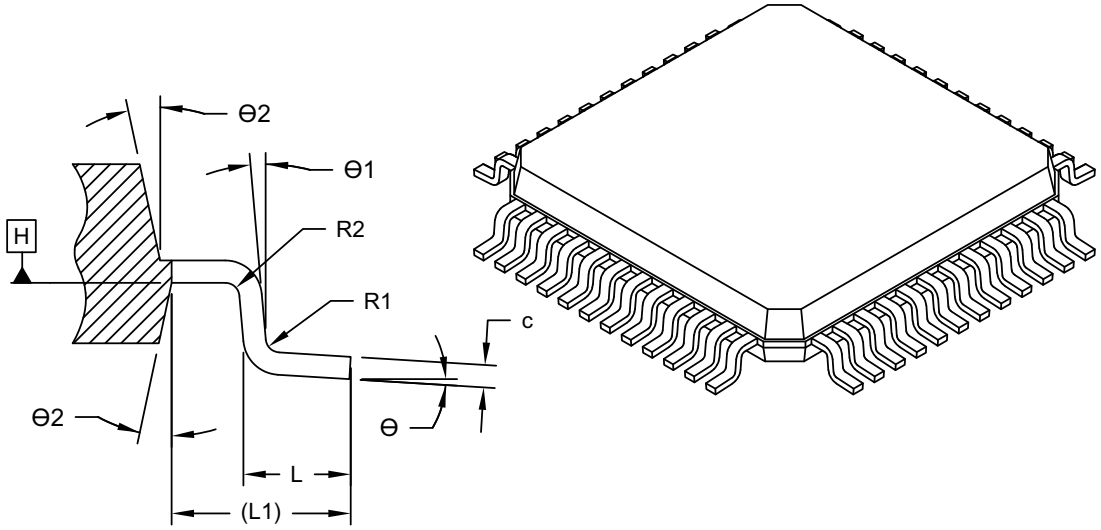


SIDE VIEW

Microchip Technology Drawing C04-1175 Rev A Sheet 1 of 2

48-Lead Plastic Thin Quad Flatpack (CQA) - 7x7x1.0 mm Body [TQFP]
Micrel Legacy Package TQFP7x7-48L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.12	-	0.21
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Terminal-to-Exposed-Pad	Θ2	11°	12°	13°

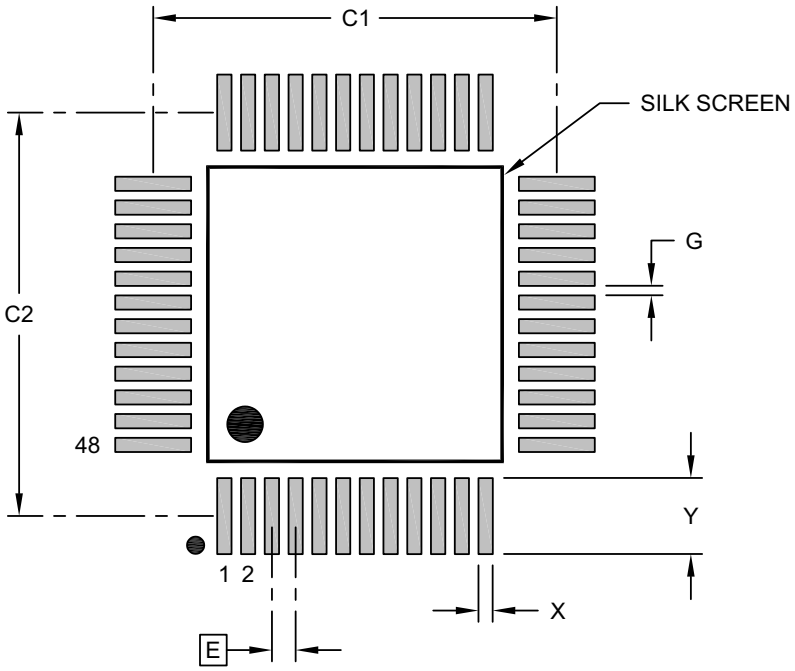
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1175 Rev A Sheet 2 of 2

48-Lead Plastic Thin Quad Flat Pack (CQA) - 7x7x1.0 mm Body [TQFP]
Micrel Legacy Package Code TQFP7x7-48LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.60
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3175 Rev A

APPENDIX A: REVISION HISTORY

Revision A (September 2023)

- Converted Micrel document SY898530U to Microchip data sheet template DS20006818A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY898530:	500 MHz, 1:16, 3.3V-to-2.5V/3.3V LVPECL Fanout Buffer	
Supply Voltage:	U	=	2.5V/3.3V
Package:	T	=	48-Lead TQFP
Temperature Range:	Z	=	0°C to +70°C
Media Type:	<blank> TR	= =	250/Tray 1,000/Reel

Examples:

a) SY898530UTZ:

SY898530, 2.5V/3.3V Supply Voltage, 48-Lead TQFP, 0°C to +70°C Temperature Range, 250/Tray

b) SY898530UTZ-TR:

SY898530, 2.5V/3.3V Supply Voltage, 48-Lead TQFP, 0°C to +70°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

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- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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