MIC2782

Dual-Input Push Button Reset IC with Immediate and Delayed Outputs

Features

- 1.5V to 5.5V Operating Supply Voltage
- 2.2 µA Supply Current with /MR1, /MR2 Not Asserted
- Factory-Programmed Setup Periods of 6s, 8s, 10s, or 12s
- Factory-Programmed Reset Timeout Periods of 0.5s, 1s, or 2s
- Integrated 65 kΩ /MR1 and /MR2 Pull-Up Resistors
- Supports Single Push-Button Reset with /MR1 Tied to /MR2
- RESET Asserts after /MR1 and /MR2 are Asserted Low for a Setup Period
- ANDOUT Asserts after /MR1 and /MR2 are Asserted Low for a Debounce Time (1.5 ms)
- Open-Drain RESET and ANDOUT Outputs
- 6-Bump, 0.4 mm Pitch, 0.8 mm x 1.2 mm Wafer Level Chip Scale Package (WLCSP)

Applications

- Smartphones
- Tablets
- eBooks
- Portable Games
- Portable Navigation Devices

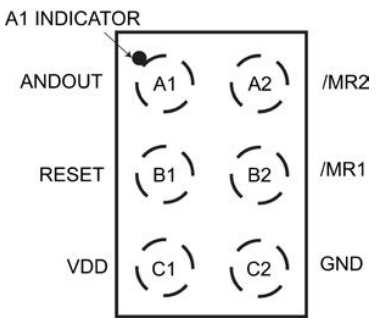
General Description

The MIC2782 is a two input, two output push-button reset IC. It will generate a reset pulse for a factory-programmed reset timeout period after both manual reset inputs have been held to a logic-low for the factory-programmed setup period. The MIC2782 also has an ANDOUT logic output that will activate if both inputs are held low for longer than a debounce time (1.5 ms) and deactivate if one or both inputs are released for longer than a debounce time (1.5 ms). The RESET and ANDOUT outputs are active-low, open-drain NMOS outputs.

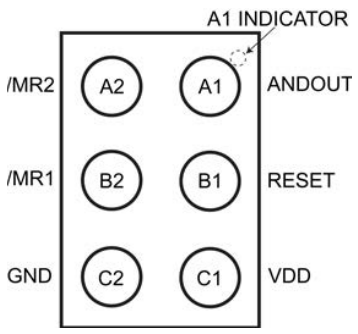
The MIC2782 operates over the 1.5V to 5.5V supply voltage range, consuming 2.2 µA of supply current at 3.3V. The device features 65 kΩ internal pull-up resistors on both of the inputs (/MR1 and /MR2). The device offers factory programmed setup periods of 6s, 8s, 10s, or 12s and reset timeout periods of 0.5s, 1s, or 2s. It is available in a space saving, 6-bump, 0.4 mm pitch, 0.8 mm x 1.2 mm wafer level chip scale package.

Package Type

Top View (Bump Side Down)



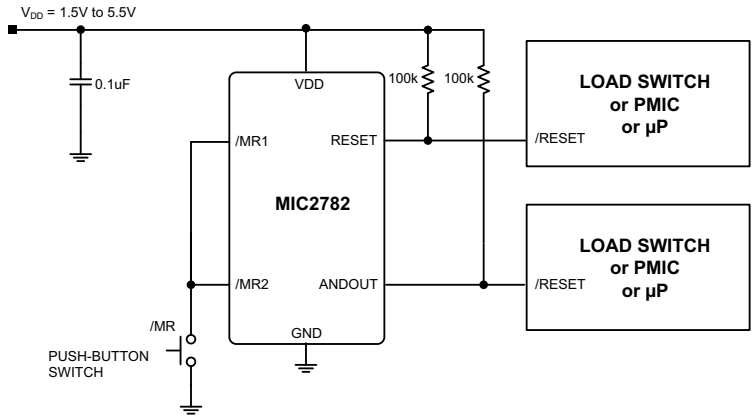
Bottom View (Bump Side Up)



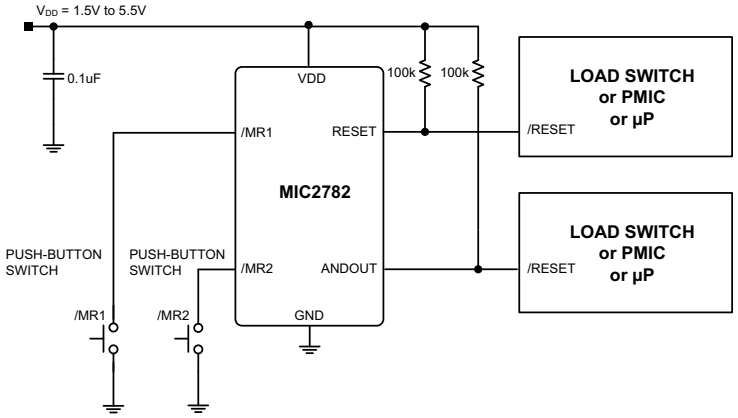
6-Bump, 0.4 mm Pitch, 0.8 mm x 1.2 mm WLCSP

Typical Application Circuits

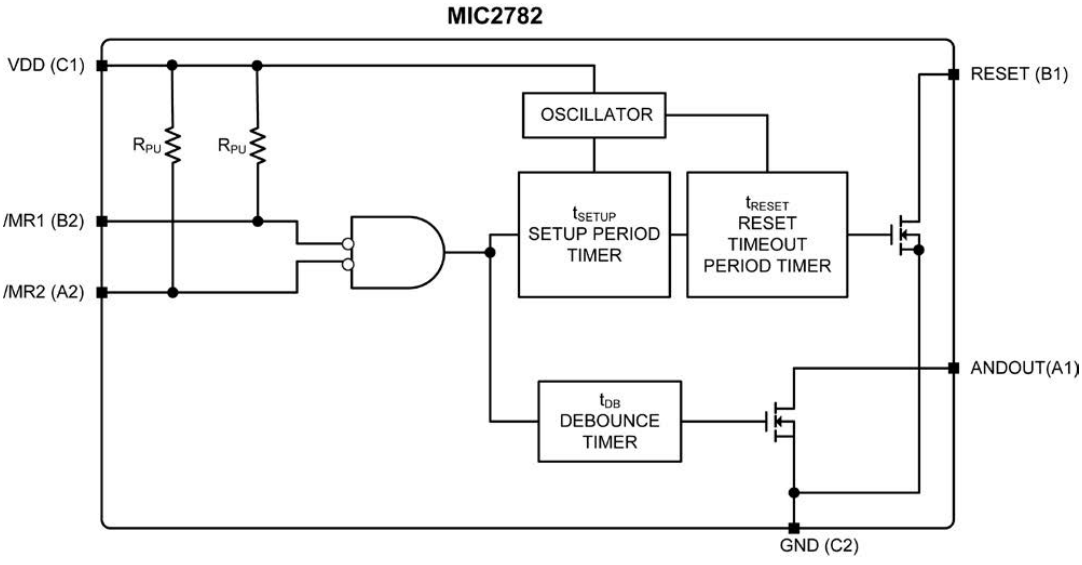
Single Button Application for MIC2782 Used for Microcontroller Reset



Dual Button Application for MIC2782 Used for Microcontroller Reset



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... GND to +6.0V
Input Voltage ($V_{/MR1}$, $V_{/MR2}$) ..... GND – 0.3V to V_{DD} + 0.3V
NMOS Output Voltage (V_{RESET}, V_{ANDOUT}) ..... GND – 0.3V to +6.0V
ESD Rating (Human Body Model, Note 1) ..... 2 kV
ESD Rating (Machine Model) 200V

Operating Ratings ‡

Supply Voltage (V_{DD}) ..... +1.5V to +5.5V
Input Voltage ($V_{/MR1}$, $V_{/MR2}$) ..... 0V to V_{DD}
NMOS Output Voltage (V_{RESET}, V_{ANDOUT}) ..... 0V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Device is ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

For typical values, V_{DD} = 3.3V, /MR1 = /MR2 = Open, T_J = +25°C, **bold** values valid for –40°C ≤ T_J ≤ +85°C; unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Supply Voltage	V_{DD}	**1.5**	—	**5.5**	V	Reset output valid
Supply Current	I_{DD}	—	2.2	**4.0**	µA	V_{DD} = 3.3V, /MR1 = /MR2 = V_{DD}
		—	3.2	**5.0**		V_{DD} = 5.0V, /MR1 = /MR2 = V_{DD}
		—	120	—		V_{DD} = 3.3V, /MR1 = /MR2 = GND
Reset Time						
Setup Period	t_{SETUP}	**5.4**	6	**6.6**	sec.	Ordering option: C
		7.2	8	**8.8**		Ordering option: D
		9.0	10	**11**		Ordering option: E
		10.8	12	**13.2**		Ordering option: F
Reset Timeout Period	t_{RESET}	**0.4**	0.5	**0.6**	sec.	Ordering option: L
		0.9	1	**1.1**		Ordering option: M
		1.8	2	**2.2**		Ordering option: R
ANDOUT Debounce Time	t_{DB}	**1**	1.5	**2**	ms	$V_{/MR1,2}$ < (V_{IL} – 100 mV)
Output Low Voltage	V_{OL}	—	—	**0.3**	V	V_{DD} = 4.5V, I_{SINK} = 1.6 mA
		—	—	**0.3**		V_{DD} = 3.3V, I_{SINK} = 1.2 mA
		—	—	**0.3**		V_{DD} = 1.5V, I_{SINK} = 0.5 mA
Open-Drain Leakage Current	$I_{LEAKAGE}$	—	—	**300**	nA	RESET, ANDOUT Inactive V_{RESET}, V_{ANDOUT} = 5.5V
/MR1, /MR2 Input						
Input High Voltage	V_{IH}	**1.2**	—	—	V	—
Input Low Voltage	V_{IL}	—	—	**0.4**	V	—
Internal Pull-Up Resistance	R_{PU}	**55**	65	**75**	kΩ	For /MR1, /MR2

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+85	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, 6-Bump WLCSP	θ_{JA}	—	125	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

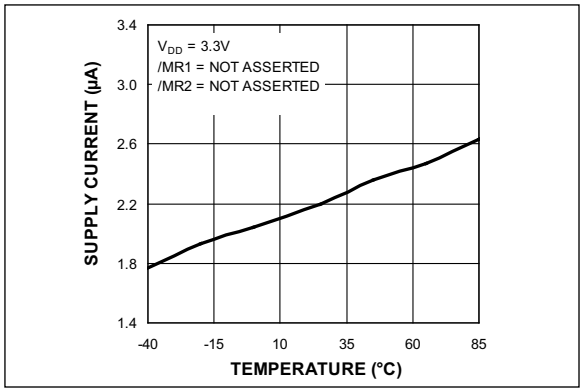


FIGURE 2-1: *V_{DD} Supply Current vs. Temperature.*

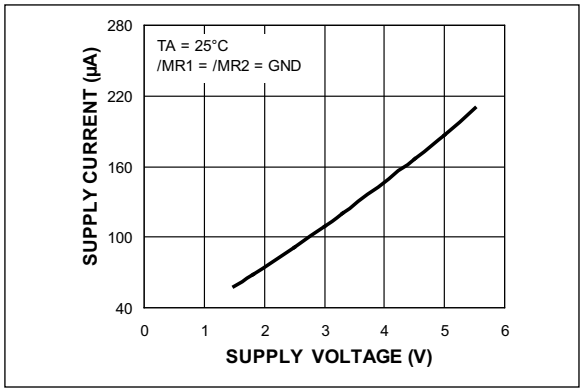


FIGURE 2-4: *Supply Current for /MR1 and /MR2 Inputs Low vs. Supply Voltage.*

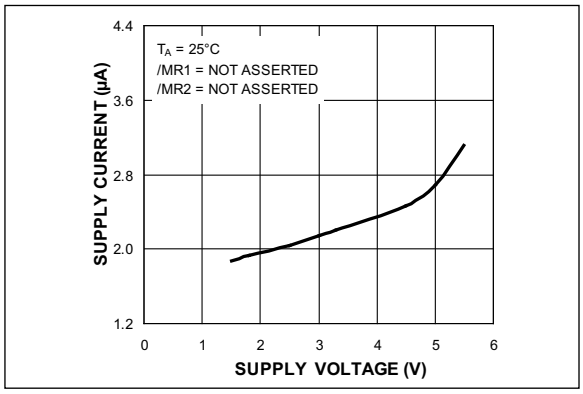


FIGURE 2-2: *V_{DD} Supply Current vs. Supply Voltage.*

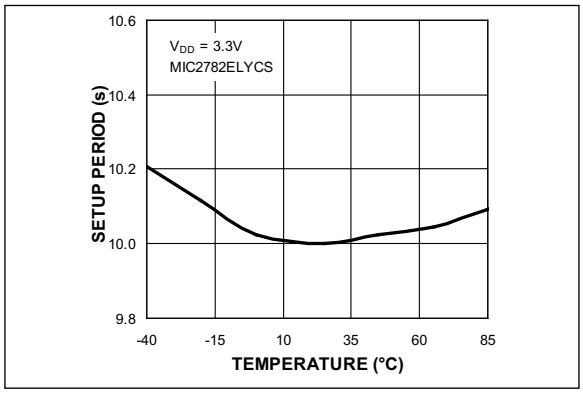


FIGURE 2-5: *Setup Period vs. Temperature.*

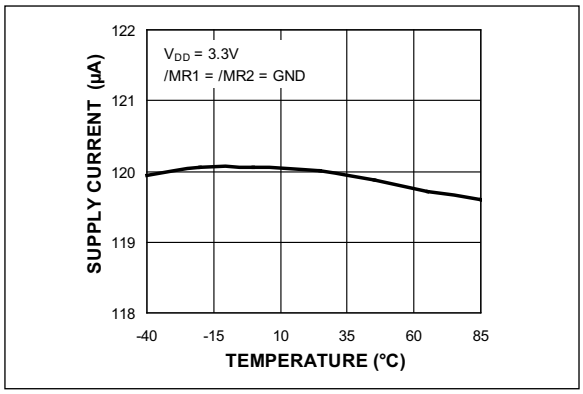


FIGURE 2-3: *Supply Current for /MR1 and /MR2 Inputs Low vs. Temperature.*

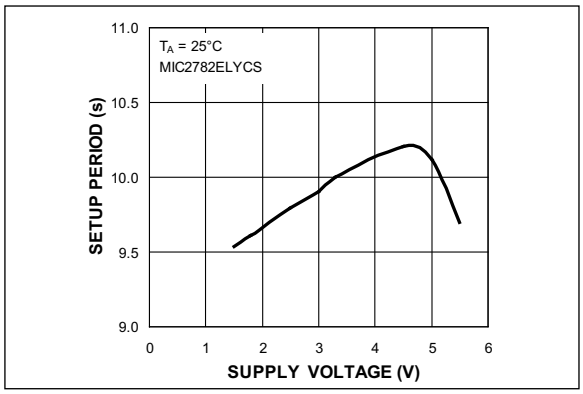


FIGURE 2-6: *Setup Period vs. Supply Voltage.*

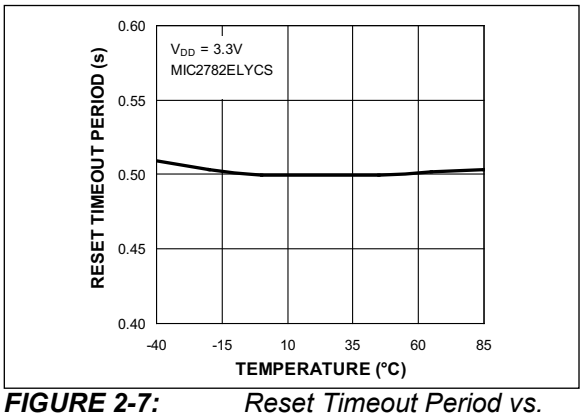


FIGURE 2-7: *Reset Timeout Period vs. Temperature.*

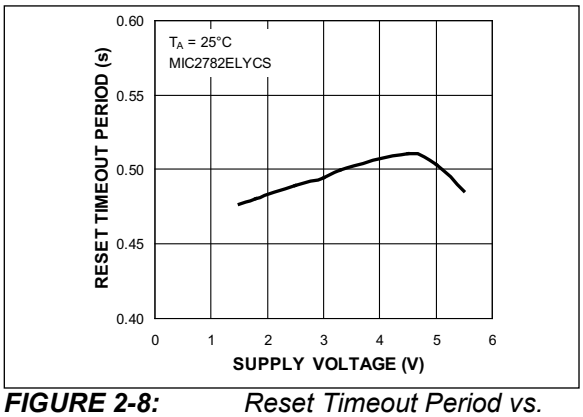


FIGURE 2-8: *Reset Timeout Period vs. Supply Voltage.*

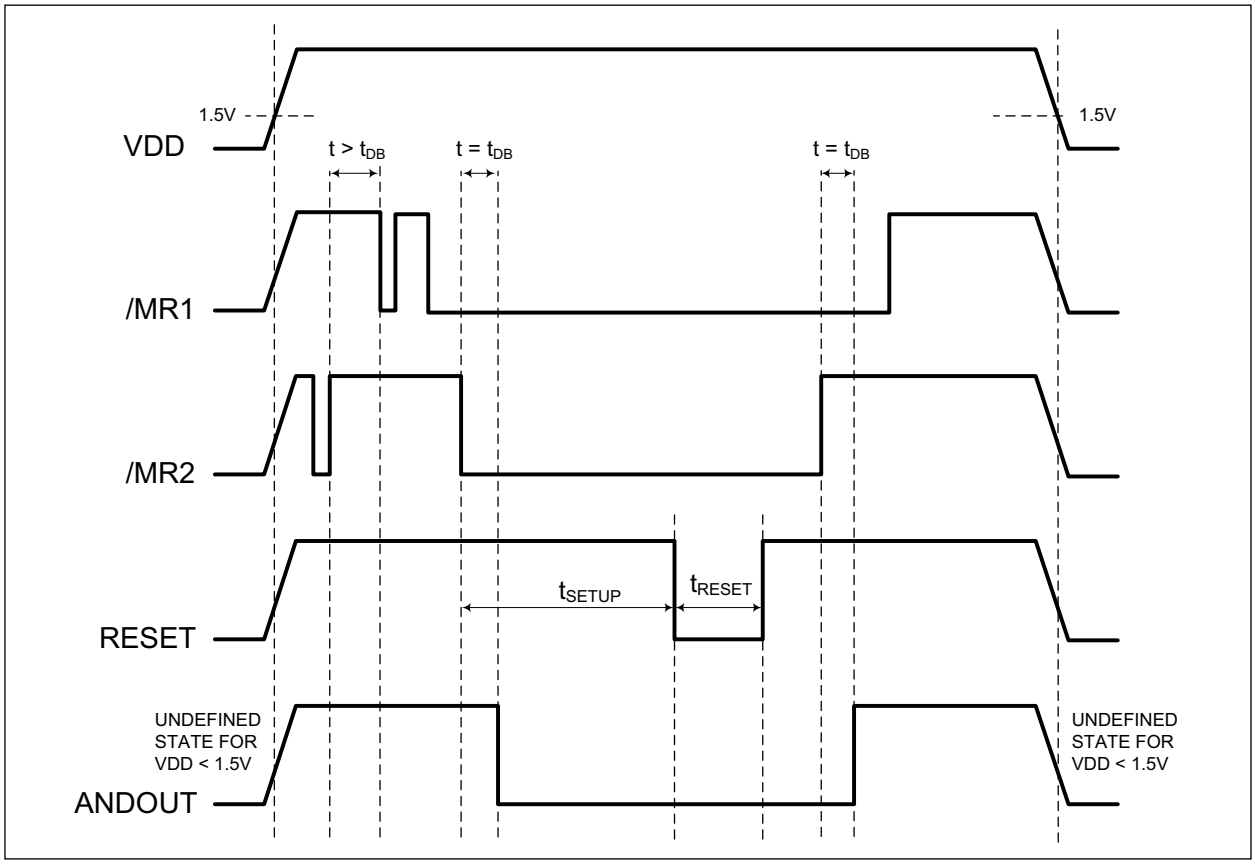
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
A1	ANDOUT	NMOS Open-Drain Output, Active-Low. Asserts low 1.5 ms after /MR1 and /MR2 are both asserted low. Connect a resistor greater than 5 kΩ from the ANDOUT pin to VDD in order to pull up the ANDOUT output voltage when inactive. No ESD diode from ANDOUT to VDD. Please see the Functional Description and Timing Diagram sections for further details of how the ANDOUT output functions.
A2	/MR2	Manual Reset Input 2, Active-Low. Internal 65 kΩ (typical) pull-up resistor to VDD. Pulling both manual reset inputs low for longer than the setup period causes one RESET output pulse for the reset timeout delay period.
B1	RESET	NMOS Open-Drain Output, Active-Low. Asserts low after /MR1 and /MR2 have both asserted low for longer than setup period. Connect a resistor greater than 5 kΩ from the RESET pin to VDD in order to pull up the RESET output voltage when inactive. No ESD diode from RESET to VDD. Please see the Functional Description and Timing Diagram sections for further details of how the RESET output functions.
B2	/MR1	Manual Reset Input 1, Active-Low. Internal 65 kΩ (typical) pull-up resistor to VDD. Pulling both manual reset inputs low for longer than the setup period causes one RESET output pulse for the reset timeout delay period.
C1	VDD	Supply Voltage. Bypass to ground with minimum 0.1 µF capacitor.
C2	GND	Supply Ground.

Timing Diagram



4.0 FUNCTIONAL DESCRIPTION

The MIC2782 is a dual push-button input reset IC with extended setup delay times. It is used for generating a hard reset for microcontrollers, PMICs, or load disconnect switches. The dual manual reset inputs and long setup delay times help protect against accidental system resets. The fixed reset timeout period allows for more predictable phone or tablet operation during hardware resets. It is used in applications such as smartphones, tablets, personal navigation devices, MP3 players, and set-top boxes (STB).

4.1 General Functionality

As shown in Figure 4-1, if both /MR1 and /MR2 are asserted low for longer than the setup period (t_{SETUP}), the RESET output will be asserted (logic-level low) for a reset timeout period (t_{RESET}). During the setup period, if either of the /MR1 or /MR2 inputs are deasserted high, then the setup period timer will be reset. To assert the RESET output low again, both the /MR1 and /MR2 inputs will have to be asserted low together for the full duration of the setup period.

If both /MR1 and /MR2 are asserted low for longer than the debounce time (t_{DB}), then the ANDOUT output will be asserted, (logic-level low). ANDOUT will remain asserted low as long as both the /MR1 and /MR2 inputs are asserted low. If either the /MR1 or /MR2 are deasserted for longer that the debounce time (t_{DB}), then the ANDOUT output will deassert high.

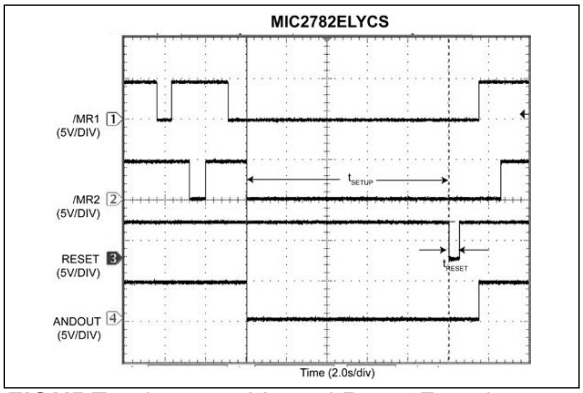


FIGURE 4-1: *Manual Reset Function.*

Keeping both manual reset inputs low for a longer time does not generate additional RESET output pulses. Deasserting either manual reset input during the RESET pulse duration, will not reset the setup timer. After the RESET pin has deasserted high, both the manual reset inputs must be held high for more than a debounce time to reset the setup timer.

ANDOUT debounce time is a de-glitch time, typically 1.5 ms, that senses the asserting of both manual reset inputs low together. A de-glitch time is needed if the manual reset inputs come from noisy push-button sources. If either manual reset inputs are asserted (or deasserted) for less than a debounce time, the ANDOUT output will not respond.

4.2 Dual Manual Reset Inputs (/MR1, /MR2)

The /MR1, /MR2 are active-low manual inputs that have integrated 65 kΩ pull-up resistors to the VDD power supply. If both inputs are asserted (logic-level low) for a setup period (t_{SETUP}), only one reset pulse, of width t_{RESET}, is generated. The behavior of the RESET and ANDOUT outputs is independent of the order in which the /MR1, /MR2 inputs are driven low. The MIC2782 consumes only 2 µA when /MR1 and /MR2 manual inputs are deasserted (logic-level high) together. Current consumption is typically 120 µA when both manual inputs are asserted low together and 55 µA when only one of the manual inputs is asserted low while the other manual input is deasserted high.

4.3 Outputs (RESET and ANDOUT)

The RESET and ANDOUT outputs are simple open-drain N-channel MOSFET structures that require a pull-up resistor. For most applications, the pull-up voltage will be the same as the power supply that supplies V_{DD} to the MIC2782. As shown in Figure 4-2, it is possible to tie this resistor to a voltage other than V_{DD}, thus enabling level-shifting of the RESET or ANDOUT outputs. The pull-up voltage must be limited to 5.5V to avoid damaging the MIC2782. The pull-up resistor must be small enough to supply current to the inputs and leakage paths that are driven by the RESET or ANDOUT outputs. A recommended value is 100 kΩ.

Because the RESET and ANDOUT outputs are open-drain, several reset sources can be wire-ORed, in parallel, to allow resets from multiple sources.

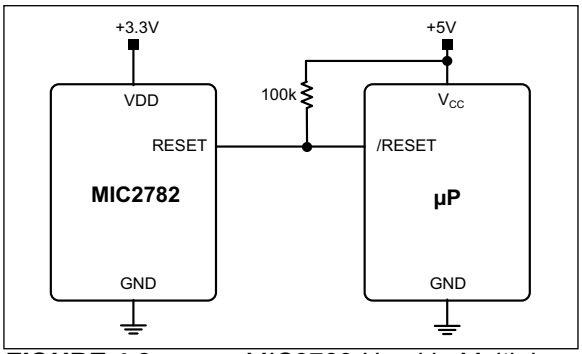


FIGURE 4-2: *MIC2782 Used in Multiple Supply System.*

4.4 Bypass Capacitor from VDD to GND

A 0.1µF input bypass capacitor must be placed from VDD (Pin C1) to GND (Pin C2).

5.0 EVALUATION BOARD SCHEMATIC

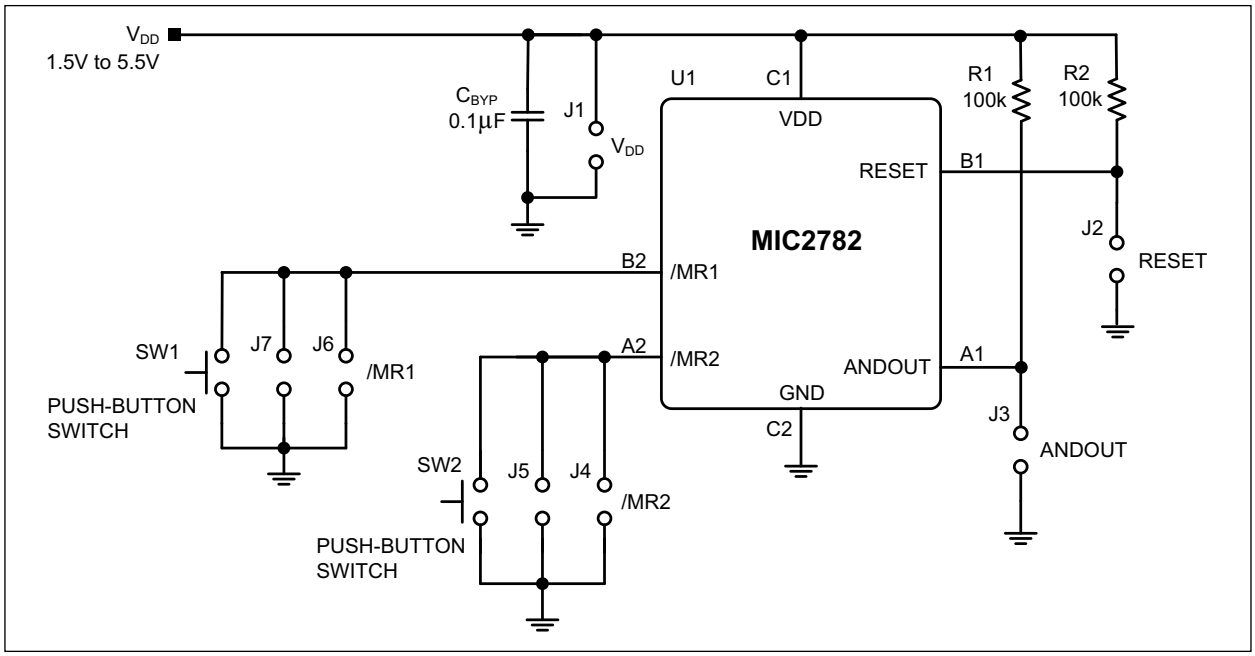


TABLE 5-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM188R71C104KA01D	Murata	0.1 µF, 16V capacitor, X7R, 0603	1
R1, R2	CRCW0603100KJNEA	Vishay	100 kΩ, 5% resistor, 0603	2
U1	MIC2782ELYCS	Microchip Technology Inc.	Dual-Input Push Button Reset IC	1

6.0 PCB LAYOUT RECOMMENDATIONS

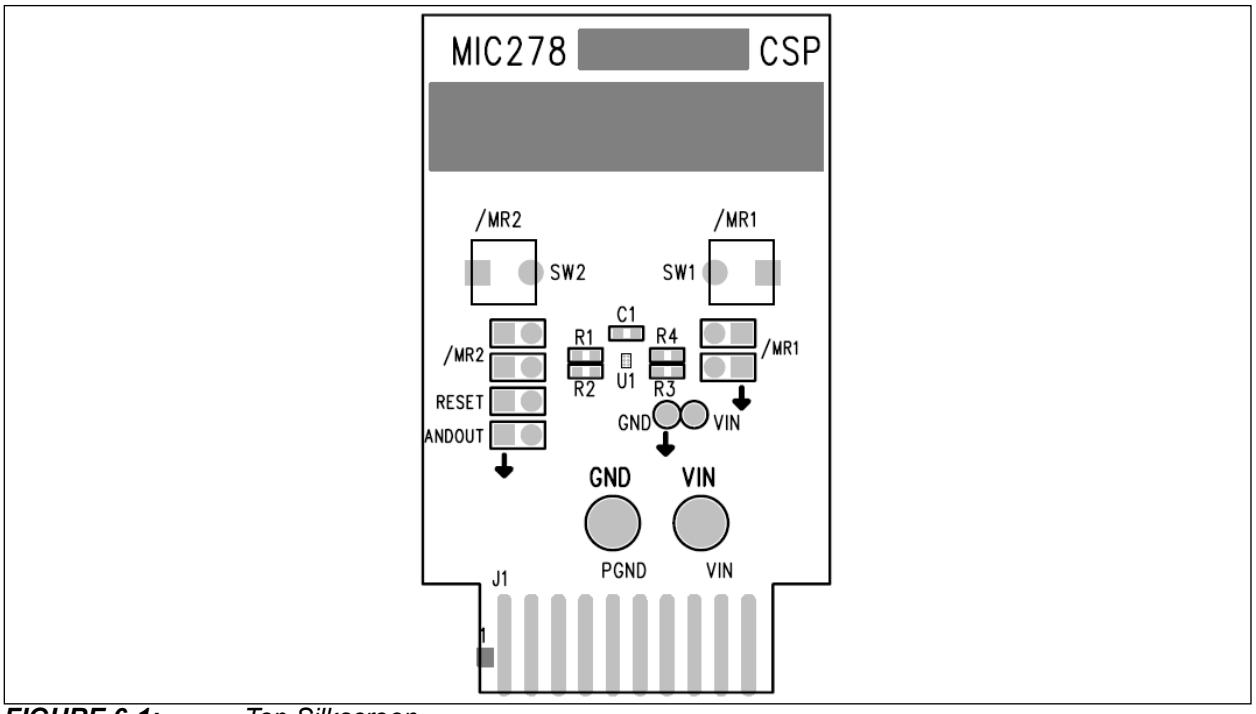


FIGURE 6-1: *Top Silkscreen.*

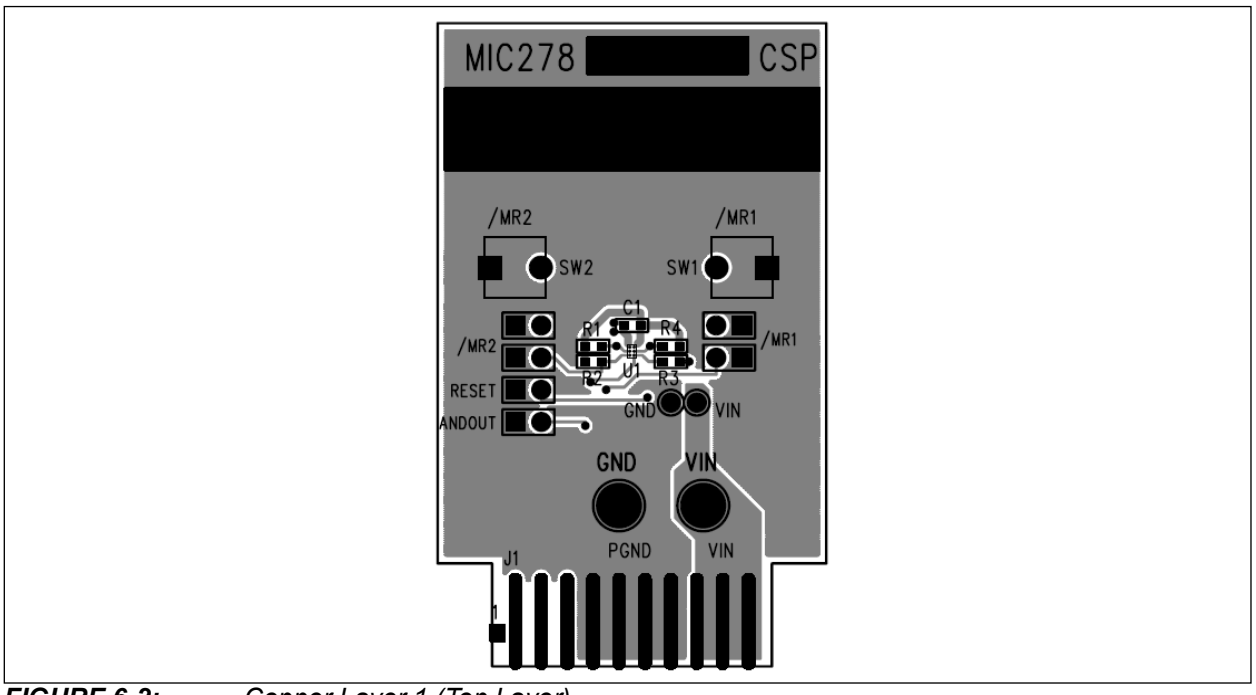


FIGURE 6-2: *Copper Layer 1 (Top Layer).*

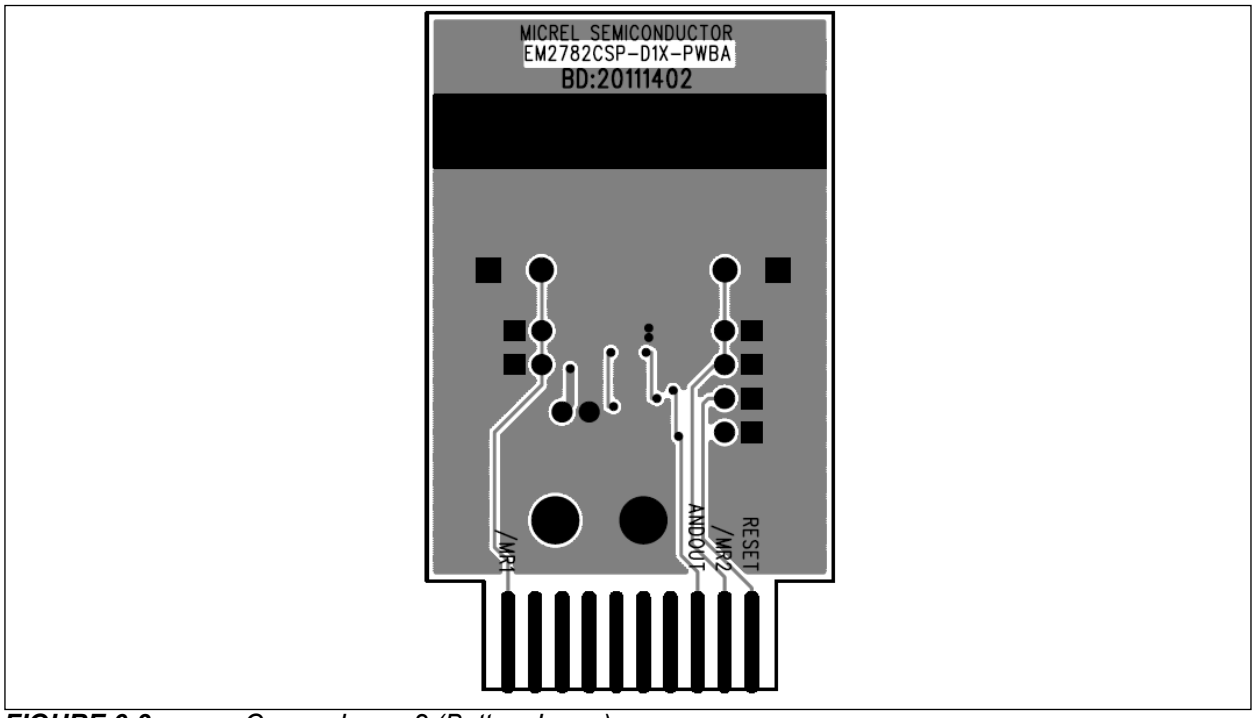


FIGURE 6-3: *Copper Layer 2 (Bottom Layer).*

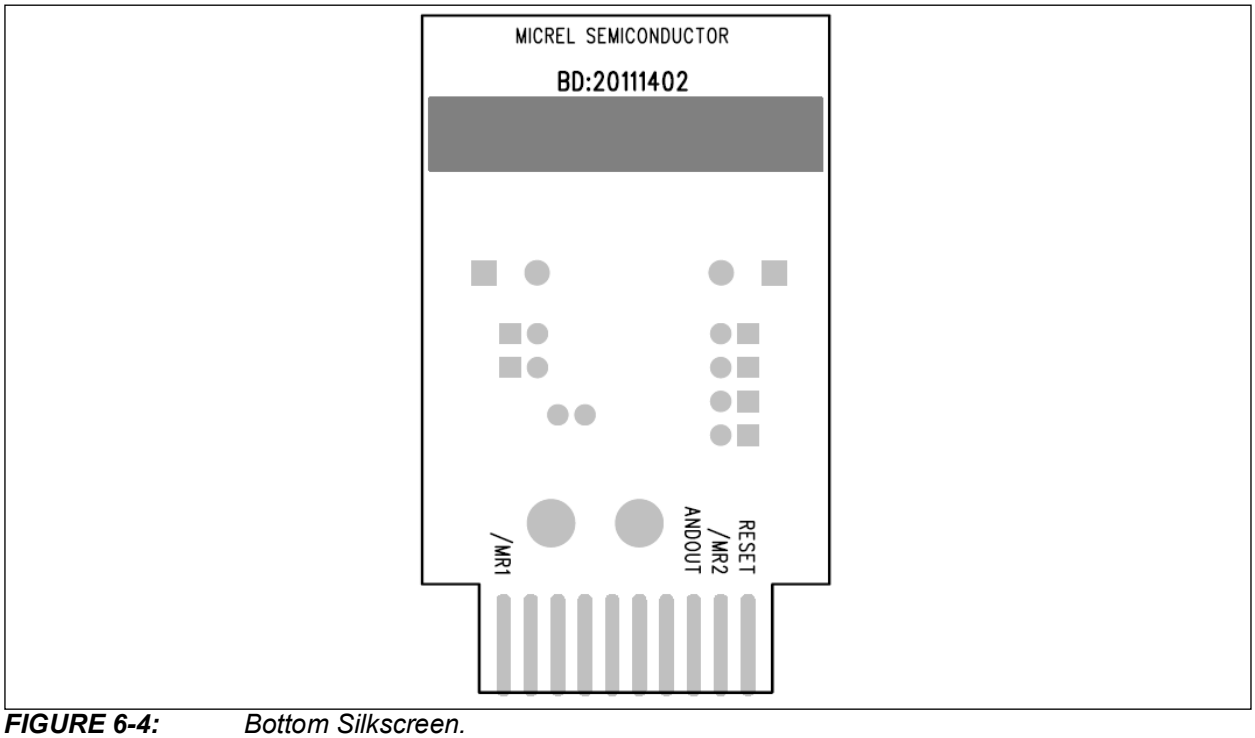
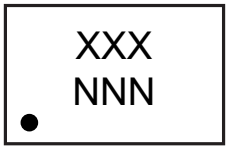


FIGURE 6-4: *Bottom Silkscreen.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

6-Bump WLCSP*



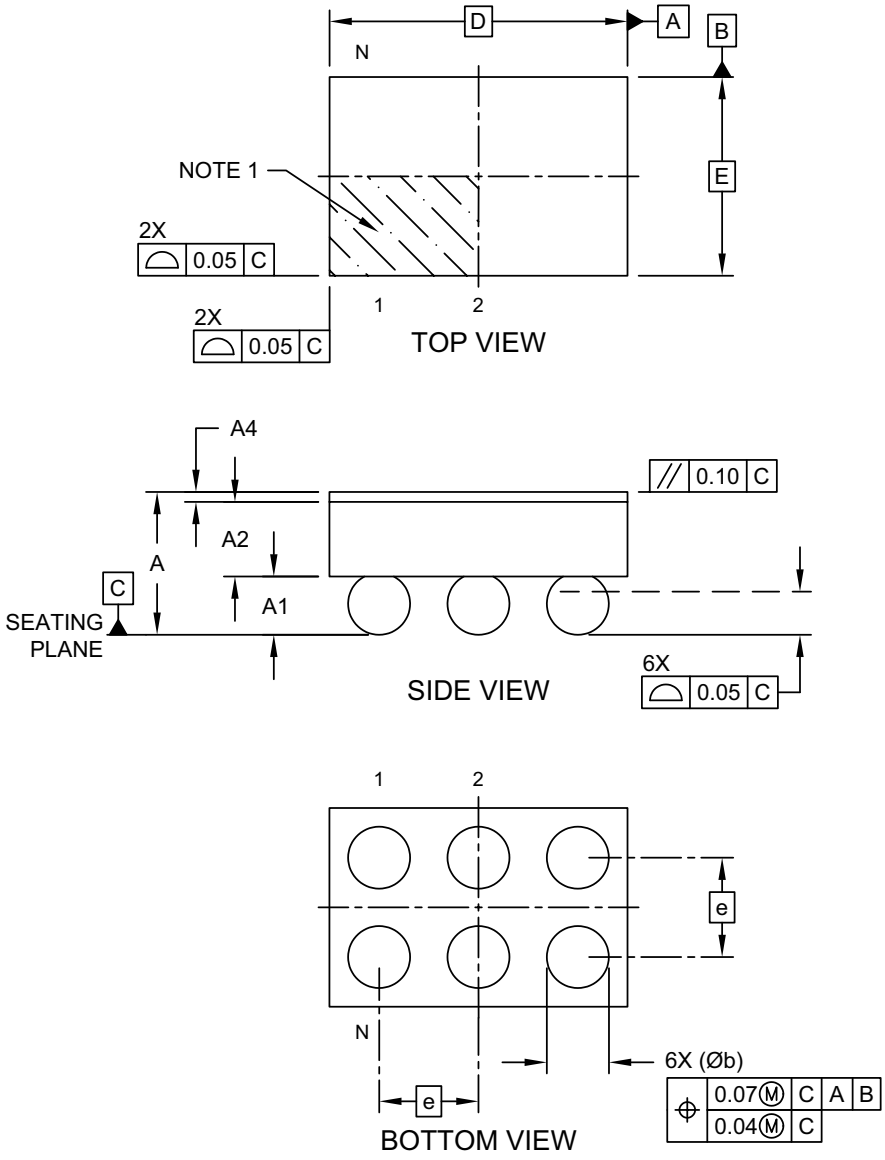
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)*	Pb-free JEDEC® designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

6-Ball Wafer Level Chip Scale Package (FMA) - 1.2x0.8x0.575 mm Body [WLCSP]
Micrel Legacy Package WLCSP080120D-6BL-PL-9

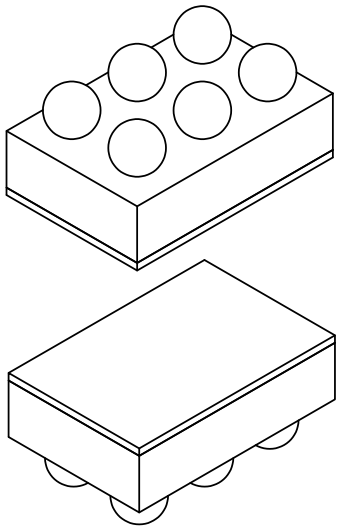
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1188-FMA Rev B Sheet 1 of 2

6-Ball Wafer Level Chip Scale Package (FMA) - 1.2x0.8x0.575 mm Body [WLCSP]
Micrel Legacy Package WLCSP080120D-6BL-PL-9

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.40 BSC	
Overall Height	A	0.475	0.525	0.575
Standoff	A1	0.14	0.19	0.24
Chip Thickness	A2	0.26	0.31	0.36
Backside Laminate Thickness	A4	0.020	0.025	0.030
Overall Length	D		1.20 BSC	
Overall Width	E		0.80 BSC	
Terminal Width	b		0.25 REF	

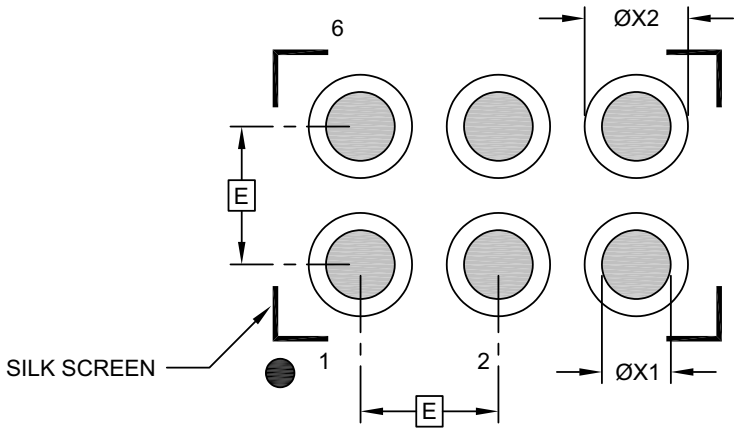
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1188-FMA Rev B Sheet 2 of 2

6-Ball Wafer Level Chip Scale Package (FMA) - 1.2x0.8x0.575 mm Body [WLCSP]
Micrel Legacy Package WLCSP080120D-6BL-PL-9

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Diameter	X1			0.22
Solder Mask Opening Diameter	X2			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3188-FMA Rev B

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2024)

- Converted Micrel document MIC2782 to Microchip data sheet DS20006941A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	X	X	X	XX	-XX
Device	Setup Period	Reset Timeout Period	Temp. Range	Package	Media Type

Device:	MIC2782:		Dual-Input Push Button Reset IC with Immediate and Delayed Outputs
Setup Period:	C	=	6 seconds
	D	=	8 seconds
	E	=	10 seconds
	F	=	12 seconds
Reset Timeout Period	L	=	0.5 second
	M	=	1 second
	R	=	2 seconds
Temperature Range:	Y	=	–40°C to +85°C
Package:	CS	=	6-Bump 0.8 mm x 1.2 mm WLCSP
Media Type:	TR	=	3,000/Reel

Examples:

a) MIC2782CLYCS-TR:

MIC2782, 6 second setup period, 0.5 second reset timeout, –40°C to +85°C Temp. Range, 6-Bump WLCSP, 3,000/Reel

b) MIC2782DRYCS-TR:

MIC2782, 8 second setup period, 2 second reset timeout, –40°C to +85°C Temp. Range, 6-Bump WLCSP, 3,000/Reel

c) MIC2782FLYCS-TR:

MIC2782, 12 second setup period, 0.5 second reset timeout, –40°C to +85°C Temp. Range, 6-Bump WLCSP, 3,000/Reel

d) MIC2782FRYCS-TR:

MIC2782, 12 second setup period, 2 second reset timeout, –40°C to +85°C Temp. Range, 6-Bump WLCSP, 3,000/Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MARKING CODES

Part Number	Marking	Setup Period	Reset Timeout Period
MIC2782CLYCS	UJA	6 seconds	0.5 second
MIC2782CRYCS	UJC	6 seconds	2 seconds
MIC2782DLYCS	UKU	8 seconds	0.5 second
MIC2782DRYCS	UJE	8 seconds	2 seconds
MIC2782ELYCS	UKW	10 seconds	0.5 second
MIC2782EMYCS	UKX	10 seconds	1 second
MIC2782FLYCS	UJF	12 seconds	0.5 second
MIC2782FRYCS	UKZ	12 seconds	2 seconds

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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