USB2640

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB2640. These checklist items should be followed when utilizing the USB2640 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 19. Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "Card Reader Interface"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Configuration Options"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB2640 implementor should have the following documents on hand:

- *USB2640 Data Sheet*
- USB2.0 Specification
- MultiMediaCard 4.2 Specification
- Secure Digital 2.0 Specification
- Other references on the product page at www.microchip.com

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground ePad, **VSS**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connector

- USB-IF certified USB Connector with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

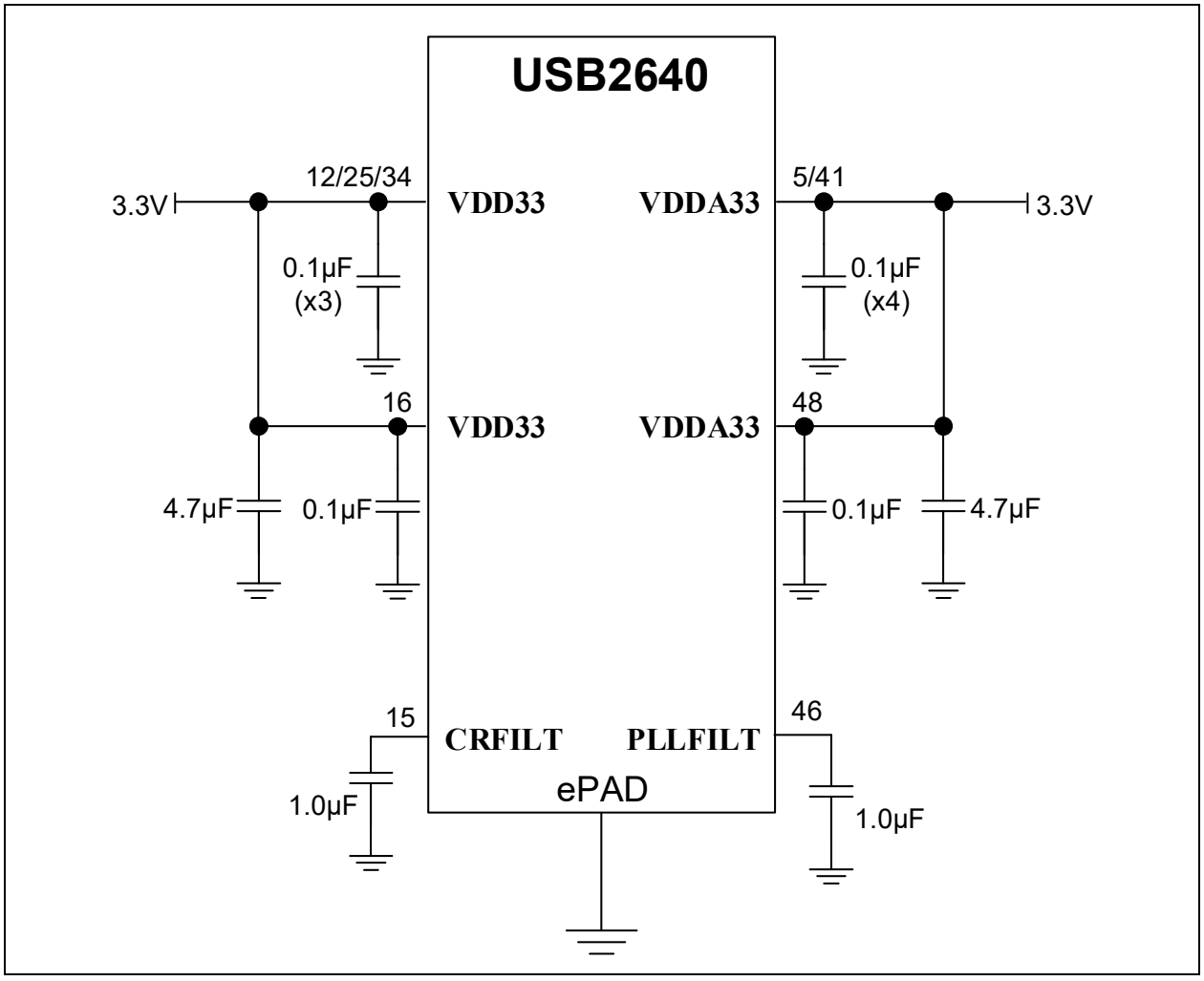
3.0 POWER

- The 3.3V supplies (**VDD33/VDDA33**) are the analog and digital domain power supply inputs. They are located on pins 5, 12, 16, 25,34, 41, and 48. These pins require a connection to a regulated 3.3V power plane and each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pins 16 (**VDD33**) and 48 (**VDDA33**) each also require a 4.7 µF bulk capacitor.
- Pin 46 (**PLLFILT**) is a power bypass for the PLL and should connect to an external filter capacitor. A 1.0 µF capacitor is recommended. Do not power external circuitry from this regulator output.

- Pin 15 (**CRFILT**) is a digital core regulator output and should connect to an external filter capacitor. A 1.0 µF capacitor is recommended. Do not power external circuitry from this regulator output.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



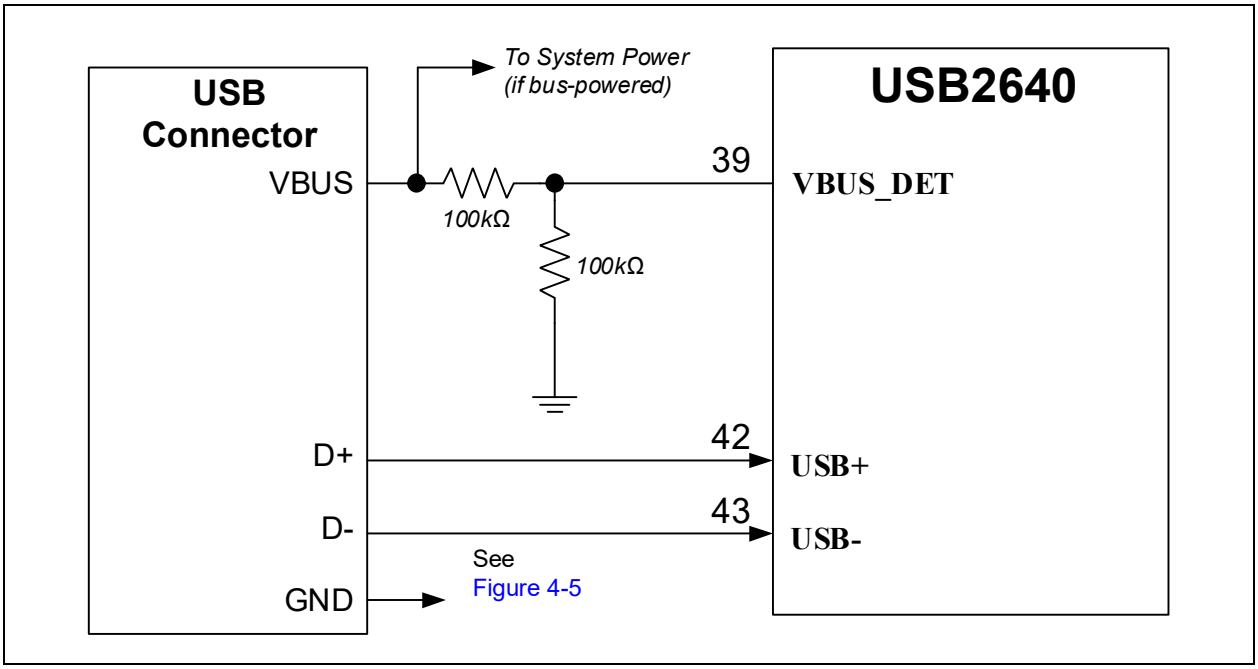
4.0 USB SIGNALS

4.1 Upstream USB Interface

- **USB+** (pin 42): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB connector.
- **USB–** (pin 43): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB Connector.
- **VBUS_DET** (pin 39): This pin is used to detect the presence of a USB host. Since a standard VBUS supply is nominally 5V, VBUS must be divided down to a voltage level that it can accept. The **VBUS_DET** pin uses 3.3V logic levels, so a resistor divider consisting of two 100 kΩ resistors is generally recommended, even though precise values are not critical as long as logical high is presented to the pin when a valid VBUS voltage is present on the USB connector.
  - **Optional:** An additional capacitor and/or ferrite bead between the **VBUS** pin of the USB connector and the **VBUS_DET** pin provides the device some immunity from noise or transients on the **VBUS** line. It is generally recommended to design in extra population options for series and parallel components which may be added to the system if additional components are deemed necessary during system testing or qualification.

For transmit and receive channel connection details, refer to Figure 4-1.

FIGURE 4-1: USB DATA SIGNAL CONNECTIONS



4.2 Downstream USB Ports

4.2.1 USB PHY INTERFACE

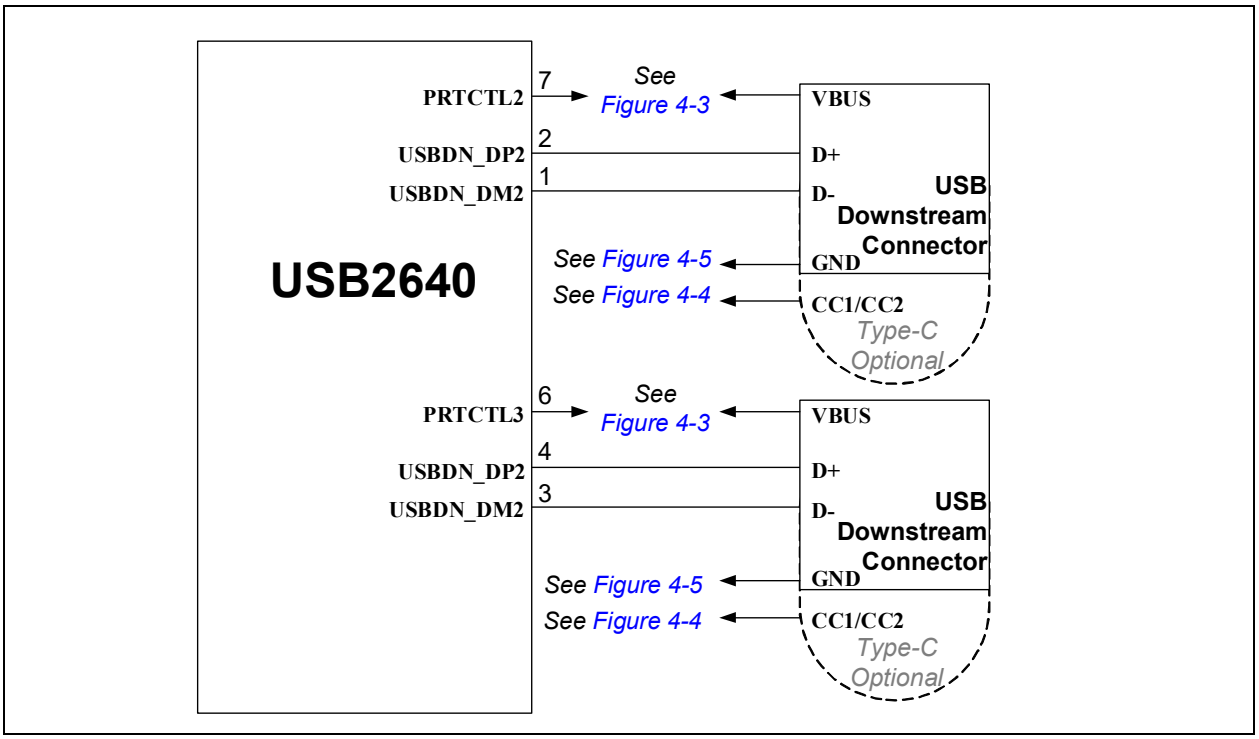
- **USBDN_DP1** (pin 2): This pin is the positive (+) signal of the downstream Port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **USBDN_DM1** (pin 1): This pin is the negative (–) signal of the downstream Port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB Connector.
- **USBDN_DP2** (pin 4): This pin is the positive (+) signal of the downstream Port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.

- **USBDN_DM1** (pin 1): This pin is the negative (–) signal of the downstream Port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.

Note:	The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^2C configuration registers.

For transmit and receive channel connection details, refer to Figure 4-2.

FIGURE 4-2: USB DOWNSTREAM PORT DATA SIGNAL CONNECTIONS



4.2.2 DISABLE DOWNSTREAM PORTS IF UNUSED

If any downstream of the USB2640 is unused, it should be disabled. This can be achieved through hub configuration (I2C), or through a port disable strap option.

4.2.3 DOWNSTREAM PORT CONTROL SIGNALS (PRTCTLX)

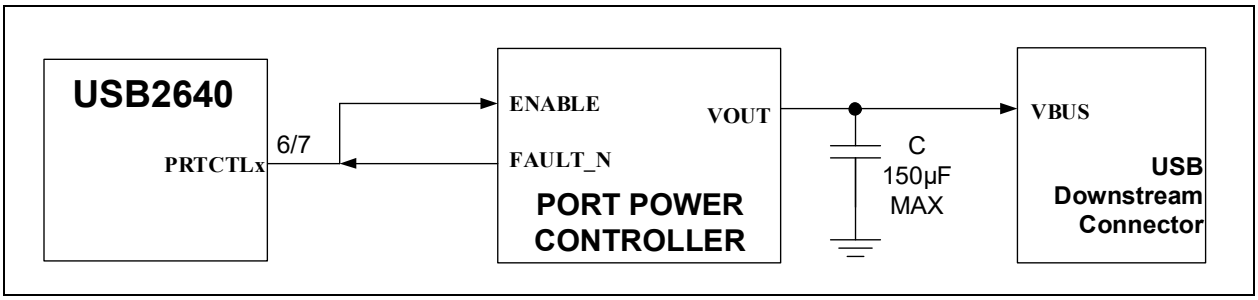
The **PRTCTLx** pin is an output pin which has the following states:

- PORT OFF: **PRTCTLx** is an output and drives low. The **PRTCTLx** pin will only transition to the PORT ON state through a specific command from the USB host.
- PORT ON: **PRTCTLx** enables internal pull-up resistor and switches to Input mode. While in this state, the input buffer monitors for overcurrent events. An overcurrent event is detected if the state of the pin is detected as low (below the V_{ILI} voltage). The port moves to the PORT OFF state after one of the following events:
  - An overcurrent event is sensed when the state of the pin is detected as low (below the V_{ILI} voltage).
  - A command from the USB host is received which instructs the hub to disable power.
  - The hub is reset or experiences a POR event.

To ensure minimal BOM cost and simplicity, select a port power controller device with a 3.3V logic level, active-high enable input, and an open-drain, active-low FAULT indication output signal. If a device which operates from a 5V logic level is selected, the **PRTCTLx** signal may need to be boosted using external logic. If a port power controller with an active-low input is selected, the **PRTCTLx** signal needs to be inverted using external logic.

A typical VBUS port power control implementation is shown in Figure 4-3.

FIGURE 4-3: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS



Note:	The implementation, as shown in Figure 4-3, assumes that the port power controller has an active-high enable input, and an active-low, open-drain style FAULT indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

4.2.4 DOWNSTREAM PORT TYPE-C SUPPORT

The USB2640 may be used with Type-C as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The USB2640 simply controls the Type-C port controller in the same way as it would control a standard Type-A port power controller. The USB2640 does not require any kind of Type-C port status information from the Type-C port controller. The **PRTCTLx** signal should be connected to an enable pin on the Type-C controller and the FAULT indicator output of the port power controller should also connect back to the **PRTCTLx** signal.

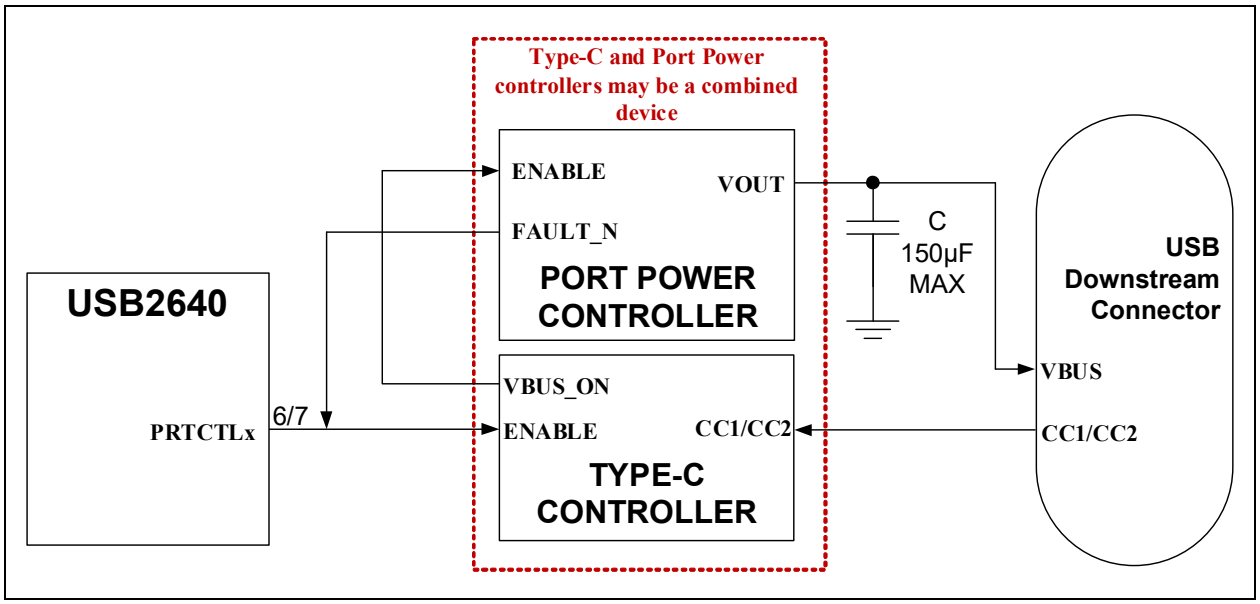
If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the enable pin of the port power controller switch supplying VBUS to the connection. The **PRTCTLx** should not directly control the VBUS enable signal of the port power controller.

A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. (However, per the USB specification, Type-C ports may not advertise a 500 mA capability. That power level is reserved for legacy port cable adapters alone). The selected port power controller should be sized accordingly.

Note:	It is not possible to implement a USB Type-C® downstream port that is compliant to all USB Type-C specification without utilizing a Type-C port controller device. The required functionality is not practical to achieve solely using discrete analog circuitry.

A typical implementation is shown in Figure 4-4.

FIGURE 4-4: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS WITH A TYPE-C PORT



Note: The implementation, as shown in Figure 4-4, assumes that the Type-C controller has an active-high enable input, and the port power controller has an active-low, open-drain style FAULT indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller and/or port power controller has different I/O characteristics.

4.3 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

1. TVS protection diodes
   - ESD protection for IEC-61000-4-2 system level tests
2. Application targeted protection ICs or galvanic isolation devices
   - DC overvoltage protection for short to battery protection
3. Common-mode chokes
   - For EMI reduction

The USB2640 can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementa-tion guidelines from the manufacturer of these devices. You may also use the following general guidelines for imple-menting these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- These devices should be placed as close to the USB connector as possible.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note:	Microchip PHYBoost configuration options are available for compensating the negative effects of these devices. This feature may help overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

4.4 GND and SHIELD Recommendations

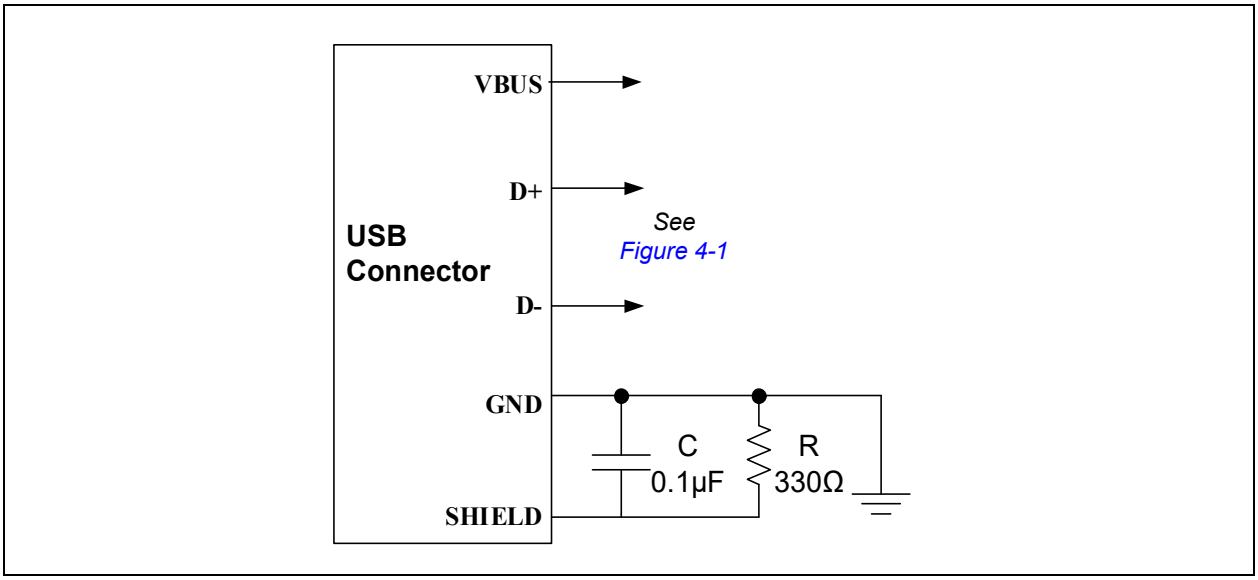
The **GND** pins of the USB connector must be connected to the PCB with a low impedance path directly to a large **GND** plane.

The **SHIELD** pins of the USB connector may be connected in one of two ways:

1. [Recommended] To **GND** through an resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
2. Directly to the **GND** plane.

The recommended implementation is shown in Figure 4-5.

FIGURE 4-5: RECOMMENDED USB CONNECTOR GND AND SHIELD CONNECTIONS



5.0 CARD READER INTERFACE

5.1 Secure Digital/Multi-MediaCard Slot

- The USB2640 supports Secure Digital (SD) 2.0, including HS-SD and SDHC media. Newer media and small-form-factor SD media (i.e. microSD) are also supported due to backward compatibility requirements on all compliant SD media although newer features and performance cannot be taken advantage of.
- 1/4/8-bit MultiMediaCard™ (MMC) 4.2 is also supported on the same interface and card slot. Newer MMC media and eMMC media is also supported due to backward compatibility requirements on all compliant MMC media although newer features and performance cannot be taken advantage of.
- If designing with a standard SD/MMC card slot, refer to Figure 5-1.
- If designing with an embedded eMMC memory, refer to Figure 5-2.
- If designing with a microSD card slot, refer to Figure 5-3.

FIGURE 5-1: SD/MMC MEDIA SLOT

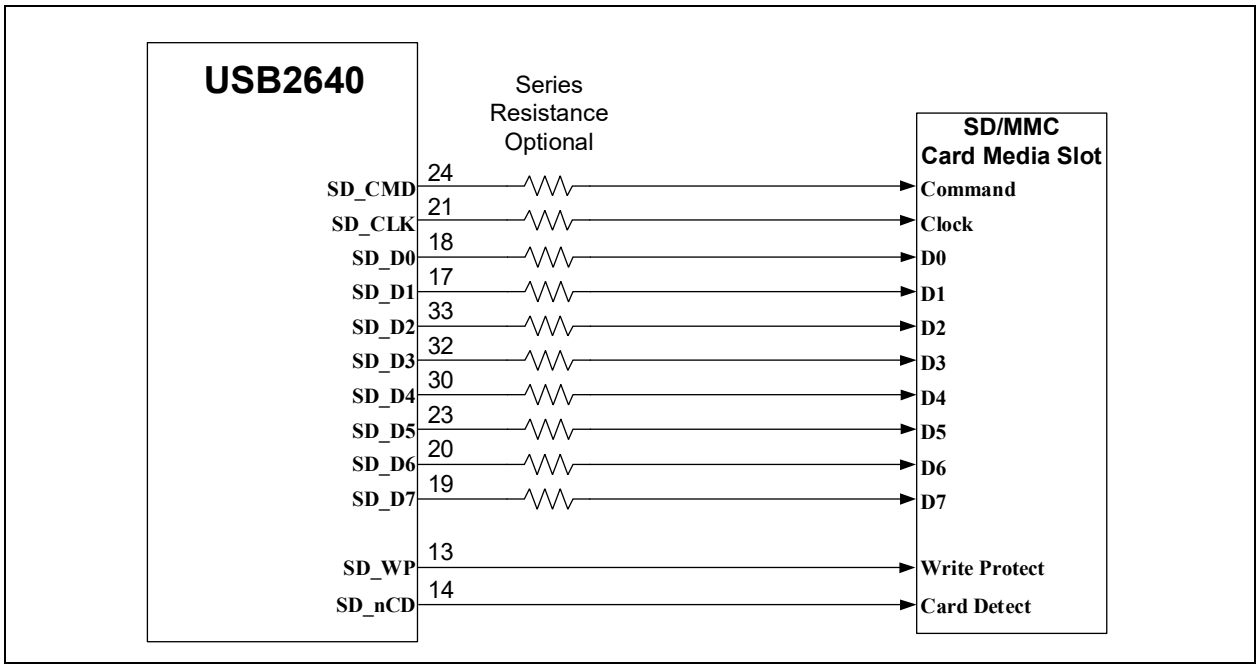


FIGURE 5-2: EMMC (EMBEDDED MMC) MEMORY CONNECTIONS

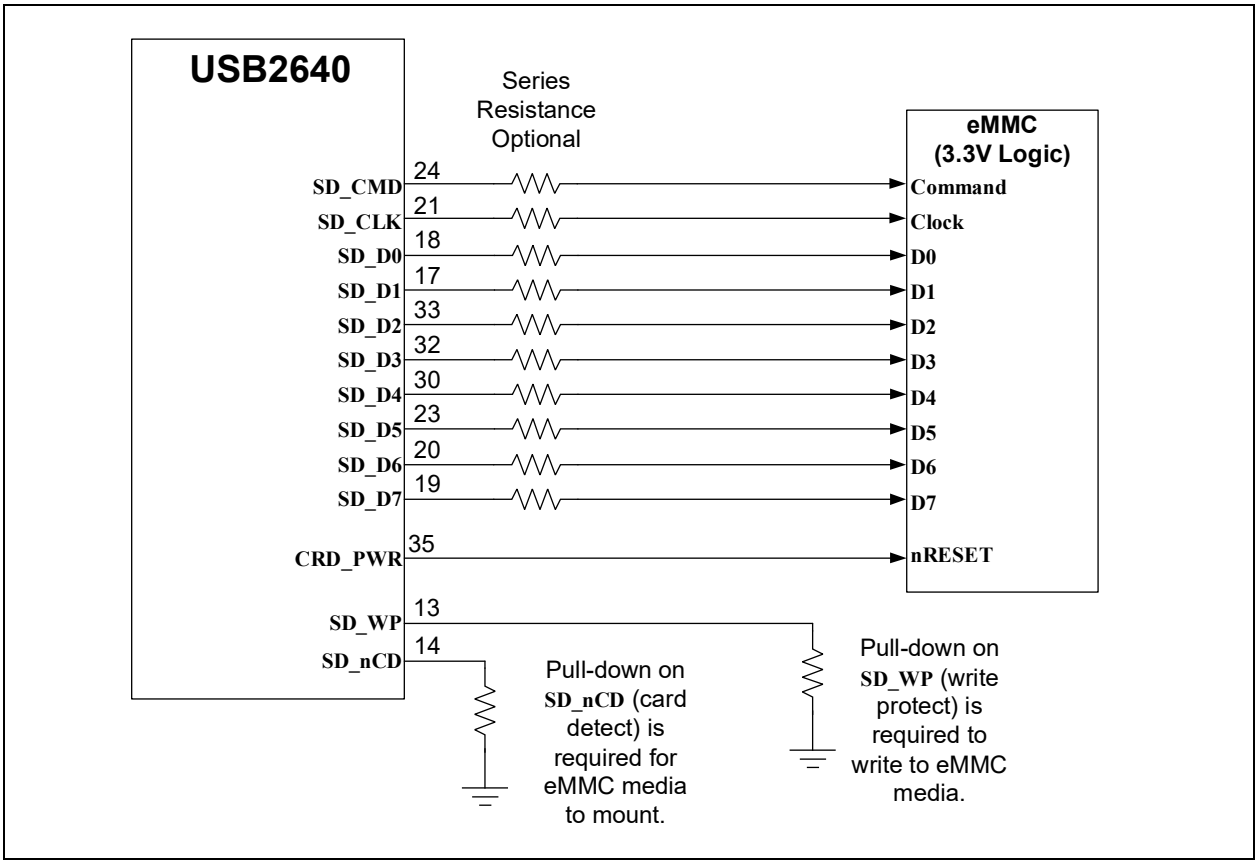
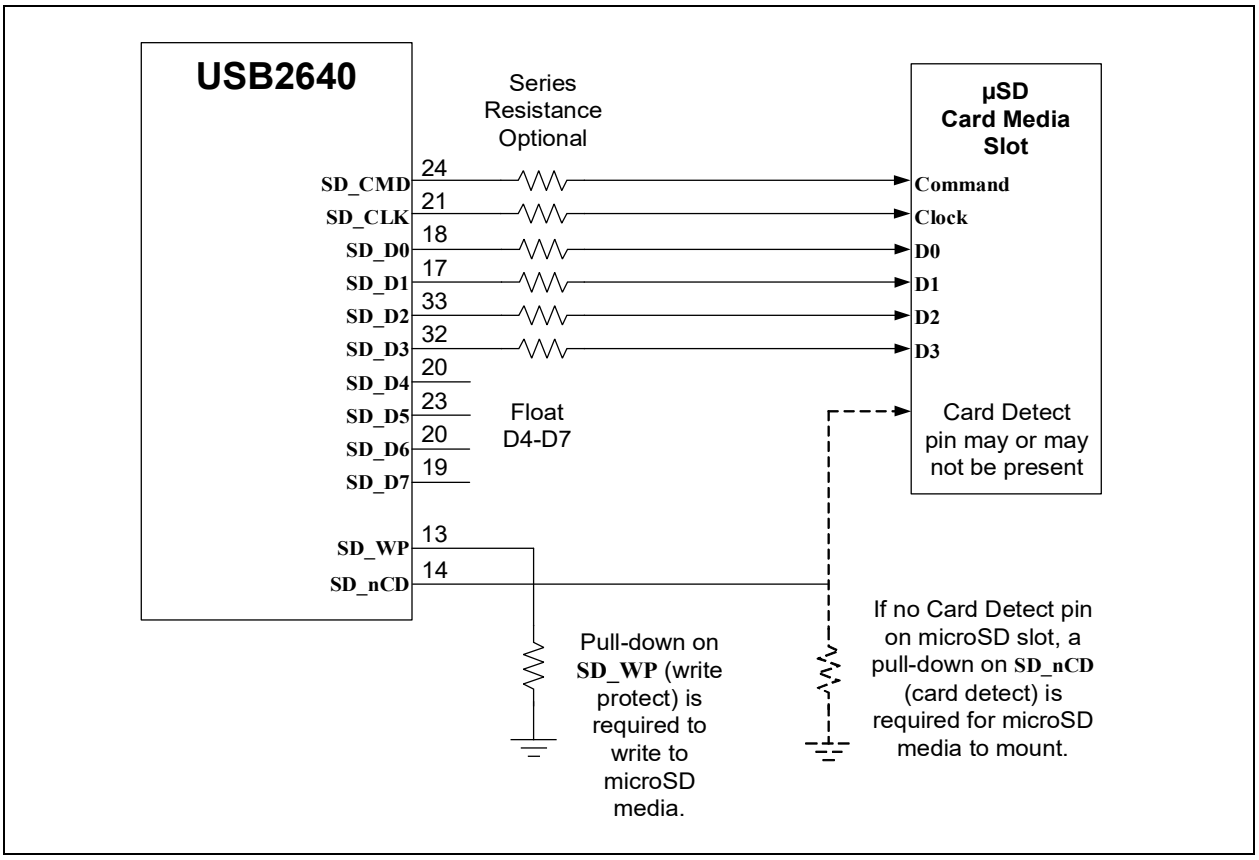


FIGURE 5-3: MICROSD CARD SLOT CONNECTIONS



5.2 xD-Picture Card™ Slot

The USB2640 supports xD-Picture Card™ 1.2 media. If designing with a standard xD-Picture Card slot, follow Figure 5-4.

5.3 Card Power Switch

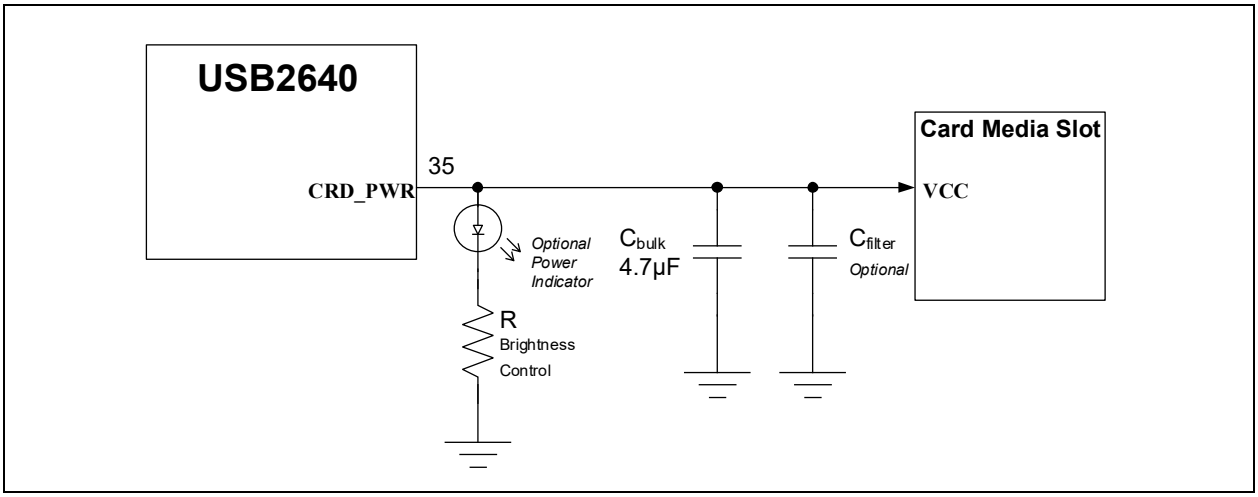
The USB2640 includes an internal 3.3V power switch on **CRD_PWR** capable of supplying up to 200 mA continuously to the attached media. The card power switch includes FAULT protection and will automatically shut off the output if current draw exceeds the 200 mA maximum.

Note:	The default setting for card power current limit is 200 mA. It may be optionally set to 100 mA via EEPROM configuration if desired.

The card power output should include some bulk capacitance to maintain voltage stability during card use. A 4.7 µF ceramic capacitor is sufficient for most-use cases. Certain high-power media may require more. Smaller capacitances can also be added to filter out high-frequency noise if present in the system.

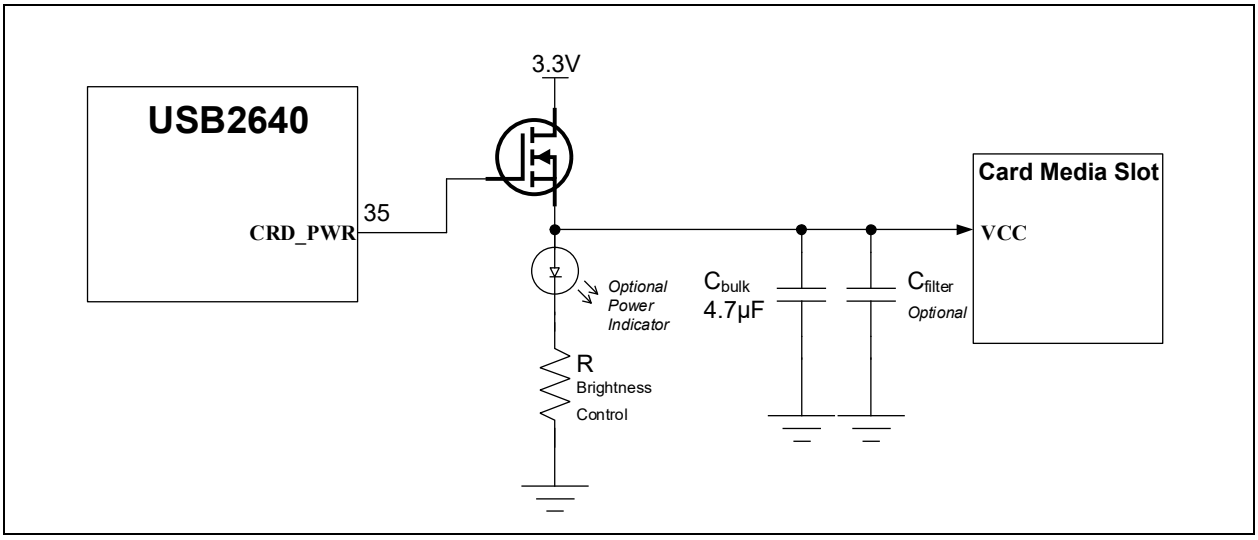
An LED may be optionally connected directly to the card power output to give visual indication of card power.

FIGURE 5-4: CRD_PWR CARD MEDIA POWER SUPPLY SWITCH



If the internal card power switch is not used, it is still recommended to use the **CRD_PWR** pin to control the supply to the card media slot. This allows the internal logic of the USB2640 to reset power to the card during error recovery attempts.

FIGURE 5-5: EXTERNAL CARD POWER SUPPLY SWITCH RECOMMENDED CONNECTIONS



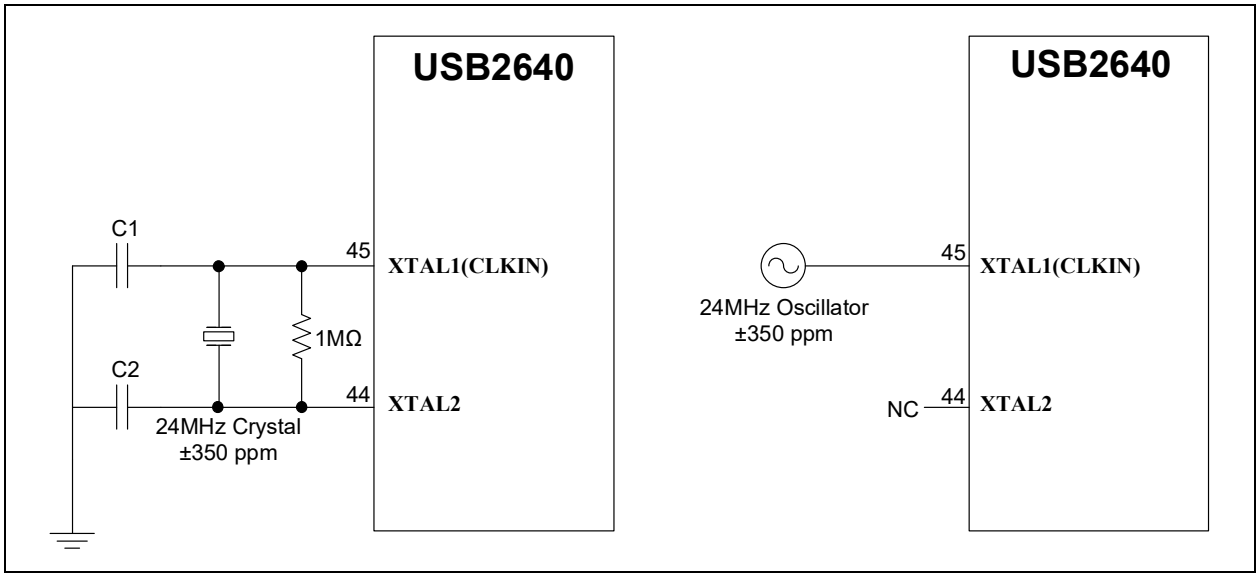
6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 24.000-MHz (±350 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB2640 Data Sheet*.

- **XTAL1(CLKIN)** (pin 45) is the clock circuit input for the USB2640. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTAL2** (pin 44) is the clock circuit output for the USB2640. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- A 1 megohm resistor (1 MΩ) is required connected across the **XTAL1** and **XTAL2** pins.
- The crystal loading capacitor values are system dependent, based on the total C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:
  - $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$
  - Where: CL is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.
  - Note that C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, within the 1 pF to 2 pF range, and then verified by physical experiments in the laboratory if PCB simulation tools are not available.
- Alternately, a 24.000 MHz, 1.2-to-3.3V clock oscillator may be supplied to **XTAL1(CLKIN)** to provide the clock source for the USB2640. When using a single ended clock source, **XTAL2** (pin 44) should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

RBIAS (pin 47) on the USB2640 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close to the IC pin as possible, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB2640 Data Sheet*.

If a monotonic or fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

It is important to size the 3.3V power rails appropriately. The 3.3V power supply must be capable of supplying sufficient power for the USB2640 (up to 330 mA at 3.3V) as well as the card media supported (up to 200 mA if using the internal card power supply output on **CRD_PWR)**.

7.3 Reset Circuit

RESET_N (pin 38) is an active-low Reset input. This signal resets all logic and registers within the USB2640. A hardware Reset (**RESET_N** assertion) is not required following power-up. Please refer to the latest copy of the *USB2640 Data Sheet* for Reset timing requirements. Figure 7-1 shows a recommended Reset circuit for powering up the USB2640 when Reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

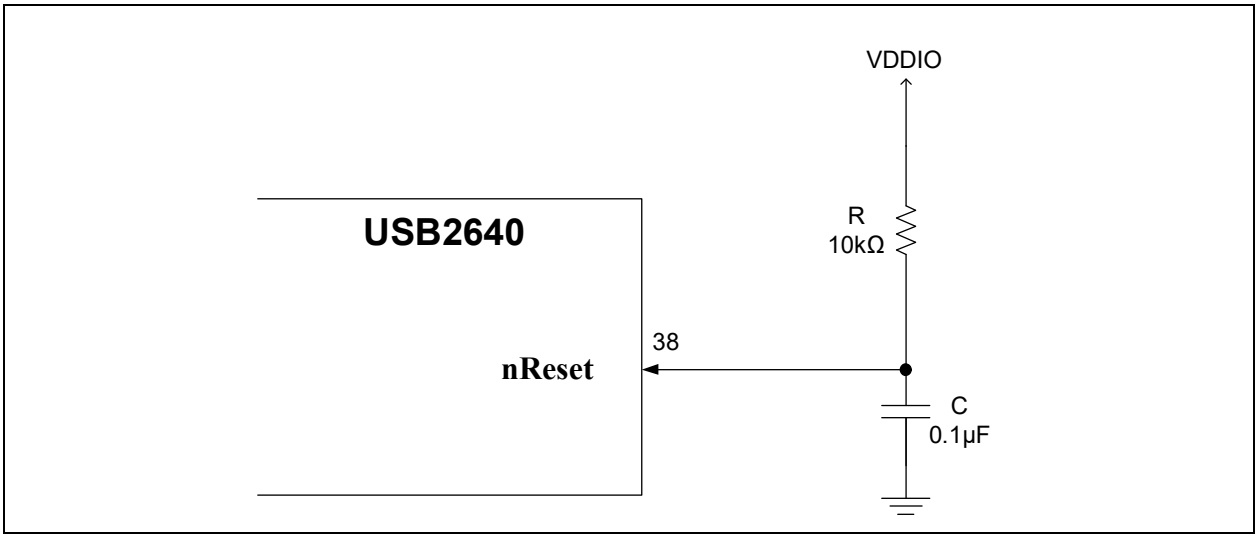
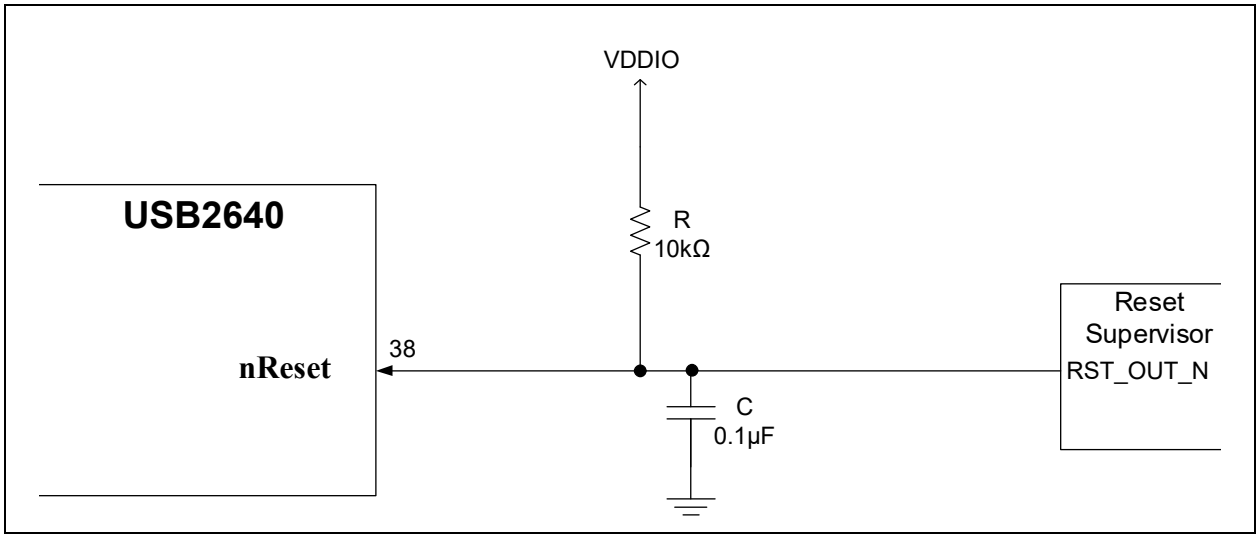


Figure 7-2 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU. The Reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm Reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted to individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 CONFIGURATION OPTIONS

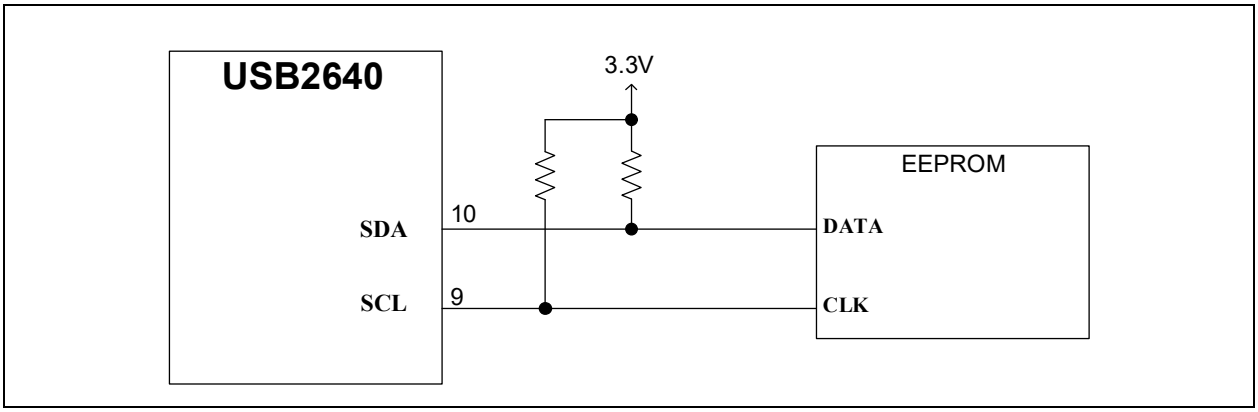
The USB2640 can be configured to allow for customizable vendor, product, and device IDs, serial number, product string descriptors, and more from either of the following methods:

- I2C 512 Byte (512x8) EEPROM memory device
- SPI interface executing a new firmware image in place

8.1 External EEPROM

An external EEPROM is not required for USB2640 operation—internal defaults may be used for many applications. If the external EEPROM is not detected at boot, internal defaults will be loaded. See Figure 8-1.

FIGURE 8-1: EEPROM CONNECTIONS



8.2 External SPI Flash memory

For custom applications, an external SPI Flash may be used to execute a unique firmware image. In most applications, this functionality is not used.

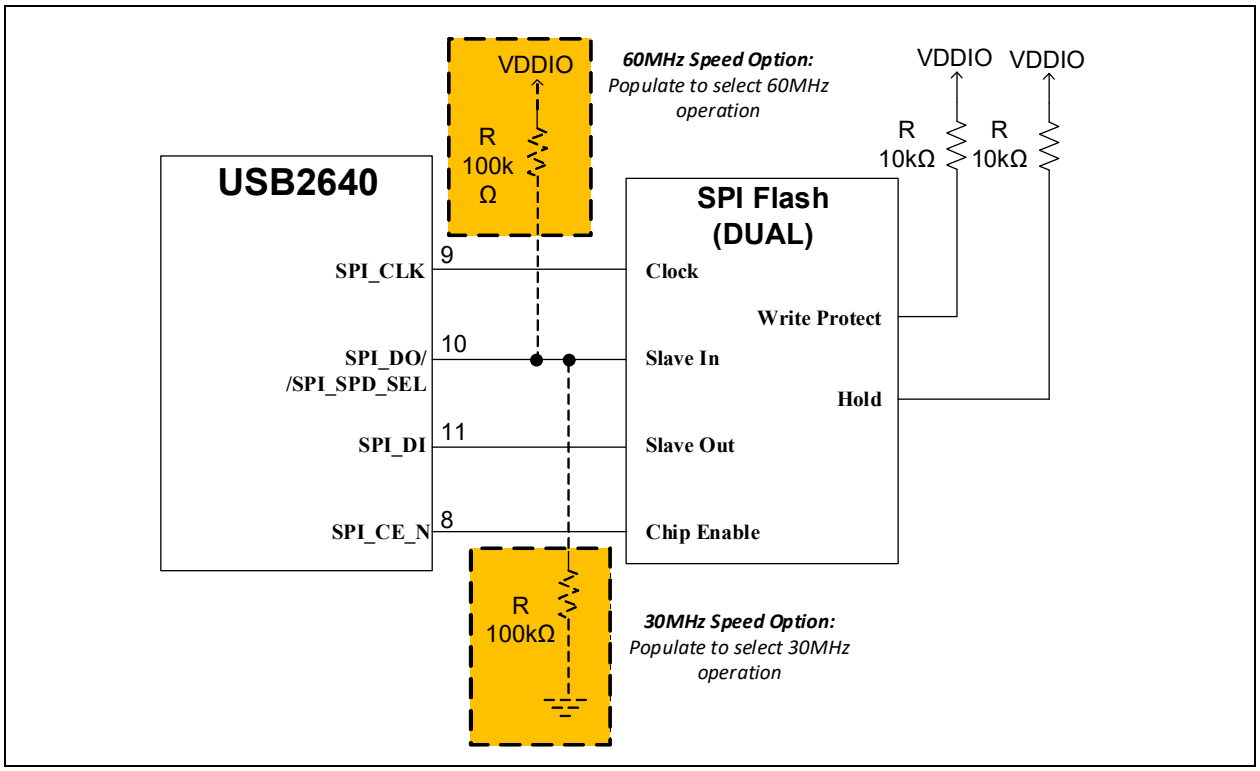
By default, the USB2640 executes firmware from an internal read only memory (ROM). The USB2640 supports optional firmware execution from an external SPI Flash device. An SPI Flash is only required if a custom firmware is required for the application.

The following are the key operational parameters:

- The SPI interface can operate at 60 MHz or 30 MHz. The speed is selected by the **SPI_SPD_SEL** hardware configuration strap.
- The SPI interface can operate in One-bit or Two-bit mode.
- Mode 0 or Mode 3 SPI Flash memory devices are supported.
- Generally, a 256 kB or larger memory size is required, but the final size is determined by the size of the custom firmware image after all customizations are implemented.

If an external SPI Flash device is used, the recommended schematic connections are shown in Figure 8-2.

FIGURE 8-2: DUAL SPI FLASH CONNECTIONS



8.3 Non-Removable Port Settings

In a typical USB2640 application, downstream ports are routed to a user-accessible USB connector and, hence, the downstream port should be configured as a removable port. By default, all downstream ports are configured as removable ports. If modifying the default settings to reconfigure a port as non-removable, configuration must be handled through either external EEPROM or SPI Flash.

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is **removable**.
- If the port is routed to a permanently attached and embedded USB device on the same PCB, or non user-accessible wiring or cable harness, it is **non-removable**.

Note:	The removable/non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host may use to understand if a port is a user-accessible port or if the device is a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs which must undergo USB compliance testing and certification must ensure the configuration settings are correct.

8.4 Self-Powered/Bus-Powered Settings

In a typical USB2640 application, the hub should be configured as self-powered, which is the default configuration setting. If modifying the default setting to bus-powered operation, configuration must be handled through either external EEPROM or SPI Flash.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the Upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is **bus-powered**.

- If the entire system (hub included) is always powered by a separate power connector, then the hub system is **self-powered**.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely **self-powered** (even if all of the power is derived from the upstream USB connector's VBUS pin).

Note:	The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub, and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device which connects to a self-powered hub which declares it needs more than 100 mA will be prevented from operating by the USB host.

NOTES:

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	The grounds are tied together.		
	Section 2.4, "USB-IF Compliant USB Connector"	USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"		The **VDD33** and **VDDA33** are within the range of 3.0V to 3.6V. 0.1 µF capacitors are connected to each power pin as close as possible, along with a 1.0 µF shared capacitor.		
		Ensure **VDDA33** (pin 48) has a 4.7 µF capacitor to GND.		
		Ensure **VDD33** (pin 16) has a 4.7 µF capacitor to GND.		
		Ensure **VDD18** (pin 15) and **VDDA18** (pin 46) each have a 1.0 µF capacitor to GND.		
		Ensure **VREG_EN** is floating unless **VDD18** is being sourced from an external regulator.		
Section 4.0, "USB Signals"	Section 4.1, "Upstream USB Interface"	The USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
		The **VBUS_DET** is properly connected, and the voltage is divided from nominal 5V VBUS to the 3.3V logic level the hub requires.		
	Section 4.2, "Downstream USB Ports"	Verify that the downstream port USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
		If the downstream ports are standard Type-A ports, verify that **PRT_CTLx** is properly connected to both the Enable pin of the downstream port power controller and the FAULT indicator output of the port power controller.		
		If the downstream ports are standard Type-C ports, verify that **PRT_CTLx** is properly connected to both the Enable pin of the downstream port power controller and the FAULT indicator output of the port power controller.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 4.3, "USB Protection"	The ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance, the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
	Section 4.4, "GND and SHIELD Recommendations"	The USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed in between the **SHIELD** pins and PCB ground.		
Section 5.0, "Card Reader Interface"	Section 5.1, "Secure Digital/Multi-MediaCard Slot"	All connections to a standard SD/MMC card slot, embedded eMMC memory, or microSD card slot are correct. Follow the diagrams in Figure 5-1, Figure 5-2, or Figure 5-4.		
	Section 5.2, "xD-Picture CardTM Slot"	Check connections to the standard xD-Picture Card slot and follow the diagram in Figure 5-4.		
	Section 5.3, "Card Power Switch"	The **CRD_PWR** either connects directly to the card media or card media slot supply power, or **CRD_PWR** enables an external supply switch if the internal card power switch is not used directly.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	The crystal or clock is 24.000 MHz (±350 ppm).		
		If a single-ended lock is used, it is connected to **XTAL1** while leaving **XTAL2** floating.		
		If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	A 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	The board power supplies deliver 3.0V to 3.6V to the hub power rails, and the power-on rise time meets the requirement of the hub as defined in the data sheet.		
		If the rise time requirement cannot be met, the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	The **RESET_N** signal has an external pull-up resistor or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Configuration Options"	Section 8.1, "External EEPROM"	If a EEPROM memory device is used, verify that the EEPROM is connected according to the diagram in Figure 8-1.		
	Section 8.2, "External SPI Flash memory"	Determine if a custom SPI FW image is required and which mode of operation the selected SPI Flash device must support. If a SPI Flash memory device is used, verify that the SPI Flash is connected according to the diagram in Figure 8-2.		
	Section 8.3, "Non-Removable Port Settings"	Verify the application requirements for removable and non-removable USB downstream ports.		
		If any port must be configured as non-removable, then the hub must be configured via EEPROM or SPI Flash.		
	Section 8.4, "Self-Powered/Bus-Powered Settings"	Refer to this section for application requirements for self-powered or bus-powered operation. If self-powered operation is required, then no additional configuration or circuitry is required. If bus-powered operation is required, then the hub must be configured via EEPROM or SPI Flash.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004545A (05-20-22)	Initial release	

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