PIC18F04/05/14/15Q41 Silicon Errata and Data Sheet Clarifications

PIC18F04/05/14/15Q41

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Introduction

The PIC18F04/05/14/15Q41 devices that you have received conform functionally to the current device data sheet (DS40002242**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F04/05/14/15Q41 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID				
		A4	A5	D1	D3	E0
PIC18F04Q41	0x7540	0xA004	0xA005	0xA0C1	0xA0C3	0xA0D0
PIC18F05Q41	0x7500	0xA004	0xA005	0xA0C1	0xA0C3	0xA0D0
PIC18F14Q41	0x7520	0xA004	0xA005	0xA0C1	0xA0C3	0xA0D0
PIC18F15Q41	0x75E0	0xA004	0xA005	0xA0C1	0xA0C3	0xA0D0

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q41 Family Programming Specification"** (DS40002143) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				A4	A5	D1	D3	E0
Analog-to-Digital Converter with Computation	ADCC	1.1.1	ADC cannot operate in certain low-power conditions	X				
		1.1.2	Double Sample Conversions	X	X	X	X	
Electrical Specifications	ADC Offset Error	1.2.1	ADC Offset Error specification lowered in ECH, ECM and ECL modes			X		
Oscillator	XT mode	1.3.1	Maximum clock frequency limited to 2 MHz for XT mode	X				
	Fail-Safe Clock Monitor	1.3.2	Enabling the FOSC Fail-Safe Clock Monitor alongside the Primary or Secondary Oscillator Clock Monitor causes issues in Sleep	X				
	EC mode	1.3.3	Maximum clock frequency for EC mode is 32 MHz for V_{DD} < 2.0V	X				
I^2C	I^2C	1.4.1	I2CxADR0/1/2/3 registers have incorrect Reset value	X				
		1.4.2	I^2C Start and/or Stop Flags may be set when I^2C is enabled	X	X	X		
		1.4.3	MDR bit is not cleared after bus time-out	X	X	X	X	X
		1.4.4	Bus time-out not detected properly when External Host Clock stretches	X	X	X	X	X
		1.4.5	Clock Stretch Disable not working properly	X	X	X	X	X
		1.4.6	Bus time-out causes false Start/Stop	X	X	X	X	X
Operational Amplifier	OPA	1.5.1	Charge Pump On Control (CPON) bit is reserved	X				
		1.5.2	Internal resistor ladder does not disconnect in Unity Gain mode	X				
Universal Asynchronous Receiver Transmitter	UART	1.6.1	UART TXDE signal may go low before the STOP bit has been entirely transmitted	X	X	X	X	
		1.6.2	Asynchronous 9-bit UART Address mode address mismatch	X	X	X	X	
Signal Measurement Timer	SMT	1.7.1	Reset Bit	X	X	X	X	
PIC18 CPU	FSR Shadow Registers	1.8.1	FSR Shadow Registers are not writable	X	X	X	X	
ICSP™	Low-Voltage Programming (LVP)	1.9.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X		
Instruction Set	`PUSHL` Instruction	1.10.1	The `PUSHL` instruction incorrectly executes	X	X	X	X	X
Note: Only those issues indicated in the last column apply to the current silicon revision.								

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 ADC Cannot Operate in Certain Low-Power Conditions

The ADC will not function when all of the following conditions exist: When the MCU system clock is sourced from LFINTOSC or SOSC and when both the BOR and FVR features are disabled.

Work around

- Method 1: Use a system clock other than LFINTOSC or SOSC.
- Method 2: Enable the BOR feature.
- Method 3: Enable the FVR feature.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.1.2 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = `1`) with no precharge time (ADPRE = `0`) and no Acquisition time (ADACQ = `0`), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1:

Disable Double Sample Conversion (DSEN = `0`) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no precharge time along with the desired Acquisition time.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	

1.2 Module: Electrical Specifications

1.2.1 ADC Offset Error Specification Lowered in ECH, ECM and ECL Modes

When operating the device using an external clock source as the system clock in ECH, ECM or ECL mode, the ADC Offset Error (AD04: E_{OFF}) is updated to 12 Least Significant bits.

Work around

To meet the specified ADC Offset Error limit of 6 Least Significant bits, do not operate the device using the system clock in ECH, ECM or ECL mode when using the ADC.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
		X		

1.3 Module: Oscillator (OSC)

1.3.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.3.2 Enabling the FOSC Fail-Safe Clock Monitor Alongside the Primary or Secondary Oscillator Clock Monitor Causes Issues with Sleep

When the FOSC Fail-Safe Clock Monitor is enabled (FCMEN Configuration bit = `1`) and either the Primary or Secondary Fail-Safe Clock Monitor is also enabled (FCMENS and/or FCMENP = `1`), putting the device to Sleep will cause a Fail-Safe condition to trigger. This has the effect of erroneously triggering Fail-Safe interrupts when there has not been a clock interruption. This can also cause the Watchdog Timer to not properly wake up the part from Sleep.

Work around

If proper functionality in Sleep is required, do not enable the Primary or Secondary Fail-Safe Clock Monitor while the FOSC Fail-Safe Clock Monitor is enabled. If Primary or Secondary Clock Monitoring in Sleep is desired, disable the FOSC Fail-Safe Clock Monitor before the device goes to Sleep.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.3.3 Maximum Clock Frequency for EC Mode Is 32 MHz for V_{DD} < 2.0V

When configured in External Clock High-Power (ECH) mode and operating at V_{DD} < 2.0V, the maximum input clock frequency is 32 MHz.

Work around

To obtain a system clock frequency of 64 MHz in ECH mode at V_{DD} < 2.0V, use a 16 MHz external clock in conjunction with the 4x Phase-Locked Loop (PLL) circuit (i.e., either RSTOSC Configuration bits = `0b010` or OSCCON1bits.NOSC = `0b010`).

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.4 Module: Inter-Integrated Circuit (I^2C)

1.4.1 The I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/2 registers reset to `0xFF` when the I2CxMD is enabled instead of `0x00`. The I2CxADR1/3 registers reset to `0xFE` when the I2CxMD is enabled instead of `0x00`.

Work around

None.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.4.2 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles (F_{OSC}/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (Fosc/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X		

1.4.3 MDR Bit Is Not Cleared after Bus Time-Out

In the Host mode of the I^2C module, when a bus time-out occurs during clock stretching and TOREC = `1`, the MDR bit will not be cleared and a Stop will not be transmitted on the bus.

Work around

Force a Stop on the bus by setting the P bit upon bus time-out in Host mode. Forcing a Stop on the bus clears the MDR bit.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	**X**

1.4.4 Bus Time-Out Not Detected Properly When External Host Clock Stretches

When the module is operating in Client mode and an external Host device is clock stretching after the 8th SCL clock and a bus time-out occurs, the bus time-out is not detected properly. When the external Host times out before the Client and releases SCL to generate a Stop condition, the module continues to stretch SDA as if to generate an ACK and hangs the bus, and a Stop is never seen on the bus.

Work around

Reset the module by toggling the EN bit.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	**X**

1.4.5 Clock Stretch Disable Not Working Properly

When the CSD bit is set between a Start condition and the 8th falling SCL edge, the I^{2}C module enters a state where the module clock stretches indefinitely after the next Start until a bus time-out occurs.

Work around

Force a reset of the module by toggling the EN bit.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	**X**

1.4.6 Bus Time-Out Causes False Start/Stop

When the module is operating in Client mode and an external Host device is clock stretching, and a bus time-out occurs in the Client, the Client releases SDA and goes into the idle state. After the external Host generates a Stop condition on the bus by releasing SCL, the module can erroneously drive a low pulse on the SDA line, which acts as a false Start and Stop on the bus.

Work around

None.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	**X**

1.5 Module: Operational Amplifier

1.5.1 The Charge Pump On Control (CPON) Bit Is Reserved

When not operating the OPA near the rails, the Charge Pump On Control (CPON) bit can be used to disable the charge pump in order to save on current consumption. This feature is currently not available, and the charge pump is always enabled whenever the OPA module is in operation.

Work around

None.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.5.2 Internal Resistor Ladder Does Not Disconnect in Unity Gain Mode

When using the OPA module in a unity gain configuration, the internal resistor ladder will not automatically disconnect from the operational amplifier, which may adversely affect the gain of the circuit. This applies when the peripheral has been configured to operate in Unity Gain mode in software by setting the UG bit, or in hardware using the hardware controlled override feature.

Work around

Disconnect the internal resistor ladder from the operational amplifier by writing to the Inverting Input Channel Selection (NCH) bits. All signals can be disconnected from the operational amplifier by writing `0b000` to the NCH bits.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X				

1.6 Module: Universal Asynchronous Receiver Transmitter (UART)

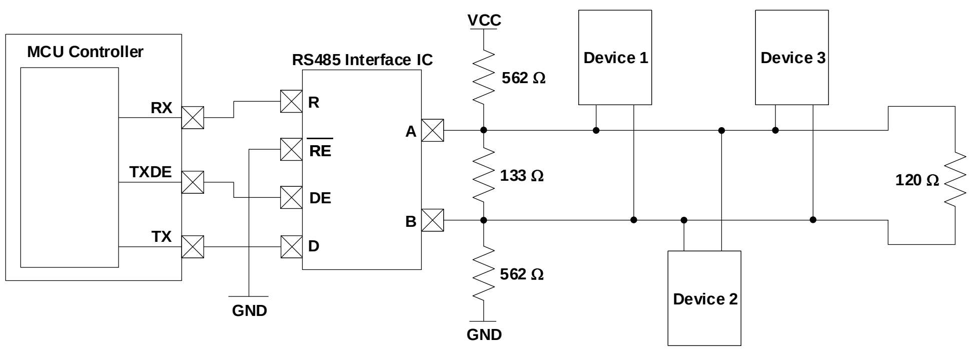
1.6.1 UART TXDE Signal May Go Low Before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE signal going low before the STOP bit has had enough time to settle.

Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	

1.6.2 Asynchronous 9-bit UART Address Mode Address Mismatch

In Asynchronous 9-bit UART Address mode, there is the possibility that a false address mismatch may occur even when the address of both devices match, or that a false address match may occur when there is an address mismatch between the devices.

Work around

None. Do not use the UART modules in Asynchronous 9-bit Address Mode.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	

1.7 Module: Signal Measurement Timer (SMT)

1.7.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work around

Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	

1.8 Module: PIC18 Core

1.8.1 FSR Shadow Registers Are Not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below).
3. Write the shadow FSRxL (data doesn't matter); this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0]).
5. Write FSRxH.
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	

1.9 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.9.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X		

1.10 Module: Instruction Set

1.10.1 The `PUSHL` Instruction Incorrectly Executes

The `PUSHL` instruction of the PIC18 Extended Instruction Set incorrectly executes when FSR2 is loaded with certain values.

Work around

Do not use `PUSHL` when FSR2 is loaded with any of the following values:

- 0xDB
- 0xDC
- 0xDE
- 0xE3
- 0xE4
- 0xE6
- 0xEB
- 0xEC
- 0xEE

Affected Silicon Revisions

A4	A5	D1	D3	**E0**
X	X	X	X	**X**

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002242**F**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Interrupt Vector Priority Table

Table 11-2 incorrectly states the vector numbers for CWG1, NCO1, DMA2SCNT, DMA2DCNT, DMA2OR, and DMA2A. The corrected values are shown below with changes highlighted in **bold**:

Table 2-1. Interrupt Vector Priority Table

Vector Number	Interrupt source	Vector Number (cont.)	Interrupt source (cont.)
0x0	Software Interrupt	0x2D	CLC2
0x1	HLVD (High/Low-Voltage Detect)	0x2E	PWM2PR
0x2	OSF (Oscillator Fail)	0x2F	PWM2
0x3	CSW (Clock Switching)	0x30	INT1
0x4	NVM	**0x31**	**-**
0x5	CLC1 (Configurable Logic Cell)	**0x32**	**CWG1 (Complementary Waveform Generator)**
0x6	CRC (Cyclic Redundancy Check)	**0x33**	**NCO1 (Numerically Controlled Oscillator)**
0x7	IOC (Interrupt-On-Change)	**0x34**	**DMA2SCNT**
0x8	INT0	**0x35**	**DMA2DCNT**
0x9	ZCD (Zero-Cross Detection)	**0x36**	**DMA2OR**
0xA	AD (ADC Conversion Complete)	**0x37**	**DMA2A**
0xB	ACT (Active Clock Tuning)	0x38	I2C1RX
0xC	CM1 (Comparator)	0x39	I2C1TX
0xD	SMT1 (Signal Measurement Timer)	0x3A	I2C1
0xE	-	0x3B	I2C1E
0xF	SMT1PWA	0x3C	-
0x10	ADT	0x3D	CLC3
0x11 - 0x13	-	0x3E	PWM3PR
0x14	DMA1SCNT (Direct Memory Access)	0x3F	PWM3
0x15	DMA1DCNT	0x40	U2RX
0x16	DMA1OR	0x41	U2TX
0x17	DMA1A	0x42	U2E
0x18	SPI1RX (Serial Peripheral Interface)	0x43	U2
0x19	SPI1TX	0x44	-
0x1A	SPI1	0x45	CLC4
0x1B	TMR2	0x46	-
0x1C	TMR1	0x47	SCAN
0x1D	TMR1G	0x48	U3RX
0x1E	CCP1 (Capture/Compare/PWM)	0x49	U3TX
0x1F	TMR0	0x4A	U3E
0x20	U1RX	0x4B	U3
0x21	U1TX	0x4C	DMA3SCNT
0x22	U1E	0x4D	DMA3DCNT
0x23	U1	0x4E	DMA3OR
0x24	TMR3	0x4F	DMA3A
0x25	TMR3G	0x50	INT2
0x26	PWM1PR	0x51	-
0x27	PWM1	0x52	-

Table 2-1. Interrupt Vector Priority Table (continued)

Vector Number	Interrupt source	Vector Number (cont.)	Interrupt source (cont.)
0x28	SPI2RX	0x53	TMR4
0x29	SPI2TX	0x54	DMA4SCNT
0x2A	SPI2	0x55	DMA4DCNT
0x2B	-	0x56	DMA4OR
0x2C	CM2 (Comparator)	0x57	DMA4A

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
H	03/2025	Added silicon errata issue 1.10.1; added DS Clarifications 2.1; updated DS revision letter.
G	06/2023	Added silicon revision E0. Added silicon errata 1.4.3, 1.4.4, 1.4.5 and 1.9.1.
F	05/2022	Added silicon revision D3.
E	04/2022	Updated the flash memory cell endurance specification data sheet clarification. Added silicon errata 1.8.1.
D	02/2022	Added silicon errata 1.1.2, 1.6.1 and 1.7.1.
C	02/2021	Added ADC offset errata and updated mask revision for KV00P RTP. Added silicon revision D1. Added silicon errata 1.5 and 1.6. Minor editorial corrections.
B	11/2020	Added silicon revision A5.
A	07/2020	Initial document release.

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