SY88149CL Evaluation Board

3.3V, 1.25Gbps PECL Limiting Post Amplifier with High-Sensitivity TTL SD

General Description

The SY88149CL evaluation board enables fast and thorough evaluation of the SY88149CL. The board is an easy-to-use, single supply design, designed to be driven by a high-speed, pattern generator. The input termination network also provides the required input bias of V_{CC}-1.3V for the SY88149CL. The SY88149CL evaluation board is intended to terminate to a 50Ω scope and provides for simple user adjustability of the SD threshold through the adjustment of an on-board potentiometer.

All data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

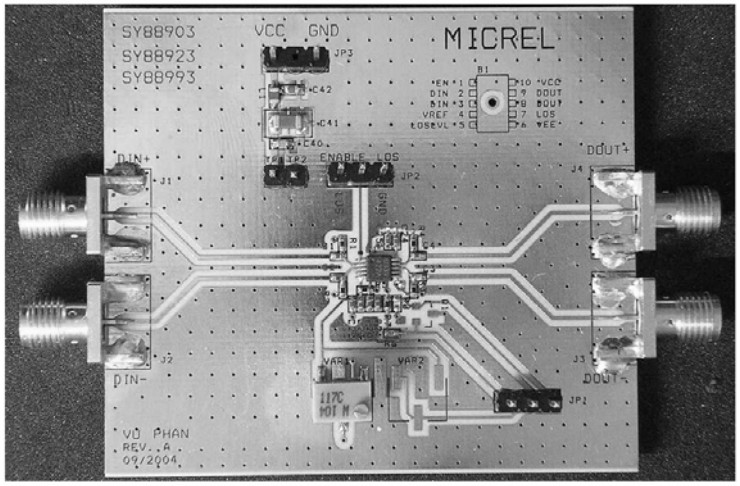
Features

- SY88149CL PECL Limiting Post Amplifier with High-Sensitivity TTL SD
- Single +3.3V power supply
- AC-coupled configuration for direct interface with 50Ω test equipment
- On-board SD sensitivity adjustment

Related Documentation

3.3V, 1.25Gbps PECL Limiting Post Amplifier with High-SensitivityTTL

Evaluation Board



Evaluation Board Description

The SY88149CL evaluation board is designed to operate with a single 3.3V ±10% power supply and is configured with AC-coupled inputs and outputs. The high-speed input and output channels are brought out to SMA connectors through matched length AC-coupled differential strip-line traces.

AC-Coupled Input

The AC-Coupled inputs automatically bias the input levels to the correct DC-operating point set by the VT jumper input. Therefore, the inputs can be driven by a differential signal smaller than 100mV ($200mV_{pp}$) without level shifting or termination resistor network in the signal path.

AC-Coupled Output

The SY88149CL is configured with AC-coupled outputs allowing the board to interface directly with 50Ω equipment. AC-coupling allows the board to use a single power supply. If only one output is being used, the unused complimentary output should be terminated into 50Ω to ground.

SY88149CL AC-Coupled Evaluation Board Setup

This section explains how to connect and setup the SY88149CL evaluation board per Figure 1. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY88149CL evaluation board.

Measurements

Evaluating DOUT & /DOUT

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to V_{CC} post and the negative lead to GND post.
2. Set the desired frequency on a pattern generator with an amplitude between $5mV_{PP}$ and $1800mV_{PP}$. Typical data patterns are 2^7-1 or 2^{23}-1 PRBS patterns depending on the application. Since the inputs to the board are AC-Coupled, the voltage offset of the pattern generator is not significant so it can be set between GND and VCC.
3. Connect the pattern generator with differential outputs as a data source to the DIN and /DIN inputs on the SY88149CL evaluation board. Use matched length differential cables.
4. Turn the power supply on.
5. Observe the DOUT and /DOUT outputs with a 50Ω scope. The output rise and fall times should be less than 260ps, with an amplitude around 800mV ($1600mV_{p-p}$ differential).

SD Hysteresis Measurements

The SY88149CL evaluation board provides a potentiometer to allow for convenient adjustment of SD_{LVL} without the need for an extra power supply. SD_{LVL} taps off a potentiometer connected between V_{CC} and V_{REF}. V_{REF} is a reference voltage of approximately V_{CC} - 1.3V. Hence, SDLVL can be set to any voltage between V_{CC} and V_{CC} -1.3, as specified in the SY88149CL data sheet. The potentiometer creates a voltage divider. Thus,

$$SD_{LVL} = V_{CC} - \left[\frac{1.3 \times R(k\Omega)}{(R(k\Omega) + 2.8k\Omega)}\right]$$

Where R is the resistance of the potentiometer from V_{CC} to the tap at SDLVL. The steps below show how to measure the SD hysteresis as a function of the input voltage swing at the DIN and /DIN inputs:

Minimum input swing hysteresis measurement

The minimum acceptable input swing for the SY88149CL is $5mV_{PP}$.

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to V_{CC} post and the negative lead to GND post.
2. Connect a DMM or similar voltage measurement device between the SD_{LVL} pin and V_{CC}.
3. Connect a second DMM or similar voltage measurement device between the SD output and GND. For the remainder of this document this DMM will be referred to as the SD DMM.
4. Connect the pattern generator with differential outputs as a data source to the DIN and /DIN inputs on the SY88149CL evaluation board. Use matched length differential cables.
5. Turn the power supply on.
6. Adjust the trimpot VAR1 so the voltage at the SD_{LVL} pin is around 1.3V below V_{CC}. This sets the SD for maximum sensitivity. At this level the SD output should go HIGH or LOW (measured with the SD DMM set up in step 4) as the input voltage swing at DIN and /DIN is varied around $5mV_{PP}$.
7. Now adjust the trimpot is to vary the voltage so it is closer to V_{CC}. Note that as the voltage at the SD_{LVL} pin approaches V_{CC} a larger input voltage swing is required to trigger the assert and deassert levels, while as the SD_{LVL} voltage moves away from V_{CC} the assert and deassert levels are triggered by input voltage swings as small as $5mV_{PP}$.
8. The hysteresis between the assert and deassert levels can be calculated with the following equation: Hysteresis(dB) =20log(SD Assert voltage/SD de-assert voltage). This hysteresis should be >2dB.

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Evaluation Board Layout

The evaluation boards are constructed with Rogers 4003 material and are coplanar in design fabricated to minimize noise, achieve high bandwidth and minimize crosstalk.

L1	GND and Signal
L2	GND
L3	VCC
L4	GND

Table 1. Layer Stack

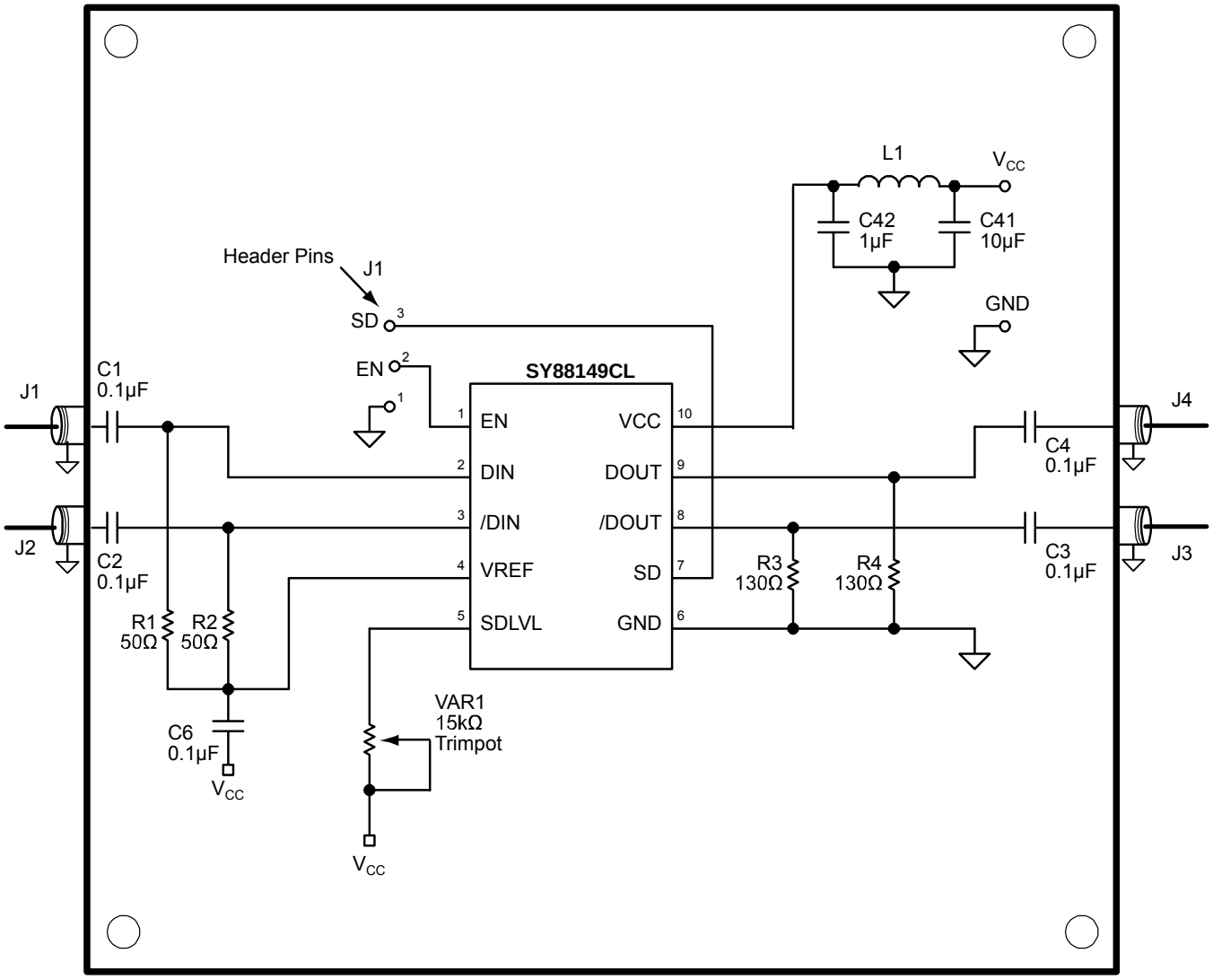

Figure 1. Setup for Measurement

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Bill of Materials (SOIC)

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4, C21, C23, C25	VJ0402Y104KXXAT	Vishay[1]	0.1μF, 25V, 10% Ceramic Capacitor, Size 0402, X5R, Dielectric	7
C20, C22, C24	VJ0402Y222KXXAT	Vishay[1]	220pF, 25V, 10% Ceramic Capacitor, Size 0402, X5R, Dielectric	3
C40	VJ0603Y104KXXAT	Vishay[1]	0.1μF, 25V, 10% Ceramic Capacitor, Size 0603, X5R, Dielectric	1
C41	293D106X0025CT	Vishay[1]	10μF, Surface Mount Capacitor, Size C	1
C42	293D105X0025CT	Vishay[1]	1μF, Surface Mount Capacitor, Size C	1
L1	BLM21A102F	Murata[2]	Ferrite Bead, Size 0603	1
JP1, JP2, JP3	TSW-103-07-S-S	Samtec[3]	0.1mil Center through hole terminal strip	3
R1, R2	CRCW040249R9F	Vishay[1]	49.9Ω, 10%, 1/16W Resistor SMD, Size 0402	2
R3, R4	CRCW04021300F	Vishay[1]	130Ω, 10%, 1/16W Resistor SMD, Size 0402	2
R5	CRCW04023001F	Vishay[1]	3kΩ, 10%, 1/16W Resistor SMD, Size 0402	1
R7	CRCW04025001F	Vishay[1]	5kΩ, 10%, 1/16W Resistor SMD, Size 0402	1
VAR1	3269W-1-153G	Bourns[4]	15kΩ Trimpot	1
J1–J4	142-0701-851	Johnson Components[5]	Jack Assembly End Launch SMA	4
U1	**SY88149CL**	**Micrel, Inc.[6]**	**Post Amplifier**	1

Notes:

1. VIshay: www.vishay.com.
2. Murata: www.murata.com.
3. Samtec: www.samtec.com.
4. Bourns: www.bourns.com.
5. Johnson Components: www.johnsoncomponents.com.
6. **Micrel, Inc.: www.micrel.com.**

Micrel Cross Reference

To find an equivalent Micrel part, go to Micrel's website at: http://www.micrel.com and follow the steps below:

1. Click on Dynamic Cross Reference.
2. Enter competitor's part number in the Dynamic Cross Reference field.
3. To download a PDF version of this information, click on the Cross Reference PDF tab.

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