

Off-Line 5.0V Output Non-Isolated Linear Regulator

Introduction

There are many applications that call for a non-isolated, low current DC power supply operating directly from the AC line. A switchmode power supply would be far too complex and expensive, whereas a simple 60Hz step down transformer would be cost effective but physically too large. Examples of such applications include battery chargers, proximity switches, television stand-by supplies, and internal supplies for switchmode power supplies. When line isolation is not necessary, the circuit presented in this application note provides a solution that is both very cost effective and compact.

The circuit presented in this note is a two-stage linear regulator capable of providing 5.0V at 50mA, but can be easily modified for other output voltages. The first stage handles the majority of voltage drop and power dissipation, allowing the second stage to employ standard low-voltage, low-power linear IC regulators. The Supertex DN2535N5 high voltage depletion-mode MOSFET is used as the first stage pass transistor.

For an isolated output, or an output with significantly higher output currents, please refer to Supertex application notes AN-H13, AN-H21, AN-H22, AN-H23, and AN-H24 which discuss the Supertex HV91XX series of switchmode PWM controller ICs.

Circuit Description

The circuit of Figure 1 provides a regulated 5.0V output at 50mA directly from a 120VAC input. Detailed descriptions will be given for the three different sections: Input rectifier, pre-regulator, and output regulator. SPICE simulation, lab measurements, and power dissipation are also addressed.

Caution

The circuit described in this application note does NOT provide galvanic isolation. When operated from an AC line, potentially lethal voltages can be present within the circuit. Adequate means of protecting the end user from such voltages must be provided by the circuit developer.

Design Requirements

The circuit in Figure 1 was developed to meet the design requirements listed in the table below. Many other output voltages and currents can be achieved simply by changing component values, without requiring any alterations in circuit topology.

Input	Output
120VAC	5.0VDC $\pm 4\%$
	0 to 50mA
	50mV _{P-P} ripple voltage

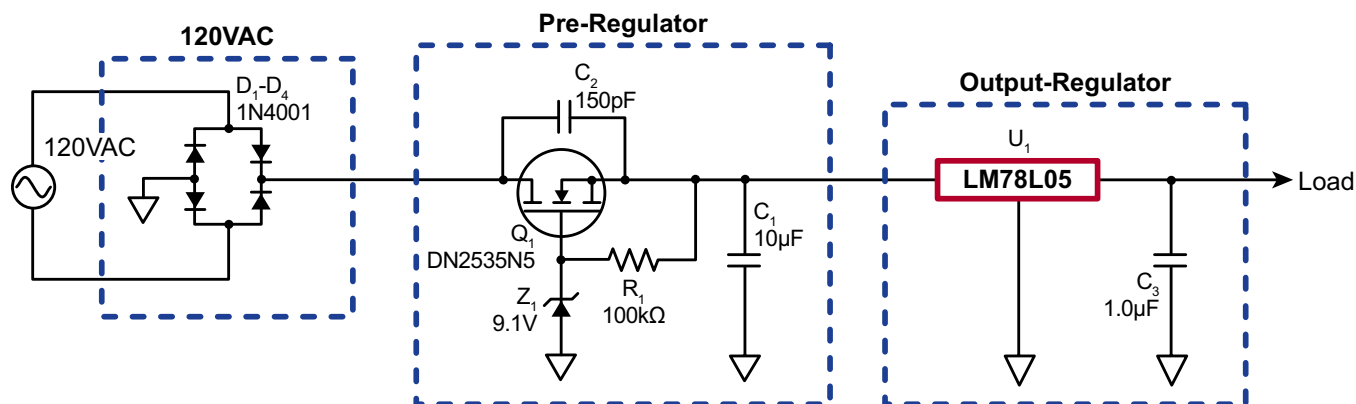


Figure 1: 5V @ 50mA Non-Isolated Power Supply

Circuit Description

Component	Function	Notes	Value	Rating
D1-D4	Rectifies AC line current	-	1N4004 (120VAC) 1N4005 (240VAC)	200V (120 VAC) 350V (240VAC) 100mA
Q1	Preregulator pass transistor	Use appropriate heat sink	DN2535N5 (120VAC) DN2540N5 (240VAC)	350V (120VAC) 400V (240VAC) 150mA
Z1	Sets preregulator output voltage	Other zener voltages may be used for other output voltages	1N757 (9.1V)	1/10W
R1	Provides bias for Q1 and Z1	-	100kΩ	1/16W
C1	Stores energy for use when AC < 9.1V	-	10μF	15V
C2	Prevents high frequency oscillations	Locate close to Q1	150pF	200V (120VAC) 350V (240VAC)
U1	Provides output regulation	Other devices may be used for other output voltages	LM78L05 (5.0V)	50mA
C3	Reduces transients at output	-	1.0μF	10V (or greater than output voltage)

Section I: Input Rectifier

Figure 2 shows the line rectification circuit. Diodes D1 through D4 are selected to handle the maximum input voltage and load current. Recommended rectifiers are 1N4004's for 120V AC line or 1N4005's for 240V AC line.

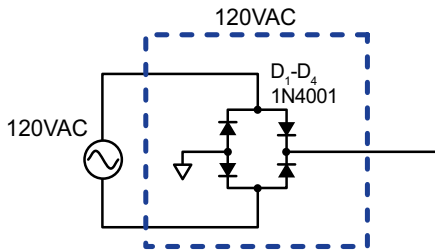


Figure 2: Input Rectifier

Power dissipation in the bridge rectifier is calculated to be:

$$P_{rect} = 2 \cdot (I_{LOAD} + I_{BIAS}) \cdot V_F$$

where:

I_{LOAD} = load current (50mA)

I_{BIAS} = bias current for Z₁ and U₁ (5.5mA)

V_F = rectifier forward voltage drop (0.7V)

This yields 78mW dissipation in the bridge rectifier.

Section II: Pre-Regulator

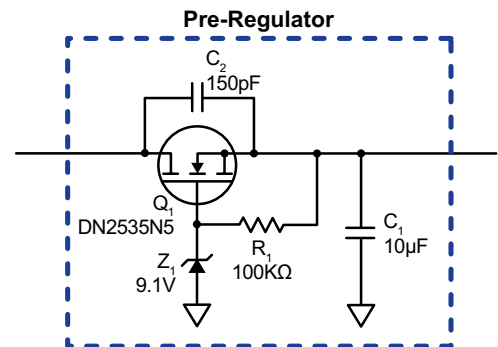


Figure 3: Pre-Regulator

Figure 3 shows the preregulator, providing high voltage input to low voltage output using the Supertex DN2535N5. The preregulator must supply an input voltage to the output regulator within a range as determined below:

$V_{SOURCE(MIN)}$ = minimum specified input voltage for the output regulator

$$V_{SOURCE(MAX)} = V_{OUT} + \frac{P_{REG(MAX)}}{I_{LOAD(MAX)}}$$

or maximum specified input voltage, whichever is less

where:

$V_{SOURCE(MAX)}$ = voltage at source of Q_1 = input voltage to output regulator

$I_{LOAD(MAX)}$ = maximum anticipated load current

$P_{reg(MAX)}$ = power dissipation rating for the output regulator

V_{OUT} = final output voltage

For the LM78L05, the minimum input voltage is specified as 7.0V. The maximum input voltage is specified as 30V. However, the 700mW@25°C power rating of the LM78L05 limits the maximum input voltage to 17.6V.

Q_1 acts as a source follower where the source voltage follows the gate voltage minus the gate-source voltage (V_{GS}):

$$V_{SOURCE} = V_{GATE} - V_{GS}$$

V_{GS} increases with increasing drain current, thus with a fixed gate voltage, the source voltage will drop with increasing load current. For design purposes, V_{GS} for the transistor under saturation and cut-off conditions (0V and $V_{GS(OFF)}$, respectively) can be used. These values can be readily obtained from the transistor data sheet. For the DN2535N5, $V_{GS(OFF)}$ can be a maximum of -3.5v.

Zener Z1 sets the gate voltage and should be selected to provide a source voltage within the range determined above, taking into account the variances of V_{GS} with load. A zener voltage of 9.1V will result in a source voltage of 9.1 to 12.6V under all load conditions.

Bias current for the Zener is determined by V_{GS}/R_2 . Using 100kΩ for R_2 , the bias current can vary between 0 and 35μA, although the actual bias current will be less than 35μA since the transistor is not operated at complete cut-off.

Storage capacitor C_1 must store enough energy to supply the load for periods when the rectified AC voltage is below 9.1 volts. The duration of this period is:

$$t_{OFF} = \frac{1}{\pi f} \arcsin \frac{(V_{Z1} - 1.4V)}{(V_{AC(PK)})}$$

where:

f = line frequency

V_{Z1} = Zener voltage

$V_{AC(PK)}$ = peak line voltage and the 1.4V accounts for rectifier drops

For the given circuit, this works out to be 241μS. The minimum value of C_1 given an allowable maximum voltage droop is:

$$C \geq t_{OFF} \cdot \frac{I_{LOAD} + I_{BIAS}}{V_{Z1} - V_{SOURCE(MIN)}}$$

where:

I_{LOAD} = load current

I_{BIAS} = bias current for Z1 and U1

V_{Z1} = zener voltage

$V_{SOURCE(MIN)}$ = minimum input voltage for U1

This works out to 6.4μF. The next highest standard value, 10μF, was selected.

Q_1 must recharge C_1 immediately after the rectified AC again rises above 9.1V. For this reason, the transistor's saturation current (I_{DSS}) must be greater than the load and bias currents. The DN2535N5's I_{DSS} is 150mA minimum, providing more than enough current to recharge C_1 .

The power dissipation for Q_1 can be calculated from the voltage drop across it times the current through it:

$$P_{Q1} = (V_{DRAIN} - V_{SOURCE}) \cdot (I_{LOAD} + I_{BIAS})$$

V_{DRAIN} is the rectified 120VACrms line minus two diode drops (1.4V) for a drain voltage of approximately 118.6Vrms. V_{SOURCE} has been previously determined to be in the range of 9.1 to 12.6 volts. Therefore, the maximum voltage across Q_1 is about 109.5V. Current through Q_1 is the sum of the load current plus the bias currents for Z1 and U1, or 50mA + 5.5mA. This yields a power dissipation in Q_1 of about 6.1W. An adequate heat sink must be provided for Q_1 to dissipate this power. Power dissipation of the other components in the preregulator are insignificant.

Capacitor C_2 across the drain-source of Q_1 is needed to avoid possible high frequency oscillations due to parasitic inductances. A value of 150pF is sufficient.

Section III: Output Regulation

The output regulator consists of an LM78L05 linear regulator and C_3 . U_1 provides an output of $5.0V \pm 4\%$ at 50mA. C_3 serves to reduce output transients.

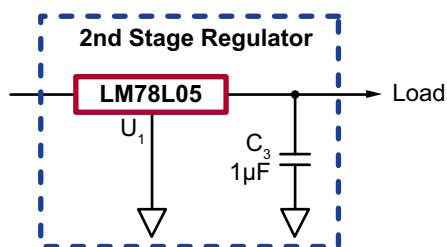


Figure 2: Input Rectifier

Power dissipation for the output regulator can be calculated as:

$$\begin{aligned}
 P_{U1} &= P_{BIAS} + P_{REG} \\
 &= (V_{IN} \times I_{BIAS}) + (V_{OUT} - V_{REG}) \times I_{OUT} \\
 &= 10V \times 5.5mA + (10V - 5V) \times 50mA \\
 &= 0.31W
 \end{aligned}$$

Measurements

The circuit of Figure 1 was constructed and measurements were taken. Overall, the circuit performed close to what simulations predicted. The preregulator output voltage is very close to simulation and calculations. Simulations predicted that V_{SOURCE} would drop 2.0V. Experimental results confirmed this.

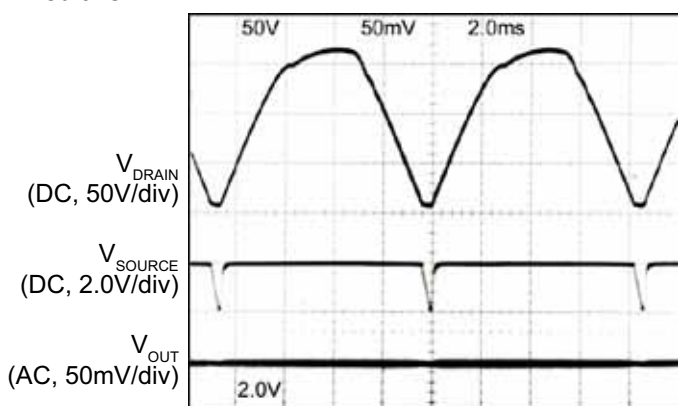


Figure 5: Experimental results showing V_{DRAIN} , V_{SOURCE} , and V_{OUT} (top to bottom).

The preregulator output voltage, for both simulation and actual results, are close to the design voltage of 10 volts.

The output regulator, LM78L05, provided a solid 5.0V output. Rejection of the 2.0V input ripple was excellent, showing no discernible output ripple. Experimental results showed about $20mV_{PP}$ of noise at the output.

240VAC Variation

A slight variation of this circuit is to power a 25mA load from a 240VAC line. Adjustment of the above circuit, replacing the 100Ω load resistor with a 200Ω and increasing the line voltage to 240VAC. Storage capacitor $C1$ may be halved since current has been halved. Overall power dissipation is about the same since the load current was halved and the line voltage doubled. The voltage rating of Q_1 could remain at 350V, since the peak voltage of a 240VAC line is 336V. However, this only provides a 4% safety margin which does not allow for variations in line voltage. The DN2540N5 with a 400V rating is recommended, providing a 19% safety margin. Recommended rectifiers for the bridge rectifier are 1N4005's.

Design Verification

Based on SPICE simulations, the circuit of Figure 1 should yield waveforms similar to those in Figure 6.

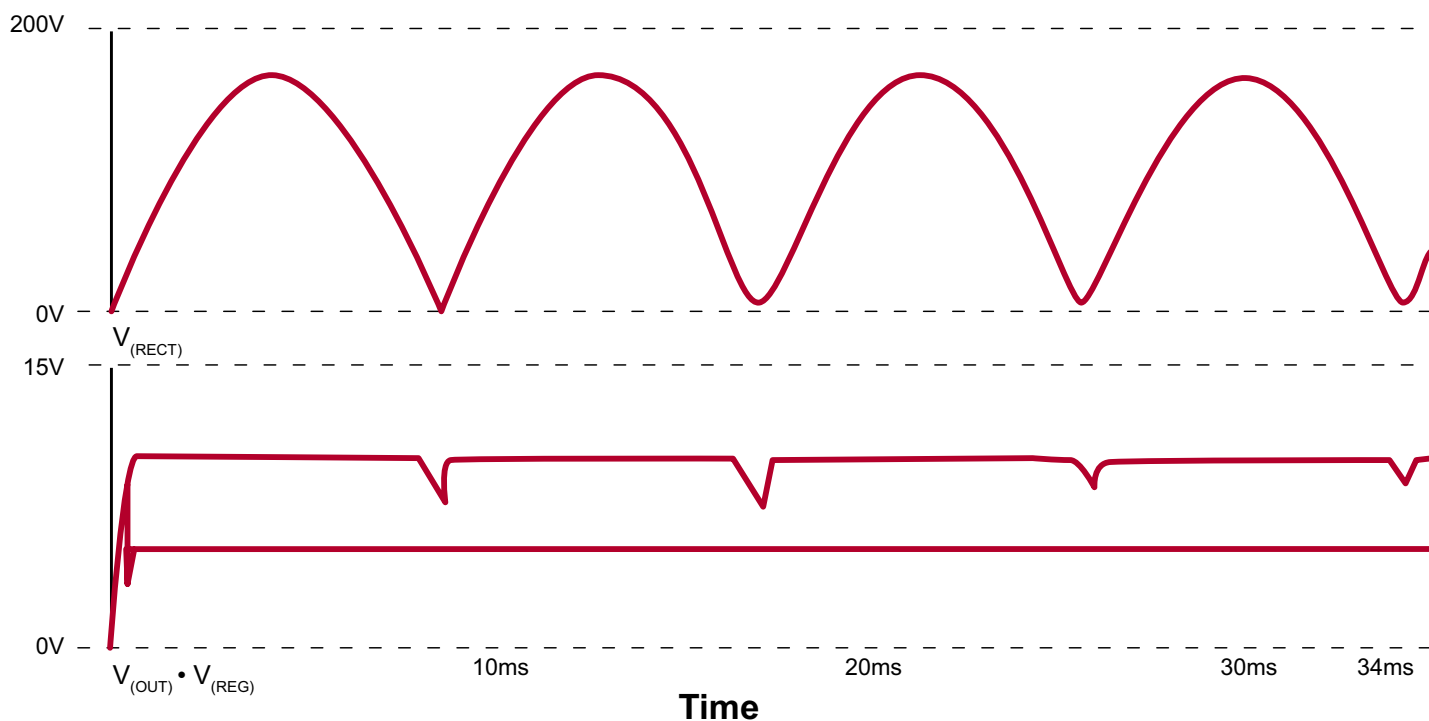


Figure 6: SPICE simulation results for 5.0V, 50mA load

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