

SST25VF016B/032B to SST26VF016B and SST26VF032B/032BA Migration

1.0 INTRODUCTION

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package. SST26VF016B and SST26VF032B/032BA also support full command-set compatibility to traditional Serial Peripheral Interface (SPI) protocol.

This document lists all the firmware and hardware changes required to migrate from SST25VF016B and SST25VF032B to SST26VF016B or SST26VF032B/032BA. Refer to the SST26VF016B data sheet (DS20005262) or SST26VF032B/032BA data sheet (DS20005218) for more information.

TABLE 1-1: SUMMARY OF CHANGES REQUIRED FOR ALL PART NUMBERS AND PACKAGES

Current Part	Recommended Upgrade	Board Layout/ Footprint Change	Firmware Change
SST25VF016B-75-4I-S2AF (8-lead SOIC)	SST26VF016B-104I/SM (8-lead SOIJ) ¹	No	Yes
SST25VF016B-75-4I-QAF (WSON)	SST26VF016B-104I/MF (WDFN) ²	No	Yes
Any SST25VF016B	SST26VF016B-104I/SN (8-lead SOIC) ³	Yes	Yes
SST25VF032B-75-4I-S2AF (8-lead SOIC)	SST26VF032B-104I/SM (8-lead SOIJ) ¹	No	Yes
SST25VF032B-75-4I-QAE (WSON)	SST26VF032B-104I/MF (WDFN) ²	No	Yes
Any SST26VF032B	SST26VF032B-104I/TD (TBGA) ⁴	Yes	Yes

1. SOIC and SOIJ are different designators for the same package.
2. WSON and WDFN are different designators for the same package.
3. 8-lead SOIC is a new 150 mil SOIC package available for SST26VF016B
4. TBGA is a new package available for SST26VF032B/032BA

**TABLE 1-2: PIN LAYOUT COMPARISON,
8-LEAD PACKAGES**

Pin No.	SST25VF016B/032B	SST26VF016B and SST26VF032B/032BA
1	CE#	CE#
2	SO	SO/SIO1
3	WP#	WP#/SIO2
4	VSS	VSS
5	SI	SI/SIO0
6	SCK	SCK
7	HOLD#	HOLD#/SIO3
8	VDD	VDD

SST25VF016B/032B TO SST26VF016B AND SST26VF032B/032BA

2.0 MIGRATION CONSIDERATIONS

The following topics should be considered when migrating from SST25VF016B and SST25VF032B to SST26VF016B and SST26VF032B/032BA.

2.1 Status and Configuration Register

The status registers of the SST25VF016B and SST25VF032B differ from the Status registers of SST26VF016B and SST26VF032B/032BA. See Tables 2-1 and 2-2. SST26VF016B and SST26VF032B/032BA also have additional Configuration registers used to configure device operations and setup defaults on I/O configuration and Block-Protection state, see Table 2-3.

TABLE 2-1: SOFTWARE STATUS REGISTER SST25VF016B/032B

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection	1	R/W
3	BP1	Indicate current level of block write protection	1	R/W
4	BP2	Indicate current level of block write protection	1	R/W
5	BP3	Indicate current level of block write protection	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

TABLE 2-2: STATUS REGISTER SST26VF016B AND SST26VF032B/032BA

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write-Enable Latch status 1 = Device is write-enabled 0 = Device is not write-enabled	0	R
2	WSE	Write Suspend-Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend-Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0	R
5	SEC ¹	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0 ¹	R
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

1. The Security ID status will always be '1' at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is '0'.

TABLE 2-3: CONFIGURATION REGISTER SST26VF016B AND SST26VF032B/032BA

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration for SPI Mode 1 = WP# and HOLD# pins disabled 0 = WP# and HOLD# pins enabled	0 ¹	R/W
2	RES	Reserved	0	R
3	BPNV	Block-Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RES	Reserved	0	R
7	WPEN	Write-Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0 ²	R/W

1. SST26VF016B/032B default at Power-up is '0'
SST26VF032BA default at Power-up is '1'
2. Factory default setting. This is a non-volatile bit; default at power-up will be the setting prior to power-down.

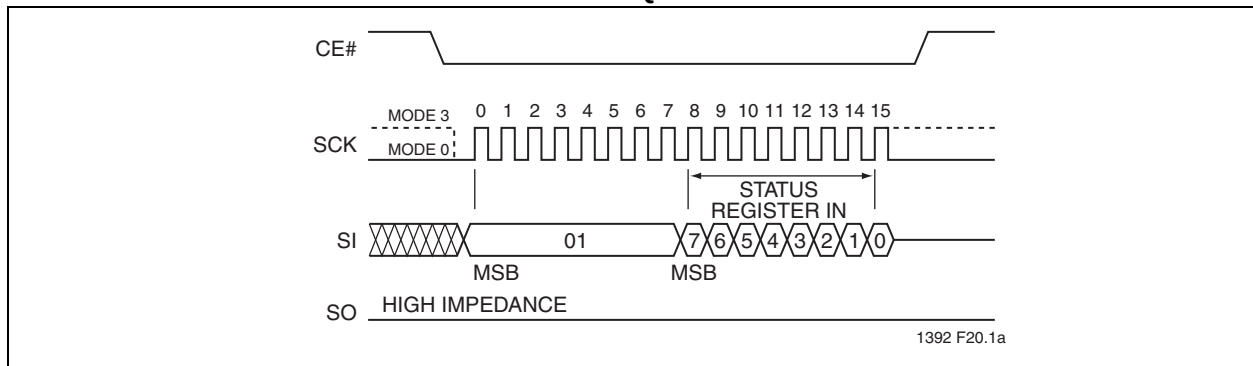
The Read-Status-Register (RDSR) instructions allow the devices to read the Status register for all parts. The Read-Configuration-Register (RDCR) commands enables the device to read the Configuration register of SST26VF016B and SST26VF032B/032BA.

The Write-Status-Register (WRSR) instruction writes to the Status and Configuration registers. Write-Enable (WREN) instruction must be issued prior to WRSR instruction. The WRSR sequence that allows the device to write to the Status register of SST25VF016B/032B is

shown in [Figure 2-1](#). The WRSR sequence that allows the device to write to the Status and Configuration registers of SST26VF016B and SST26VF032B/032BA is shown in [Figure 2-2](#)

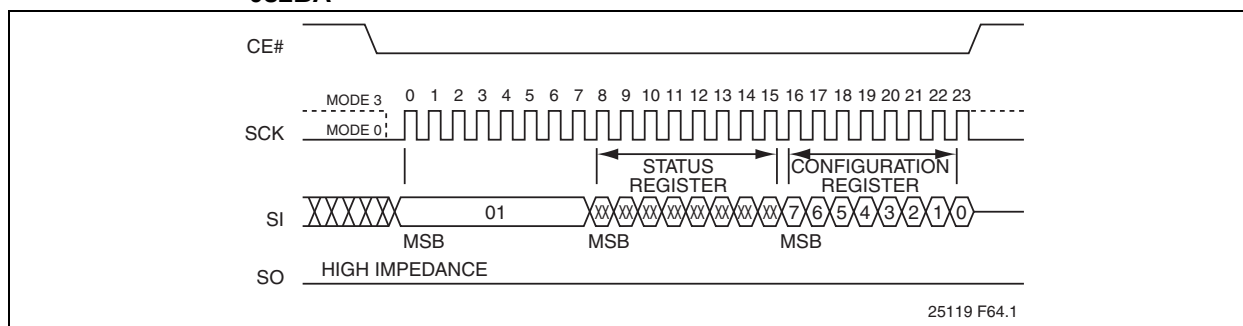
The default I/O state factory settings are the same between SST25VF016B/032B and SST26VF016B or SST26VF032B. The SST26VF032BA factory default settings for I/O WP# and HOLD# are disabled and different from the SST25VF016B/032B.

FIGURE 2-1: WRITE-STATUS-REGISTER SEQUENCE SST25VF016B/032B



SST25VF016B/032B TO SST26VF016B AND SST26VF032B/032BA

FIGURE 2-2: WRITE-STATUS-REGISTER SEQUENCE SST26VF016B AND SST26VF032B/032BA



2.2 Device Protection

SST26VF016B and SST26VF032B/032BA employ a new protection scheme that allows for more flexibility and a higher level of protection in comparison to the SST25VF016B/032B. SST25VF016B/032B offer traditional memory protection via block protection bits in the Status Register, whereas SST26VF016B and SST26VF032B/032BA support individual block protection via Block Protection Register instructions.

All the parts power up with memory protected. To execute Program or Erase commands, remove the protection.

To remove the memory protection of SST25VF016B and SST25VF032B, clear the protection bits in the status register. The status register contains protection bits BP0, BP1, BP2, and BP3, all of which are set to 0 to clear all protection.

SST26VF016B and SST26VF032B/032BA support the Global Block-protection Unlock command (98H) to unlock the entire memory. [Table 2-4](#) lists all block protection commands for SST26VF016B and SST26VF032B/032BA.

**TABLE 2-4: BLOCK PROTECTION COMMANDS
SST26VF016B AND
SST26VF032B/032BA**

Instruction	OpCode
Read Block Protection Register	72H
Write Block Protection Register	42H
Lock Down Block Protection Register	8DH
non-Volatile Write Lock-Down Register	E8H
Global Block Protection Unlock	98H

2.3 Device ID

Each part uses a different device ID. See [Table 2-5](#).

TABLE 2-5: DEVICE ID

Part	Device ID
SST25VF016B	BF2541H (BFH = Manufacturer ID, 25H = Memory Type, and 41 = Device ID)
SST25VF032B	BF254AH (BFH = Manufacturer ID, 25H = Memory Type, and 4A = Device ID)
SST26VF016B	BF2641H (BFH = Manufacturer ID, 26H = Memory Type, and 41 = Device ID)
SST26VF032B/032BA	BF2642H (BFH = Manufacturer ID, 26H = Memory Type, and 42 = Device ID)

The device IDs for all devices are accessed with the same operation command and protocol, but the return data will be different for each device. See [Table 2-6](#) for more information about the operation commands.

SST26VF016B and SST26VF032B/032BA support JEDEC's Serial Flash Discoverable Parameters (SFDP) v1.1 as an additional method of device identification.

2.4 Programming

SST25VF016B/032B allow Byte Program and AAI Word Program instructions for programming. SST26VF016B and SST26VF032B/032BA allow Page Program instruction for programming.

Byte Program and AAI-word Program allow programming one and two bytes of data respectively, while the Page Program instruction allows programming one to 256 bytes of data at a time using either SPI or SQI protocol.

For SST25VF016B/032B, the maximum time to program one byte of data using Byte Program instruction, or two bytes of data using AAI-word Program instruction, is 10 μ s. For SST26VF016B and SST26VF032B/

032BA, the typical time to program the first byte of data using Page Program instruction is 50 μ s and the time to program subsequent bytes is 4 μ s (typical). To program 256 bytes of data with SST26VF016B or SST26VF032B/032BA using Page Program instruction takes 1.5ms maximum. If less than 256 bytes of data is programmed, it would take less than the 1.5ms maximum time. Before proceeding to the next instruction, the controller can either wait the maximum program time or keep reading the status register to detect end of programming.

The Byte Program, AAI Word- Program instruction and Page-Program instruction are shown in Figures 2-3 –2-6.

FIGURE 2-3: BYTE PROGRAM SST25VF016B/032B

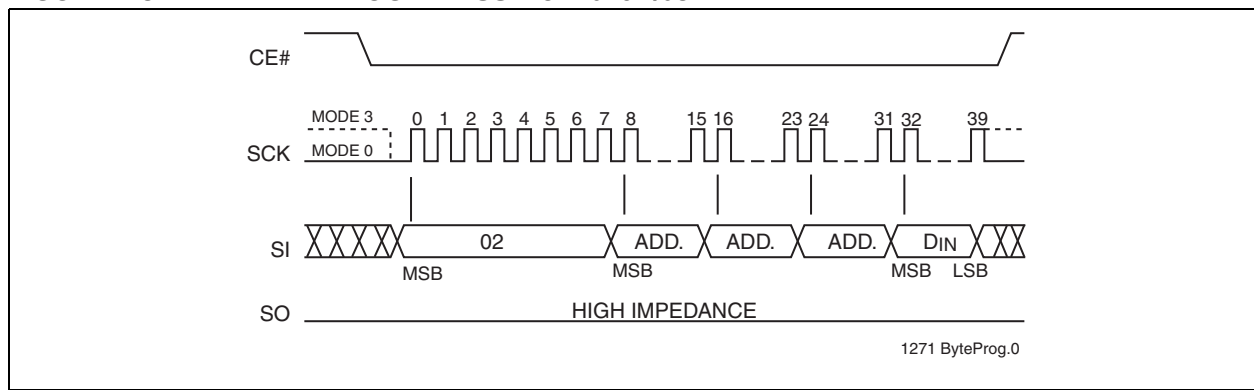
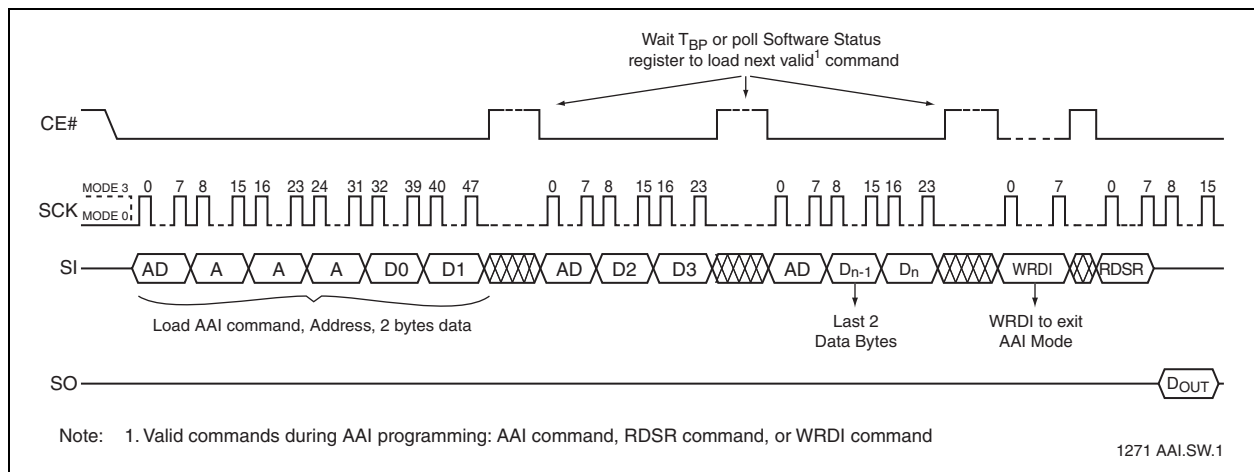


FIGURE 2-4: AAI WORD PROGRAM SST25VF016B/032B



SST25VF016B/032B TO SST26VF016B AND SST26VF032B/032BA

FIGURE 2-5: PAGE PROGRAM INSTRUCTION SST26VF016B AND SST26VF032B/032BA(SQI)

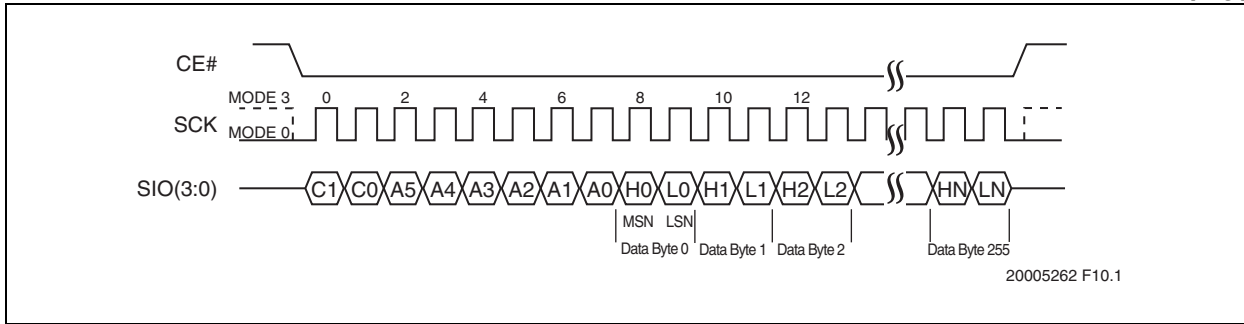
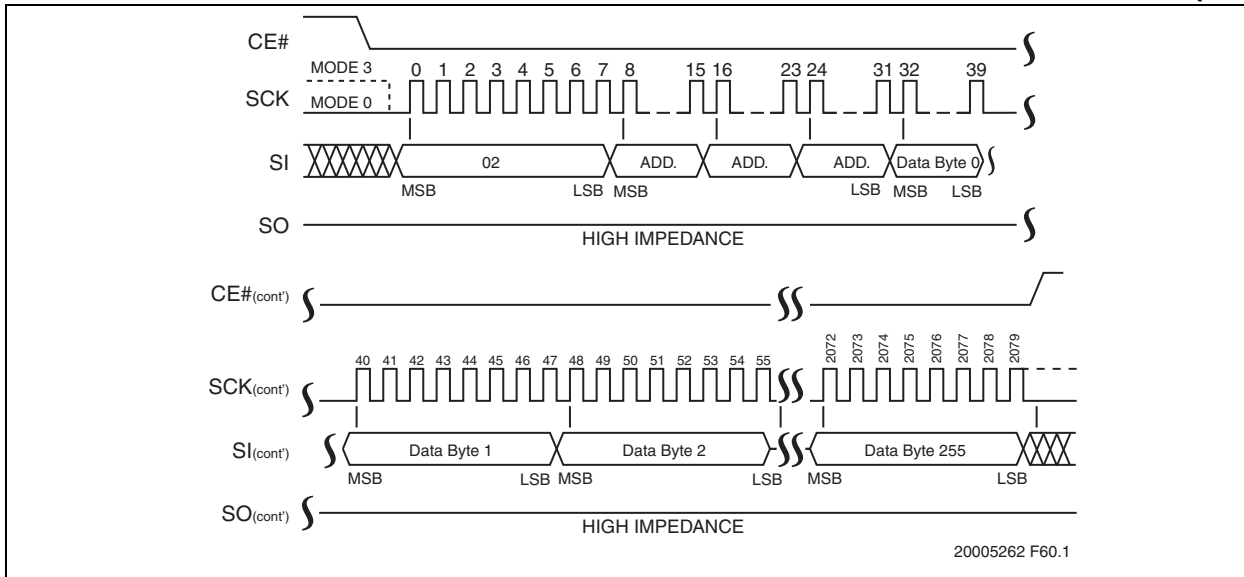


FIGURE 2-6: PAGE PROGRAM INSTRUCTION SST26VF016B AND SST26VF032B/032BA (SPI)



2.5 Communication Protocol

SST25VF016B/032B only utilize SPI protocol, but SST26VF016B and SST26VF032B/032BA can use either SPI and SQI protocol. SST26VF016B or SST26VF032B will work with a host controller that only supports SPI. If the host controller supports both SPI and SQI, then all the features of SST26VF016B and SST26VF032B/032BA are available.

SST25VF016B/032B support a clock frequency up to 80MHz and SST26VF016B and SST26VF032B/032BA support a clock frequency up to 104MHz.

2.6 Host Controller Supports SPI

Most operation commands of SST25VF016B/032B are compatible with SST26VF016B or SST26VF032B with minimal changes required. See [Table 2-6](#).

TABLE 2-6: OPERATION COMMAND COMPATIBILITY

SST25VF016B/032B Device Operation Instructions	OpCode	Compatible with SST26VF016B/032B/032BA	Comments
Read	03H	Yes	
High-Speed Read	0BH	Yes	
4 KB Sector-Erase	20H	Yes	
32KByte Block Erase	52H	Change Required	This command is not supported in SST26VF016B and SST26VF032B/032BA. For 32 KByte Block Erase, use D8H.
64KByte Block Erase	D8H	Change Required	The memory maps of SST25VF016B/032B and SST26VF016B or SST26VF032B/032BA are different. See the applicable data sheets for more information.
Chip-Erase	60H or C7H	Change Required	SST26VF016B and SST26VF032B/032BA supports C7H but not 60H instruction
Byte-Program ¹	02H	Change Required	SST26VF016B and SST26VF032B/032BA support Page-Programming and the 02H instruction is a page-programming instruction.
AAI Word-Program	ADH	Change Required	SST26VF016B and SST26VF032B/032BA do not support AAI, and the ADH instruction is not supported.
RDSR	05H	Yes	
EWSR	50H	No	Not supported by SST26VF016B and SST26VF032B/032BA
WRSR	01H	Change Required	The parts use different block protection schemes and the block protection bits in the Status Register are removed from SST26VF016B and SST26VF032B/032BA. WRSR instructions for SST26VF016B and SST26VF032B/032BA ignore Write to the 1st data byte to the Status Register, and only accept Write to the 2nd data byte for the Configuration Register.
WREN	06H	Yes	
WRDI	04H	Yes	
RDID	90H or ABH	No	Not supported by SST26VF016B and SST26VF032B/032BA
JEDEC-ID	9FH	Yes	Device Id is different between the parts.
EBSY	70H	No	SST26VF016B and SST26VF032B/032BA do not support RY/BY# status on output pin.
DBSY	80H	No	

1. Byte Programming can be done in SST26VF016B and SST26VF032B/032BA using the Page Program opcode 02H. However, the programming time to complete programming a byte using Page Program command is typically 50 μ s

2.7 Host Controller Supports Both SPI and SQI

If the host controller can support both SPI and SQI protocol then the above changes described are still relevant and in addition all features of SST26VF016B and SST26VF032B/032BA are now available for use. A review of the current methods/code to perform Read and Program operations must be done and the firmware should be upgraded to take advantage of all the features available as described in the data sheet.

SST26VF016B and SST26VF032B/032BA support higher functionality and performance such as:

- up to 104 MHz operating frequency
- multi-I/O read/program capability
- enhanced security and OTP security memory area outside of the main memory array
- JEDEC Serial Flash Discoverable Parameters (SFDP)
- Suspend Program/Erase capability.

Refer to the SST26VF016B and SST26VF032B/032BA data sheet for detailed instructions.

2.8 Conclusion

This document describes the aspects to consider when migrating from SST25VF016B/032B to SST26VF016B or SST26VF032B/032BA. SST26VF016B and SST26VF032B/032BA are great choices because they support higher clock frequency, uses both SPI and SQI protocol, and continue to provide the superior reliability represented by SuperFlash® technology.

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