REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		5-07-13
B	Corrected RGMII_ID_MODE Polarities		10-08-13
C	Added GPIO Reset Requirement		11-21-14

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN8820, 56-pin QFN Package

MICROCHIP

SMSC
SUCCESS BY DESIGN

SMSC
80 Arkay Drive, Suite 100
Hauppauge, New York 11788

Document Number	Revision
SC471244	**C**

Schematic Checklist for LAN8820

Information Particular for the 56-pin QFN Package

LAN8820 QFN Phy Interface:

1. TR0P (pin 44); This pin is the transmit/receive positive channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

2. TR0N (pin 43); This pin is the transmit/receive negative channel 0 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

3. TR1P (pin 47); This pin is the transmit/receive positive channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

4. TR1N (pin 46); This pin is the transmit/receive negative channel 1 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

5. TR2P (pin 52); This pin is the transmit/receive positive channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

6. TR2N (pin 51); This pin is the transmit/receive negative channel 2 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

7. TR3P (pin 55); This pin is the transmit/receive positive channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

8. TR3N (pin 54); This pin is the transmit/receive negative channel 3 input/output connection of the internal Phy. It requires a 49.9Ω, 1.0% pull-up termination resistor. The termination resistor must be biased to a +2.5V supply. This pin also connects to the 10/100/1000 magnetics.

9. For Transmit/Receive Channel connections and termination details, refer to Figure 1.

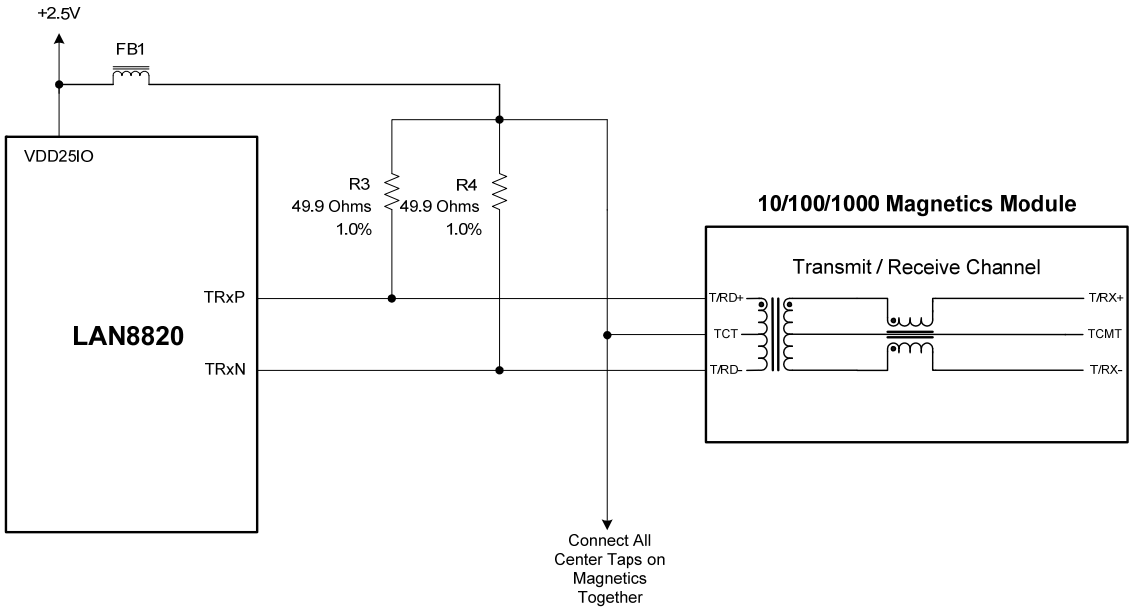


Figure 1 – Transmit / Receive Channel x Connections and Terminations

LAN8820 QFN Magnetics:

1. The center tap connection on the LAN8820 side for each channel must be connected to the same power supply as the bias supply for the Ethernet terminations.

2. The center tap connection on the cable side (RJ45 side) for each channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

3. Assuming the design of an end-point device (NIC), TR0P (pin 44) of the LAN8820 QFN should trace through the magnetics to pin 1 of the RJ45 connector.

4. Assuming the design of an end-point device (NIC), TR0N (pin 43) of the LAN8820 QFN should trace through the magnetics to pin 2 of the RJ45 connector.

5. Assuming the design of an end-point device (NIC), TR1P (pin 47) of the LAN8820 QFN should trace through the magnetics to pin 3 of the RJ45 connector.

6. Assuming the design of an end-point device (NIC), TR1N (pin 46) of the LAN8820 QFN should trace through the magnetics to pin 6 of the RJ45 connector.

7. Assuming the design of an end-point device (NIC), TR2P (pin 52) of the LAN8820 QFN should trace through the magnetics to pin 4 of the RJ45 connector.

8. Assuming the design of an end-point device (NIC), TR2N (pin 51) of the LAN8820 QFN should trace through the magnetics to pin 5 of the RJ45 connector.

9. Assuming the design of an end-point device (NIC), TR3P (pin 55) of the LAN8820 QFN should trace through the magnetics to pin 7 of the RJ45 connector.

10. Assuming the design of an end-point device (NIC), TR3N (pin 54) of the LAN8820 QFN should trace through the magnetics to pin 8 of the RJ45 connector.

RJ45 Connector:

1. The RJ45 shield should be attached directly to chassis ground.

VDD25IO Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN8820. All power pins on the LAN8820 must be supplied by external power supplies.

2. The power drawn by the VDD25IO pins, the Ethernet terminations and the 10/100/1000 magnetics is approximately 238 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

3. The VDD25IO supply pins on the LAN8820 QFN are 7, 19, 24 & 37. These pins require a connection to +2.5V.

4. Each VDD25IO pin should also have one .01 μF (or smaller) capacitor to decouple the LAN8820. The capacitor size should be SMD_0603 or smaller.

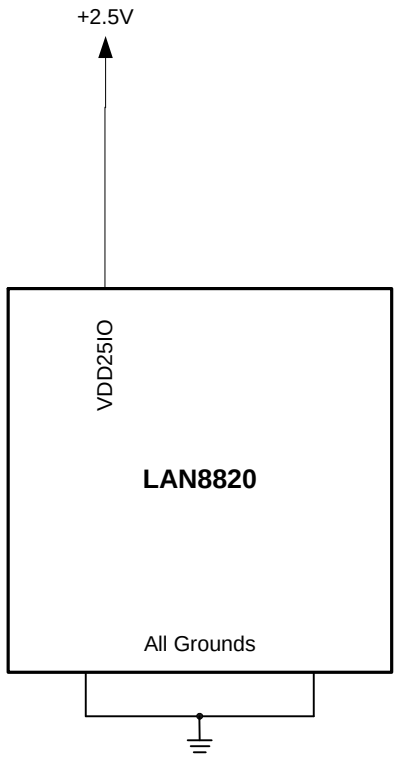


Figure 2 - VDD25IO Power Supply Connections

+1.2V Power Supply Connections:

1. **Note:** There are no internal regulators within the LAN8820. All power pins on the LAN8820 must be supplied by external power supplies.

2. The power drawn by the VDD12CORE pins, the VDD12A pins, the VDD12BIAS pin, and the VDD12PLL pin is approximately 454 mA. The design engineer should be sure to size the external power supply appropriately being able to supply at least two times the expected current. This should allow for enough headroom to compensate for any system variations.

3. VDD12CORE (pins 8, 13, 20, 23, 30 & 36), these six pins must be connected to an external +1.2V supply and provide power to the +1.2V core of the LAN8820.

4. The VDD12CORE pins should each have one .01 μF (or smaller) capacitor to decouple the LAN8820. The capacitor size should be SMD_0603 or smaller.

5. VDD12A (pins 45, 48, 53 & 56), these four pins supply power to the analog block of the LAN8820. These pins must be connected to an external +1.2V supply through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. The VDD12A pins should each have one .01 μF (or smaller) capacitor to decouple the LAN8820. The capacitor size should be SMD_0603 or smaller.

7. VDD12BIAS (pin 49), this pin must be connected to an external +1.2V supply directly (no ferrite bead required).

8. The VDD12BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN8820. The capacitor size should be SMD_0603 or smaller.

9. VDD12PLL (pin 50), this pin supplies power for the Ethernet PLL. This pin must be connected to an external +1.2V power supply through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

10. The VDD12PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN8820. The capacitor size should be SMD_0603 or smaller.

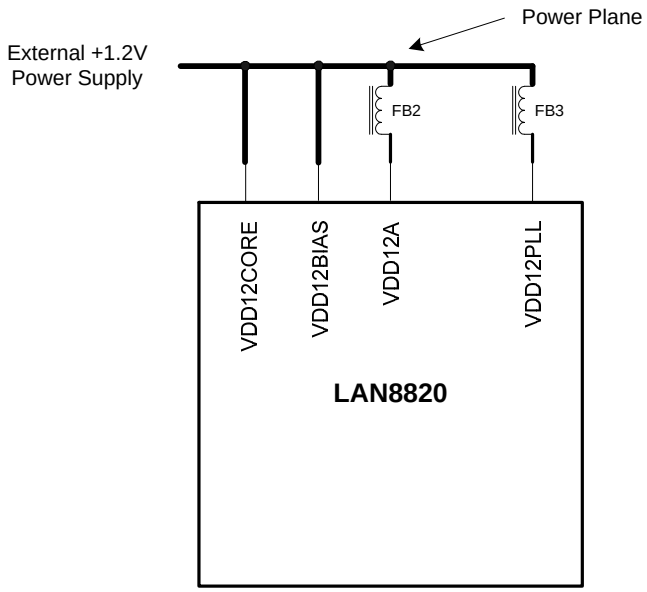


Figure 3 - LAN8820 +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN8820 QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN8820 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN8820 QFN. For exact specifications and tolerances refer to the latest revision LAN8820 data sheet.

2. XI (pin 5) on the LAN8820 QFN is the clock circuit input. This pin requires a 27 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 6) on the LAN8820 QFN is the clock circuit output. This pin requires a matching 27 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN8820 QFN.

ETHRBIAS Resistor:

1. ETHRBIAS (pin 42) on the LAN8820 QFN should connect to digital ground through a 8.06K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 17) requires an external pull-up resistor to VDD25IO as this output is an Open Drain type.

2. When using the RGMII interface of the LAN8820 with a MAC device on board, a pull-up resistor on the MDIO signal (pin 41) is required. A pull-up resistor of 1.5KΩ to VDD25IO is required for this application

RGMII Interface:

1. The following table indicates the proper connections for the 14 RGMII signals.

From:	Connects To:	
LAN8820 QFN	**RGMII MAC Device**	**Notes**
RXD0 (pin 9)	RXD<0>	
RXD1 (pin 10)	RXD<1>	
RXD2 (pin 11)	RXD<2>	
RXD3 (pin 12)	RXD<3>	
RXD4	RXD<4>	Not Used in RGMII Mode
RXD5	RXD<5>	Not Used in RGMII Mode
RXD6	RXD<6>	Not Used in RGMII Mode
RXD7	RXD<7>	Not Used in RGMII Mode
RXCTRL (pin 14)	RXCTRL	
RX_DV	RX_DV	Not Used in RGMII Mode
RX_ER	RX_ER	Not Used in RGMII Mode
RXC (pin 18)	RX_CLK	
TX_ER	TX_ER	Not Used in RGMII Mode
TXD0 (pin 27)	TXD<0>	
TXD1 (pin 26)	TXD<1>	
TXD2 (pin 25)	TXD<2>	
TXD3 (pin 22)	TXD<3>	
TXD4	TXD<4>	Not Used in RGMII Mode
TXD5	TXD<5>	Not Used in RGMII Mode
TXD6	TXD<6>	Not Used in RGMII Mode
TXD7	TXD<7>	Not Used in RGMII Mode
TXCTRL (pin 28)	TXCTRL	
TX_EN	TX_EN	Not Used in RGMII Mode
TXC (pin 29)	TX_CLK	
GTXCLK	GTX_CLK	Not Used in RGMII Mode
CRS	CRS	Not Used in RGMII Mode
COL	COL	Not Used in RGMII Mode
MDIO (pin 41)	MDIO	
MDC (pin 40)	MDC	

2. Provisions should be made for series terminations for all outputs on the RGMII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8820 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω.

CONFIG[3..0] Pins:

1. CONFIG0 (pin 39) This pin sets the PHYADD[1:0] bits of the 10/100 Special Modes Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDD25IO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

2. CONFIG1 (pin 38) This pin sets the PAUSE bit of the Auto Negotiation Advertisement Register and PHYADD [2] bit of the 10/100 Special Modes Register on reset or power up. It must be connected to VSS, 100_LED, 1000_LED, or VDD25IO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

3. CONFIG2 (pin 35) This pin sets the MOD[1:0] bits of the Extended Mode Control/Status Register on reset or power up. It must be connected to VSS, 100_LED, 1000_LED, or VDD25IO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

4. CONFIG3 (pin 34) This pin sets the CLK125DIS bit and MOD[3] bit of the Extended Mode Control/Status Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDD25IO. Refer to the latest revision of the data sheet, Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," for additional information.

LED pins:

1. 10_LED (pin 33) This LED pin indicates the 10BASE-T Link status of the Phy.

2. 100_LED (pin 32) This LED pin indicates the 100BASE-TX Link status of the Phy.

3. 1000_LED (pin 31) This LED pin indicates the 1000BASE-T Link status of the Phy.

Dedicated Configuration Strap Pins:

1. HPD_MODE (pin 32), this configuration strap is used to select the Hardware Power Down (HPD) mode. When pulled-up, the PLL is not disabled when HPD is asserted. When pulled-down, the PLL is disabled when HPD is asserted. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDD25IO.

2. REFCLK_SEL (pin 33), this configuration strap is used to select the XI pin's reference clock frequency input. When pulled-up, a 125MHz reference clock is selected. When pulled-down, a 25MHz reference clock is selected. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDD25IO.

3. RGMII_ID_MODE (pin 31), this configuration strap is used to configure the RGMII PHY TXC/RXC delay enable bit defaults. When pulled-up, the RGMII PHY TXC/RXC delays are enabled by default. When pulled-down, the RGMII PHY TXC/RXC delays are disabled by default. Refer to Section 3.3, "RGMII Interface," for more information. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDD25IO.

Miscellaneous:

1. There is one No-Connect pin on the LAN8820. It is very important that this pin remains as a no-connect. This is pin 21 on the device.

2. nRESET (pin 16), this pin is an active-low reset input. This signal resets all logic and registers within the LAN8820. This signal is pulled high with a weak internal pull-up resistor. The nRESET should not be left unconnected as the +3.3V internal power-on reset circuitry is RC based.

3. A hardware reset (nRESET assertion) is required by the LAN8820 following power-up. Refer to Section 5.5.3, "Power-On Reset Timing," in the data sheet for additional information. Microchip does not recommend the use of an RC circuit or POR monitor for this pin reset. A controllable reset (GPIO) is recommended. In this case, Microchip recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

4. In certain conditions and on certain parts, the device may report all normal functionality, but not be able to link in Gigabit Ethernet mode when connected to a Gigabit Ethernet partner. In this mode, 100BASE-TX and 10BASE-T modes will remain functional. The possibility of encountering this state depends on the power supply ramp rates along with the device temperature when powering up the device. In the affected state, if a Gigabit partner is connected, the Auto-Negotiation process will continually restart and no Ethernet link will be achieved. System implementers must follow the power-on procedure detailed in the LAN8820/LAN8820i Datasheet section 3.6.1 to alleviate the possibility of encountering the event.

5. HPD (pin 15), this pin places the device into Hardware Power Down (HPD) mode. Refer to the latest revision of the data sheet, Section 3.7.3, "Hardware Power-Down," for additional information. This pin has a weak internal pull-down and can be driven high with an external 1.0K Ω resistor to VDD25IO.

6. The LAN8820 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN8820 data sheet.

7. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

8. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

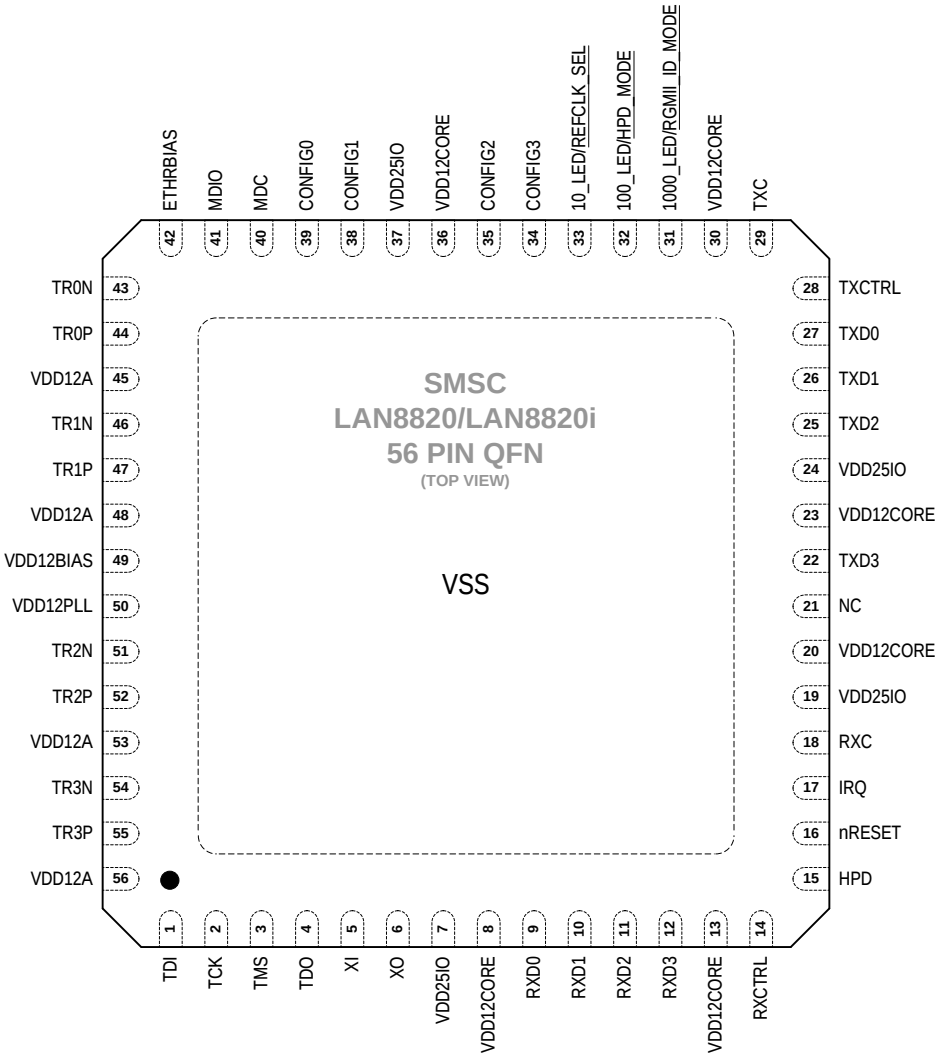
LAN8820 QFN QuickCheck Pinout Table:

Use the following table to check the LAN8820 QFN shape in your schematic.

LAN8820 QFN			
Pin No.	Pin Name	Pin No.	Pin Name
1	TDI	29	TXC
2	TCK	30	VDD12CORE
3	TMS	31	1000_LED / RGMII_ID_MODE
4	TDO	32	100_LED / HPD_MODE
5	XI	33	10_LED / REFCLK_SEL
6	XO	34	CONFIG3
7	VDD25IO	35	CONFIG2
8	VDD12CORE	36	VDD12CORE
9	RXD0	37	VDD25IO
10	RXD1	38	CONFIG1
11	RXD2	39	CONFIG0
12	RXD3	40	MDC
13	VDD12CORE	41	MDIO
14	RXCTRL	42	ETHRBIAS
15	HPD	43	TR0N
16	nRESET	44	TR0P
17	IRQ	45	VDD12A
18	RXC	46	TR1N
19	VDD25IO	47	TR1P
20	VDD12CORE	48	VDD12A
21	NC	49	VDD12BIAS
22	TXD3	50	VDD12PLL
23	VDD12CORE	51	TR2N
24	VDD25IO	52	TR2P
25	TXD2	53	VDD12A
26	TXD1	54	TR3N
27	TXD0	55	TR3P
28	TXCTRL	56	VDD12A
57		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN8820 QFN Package Drawing:



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Reference Material:

1. SMSC LAN8820 Data Sheet; check web site for latest revision.
2. SMSC LAN8820 Reference Design, check web site for latest revision.
3. SMSC Reference Designs are schematics only; there are no associated PCBs.