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DOCUMENT DESCRIPTION

Routing Checklist for the LAN9311I, 128-pin XVTQFP Package

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Routing Checklist for LAN9311I

Information Particular for the 128-pin XVTQFP Package

LAN9311I XVTQFP Phy No. 1 Interface:

1. The traces connecting the transmit outputs (TXP1, pin 111) & (TXN1, pin 110) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the receive inputs (RXP1, pin 116) & (RXN1, pin 115) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

4. The VDD33A1 power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

5. The union of the 10.0Ω resistor supplying VDD33A1 to the Transmit & Receive Channel center taps of the magnetics and the 0.022 μF capacitor, should be routed as a mini-plane.

LAN9311I XVTQFP Phy No. 2 Interface:

1. The traces connecting the transmit outputs (TXP2, pin 126) & (TXN2, pin 127) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the receive inputs (RXP2, pin 123) & (RXN2, pin 124) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

4. The VDD33A2 power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

5. The union of the 10.0Ω resistor supplying VDD33A2 to the Transmit & Receive Channel center taps of the magnetics and the 0.022 μF capacitor, should be routed as a mini-plane.

LAN9311I XVTQFP Magnetics No. 1 & No. 2:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

RJ45 Connector No. 1 & No. 2:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.

2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

+3.3V Power Supply Connections:

1. Route the (16) VDD33IO pins of the LAN9311I XVTQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (16) VDD33IO decoupling capacitors for the LAN9311I XVTQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

3. Route the (2) VDD33A1 pins of the LAN9311I XVTQFP directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the (2) VDD33A1 decoupling capacitors for the LAN9311I XVTQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

5. Also, route the VDD33A1 bulk capacitor for the LAN9311I XVTQFP power pins as short as possible directly to the VDD33A1 power plane.

6. Route the (2) VDD33A2 pins of the LAN9311I XVTQFP directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.

7. In addition, route the (2) VDD33A2 decoupling capacitors for the LAN9311I XVTQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

8. Also, route the VDD33A2 bulk capacitor for the LAN9311I XVTQFP power pins as short as possible directly to the VDD33A2 power plane.

9. Route the VDD33BIAS pin 120 of the LAN9311I XVTQFP directly into a solid, +3.3V power plane created through a ferrite bead. The pin-to-plane trace should be as short as possible and as wide as possible.

10. In addition, route the VDD33BIAS decoupling capacitor for the LAN9311I XVTQFP power pins as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

11. Also, route the VDD33BIAS bulk capacitor for the LAN9311I XVTQFP power pin as short as possible directly to the VDD33BIAS power plane.

VDD18CORE:

1. The VDD18CORE (pin 74) must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it. Pin 74 and the caps should be routed directly into a solid, +1.8V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. The other (6) VDD18CORE pins should be routed directly into this same solid, +1.8V power plane. The pin-to-plane trace should be as short as possible and as wide as possible. Be sure to use multiple vias as necessary.

3. In addition, route the (7) VDD18CORE decoupling capacitors for the LAN9311I XVTQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.8V & digital ground plane) for each cap.

4. The VDD18PLL (pin 107) must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it. Pin 107 and the caps should be routed through the associated ferrite bead directly into a solid, +1.8V power plane (VDD18CORE).

5. **Do Not**, under any circumstances, connect VDD18CORE to VDD18TX2. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9311I.

6. **Do Not**, under any circumstances, use either VDD18CORE or VDD18TX2 to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9311I only.

VDD18TX2:

1. The VDD18TX2 (pin 121) must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it.

2. The VDD18TX1 (pin 118) must be routed with a heavy, wide trace with multiple vias to the single decoupling cap associated with it and then routed with a heavy trace to pin 121.

3. **Do Not**, under any circumstances, connect VDD18TX2 to VDD18CORE. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9311I.

4. **Do Not**, under any circumstances, use either VDD18TX2 or VDD18CORE to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9311I only.

Ground Connections:

1. The (7) digital ground pins (VSS) on the LAN9311I XVTQFP should be routed directly into a solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

2. We recommend that the Digital Ground pins (VSS) and the Analog Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

3. The LAN9311I XVTQFP device does have an exposed die paddle ground. Simply connect all ground pins (VSS) directly to a solid, contiguous ground plane. The digital ground pin (pin 129, EDP) on the LAN9311I XVTQFP should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 25 power vias in a 5x5 grid.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

EEPROM Interfaces:

Microwire™ (3-wire) EEPROM Interface:

1. There are no critical routing instructions for the Microwire EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

I^2C (2-wire) EEPROM Interface:

1. There are no critical routing instructions for the I^2C EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

EXRES Resistor:

1. The EXRES resistor (pin 119) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-ups/Pull-down connections.

CPU Interface

1. Good, general design practices should be adhered to ensure proper operation.
2. Follow recommended processor design guidelines to ensure proper operation.
3. Follow recommended interpair spacing guidelines within data bus byte lanes, address bus and control group signals.
4. Follow recommended intrapair spacing guidelines between data bus byte lanes, address bus and control group signals.
5. As with any high-speed design interface, it is the design engineer's responsibility to review the PCB routing for specification adherence. The design engineer should review all timing relationships as put forth in the selected processor's data sheet and the LAN9311I XVTQFP data sheet and make certain that any PCB routing does not add significant timing delays. These timing relationships can be found in the Host Bus System Timing section of the LAN9311I XVTQFP data sheet.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN9311I XVTQFP device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.